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Development and Validation of a Smart Architecture for Thyristor Valves

G. Sala, *Member, IEEE*, G. De Bonis, A. Costabeber (*), A. Tani,
M. Johnson *Senior Member, IEEE*, J. Clare *Senior Member, IEEE*

Abstract – A high voltage thyristor converter is realized by many valve sections, whose volume is approximately occupied for only the 10% by thyristors and for the 10% by the relevant gate drivers. The remaining 80% is taken by passive auxiliary circuits, needed to protect thyristors during turn-on and turn-off commutations. This work represents a preliminary validation of an innovative architecture that aims to reduce the auxiliary circuit cost, volume, and weight of the overall valve, through the investigation of active, instead of passive solutions. The work starts from investigation of the phenomena behind the valve transient behaviors and proceeds with simulations and experimental tests, using a reduced scale circuit prototype. The match between the obtained results validates the investigated active configurations, confirming that the proposed solution can be used for improving thyristor valves.

Index Terms – HVDC transmission, AC-DC power conversion, LCC converters, power semiconductor switches, thyristor valves.

I. INTRODUCTION

Nowadays HVDC (High Voltage DC) transmission represents the most suitable technical solution to transmit electrical power over long distances, generally above 800 km for overhead lines and above 50 km for submarine cables. The higher is the electrical power to be transmitted, the higher is the voltage level. For voltages of hundreds of kV and currents of a few kA, thyristor converters are one of the best solutions. Compared to other power semiconductor devices, thyristors feature the highest voltage withstanding capability and the highest efficiency. Despite the employment of thyristors is a mature and very reliable solution, it has some important drawbacks. The main one is the need of bulky, heavy, and expensive auxiliary circuits to protect thyristors during turn-on and turn-off commutations.

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Until the 1990s, most of the research focused on thyristors improvement, rather than overall valve enhancement. In 1987, M. L. Woodhouse wrote a paper about voltage and current stresses implications on valve design, which includes the statement: “the considerations that lead to a specific valve design remain a mystery” [1].

Since the 1990s, thyristor valves have improved also in terms of auxiliary circuits, but the main enhancements dwelled upon the passive components.

Even though the parameter extraction of a valve tower is a complex topic, an accurate model must be used to well predict the behavior of the converter and to design suitable passive circuits to suppress overvoltages and to protect from unacceptable currents in the thyristor series [2]. Analytical methods to extract the stray capacitances of the valve and studies on their effects on thyristors’ behavior have been developed, [3] - [4]. To improve the accuracy of detailed models, the circuit parameters can also be extracted by means of finite element and accurate numerical simulations [5]. Furthermore, to take into account of parameters such as temperature and electric field distribution in the components, the design of the passive components in the auxiliary circuits can be not straightforward, requiring multi-disciplinary analytical and numerical models [6].

The use of detailed models becomes even more important when the number of switching devices in series rises [7]. For example, a trigonometric exponential model has been extended to consider also the stray inductances in [8], showing how the solution helps to better predict current and overvoltage of the device. Also, conventional analytical methods based on low-frequency models can be not suitable for damping circuit design. For this purpose, a multi-objective optimization for the design of the damping circuit is proposed in [9]. Whereas the authors in [10] combined a wideband model, which exploits a genetic algorithm to determine its parameters from experimental results, with a deduction of the parasitic capacitances by means of boundary-element method. For this purpose, a more accurate overvoltage analysis, insulation design, and electromagnetic disturbance prediction was carried out.

Aim of this work is to validate a design solution based on an active system, that embeds auxiliary power electronic components. This system is capable of partially doing what is usually obtained by passive components, such as di/dt limiting during turn-on and voltage equalization during turn-off. The innovative solution is expected to reduce the overall cost, volume, and weight of thyristor valves, thanks to the

elimination of the passive components. In addition, the introduction of the active control does not require an accurate identification and design of the passive damping systems.

The expected advantages in terms of size and cost of smart thyristor valves aim to increase the number of applications for which HVDC is more competitive and convenient than HVAC.

Examining active solutions for the management of thyristors is a reasonable choice nowadays. In fact, available IGBTs and SiC MOSFETs have much higher current and voltage ratings and they have a considerably enhanced reliability than in the past decades. For example, in [11] the authors proposed the use of an active circuit made by parallel IGBTs to compensate for the difference in the leakage among series GCT thyristors, and in [12] a different approach is investigated for the voltage balancing of series SPETO thyristors.

In addition, the computational capacity of microcontrollers makes it possible to manage also fast and complex controls. As examples, strategies to compensate for voltage differences among series devices (IGBTs and SiC MOSFETs, respectively) are proposed in [13] and [14], where a turn-off delay compensation is introduced by the controller for this purpose. In [15] and [16] a similar problem is mitigated with suitable control algorithms of the series IGBTs in a director switch.

In the end, both the hardware to be used in the aimed auxiliary active circuits and the control needed have already reached the necessary technological level to be employed in the considered application.

Simulations and experimental tests have been carried out to assess the problem and validate the proposed solution. Turn-on and turn-off active control systems are analyzed independently, and the associated experimental tests are conducted separately. Both turn-on and turn-off active branches are realized by an auxiliary switch and an auxiliary resistance in series.

In Section II, the architecture of actual thyristor valves and the related transient phenomena are introduced. In Section III, the active control circuits that are analyzed in this work are presented. Before outlining the conclusions of the work, Section IV illustrates the simulation and experimental results obtained with a laboratory prototype.

II. ACTUAL THYRISTOR VALVES

Generally, the architecture design of thyristor valves involves only passive components, employed to protect thyristors during turn-on and turn-off transitions.

The key component of a thyristor valve is named as thyristor level. An electrical circuit of a thyristor level is schematized in Fig. 1. The circuit includes the thyristor (Thy), the gate driver (Gate Unit), the ohmic-capacitive damping branch (R_d - C_d), and the DC grading resistor (R_{dc}).

Thyristor levels are then connected in series with one saturable inductor (L_{SAT}) to obtain a section of the thyristor valve, and many sections in series constitute the valve module, as illustrated in the electrical circuit of Fig. 2 for a 2-sections 6-levels valve module.

Fig. 3 illustrates the layout of the same module as it could appear in many industrial valves. Various examples of similar

modules have been proposed for HVDC transmission projects [17]–[20].

Finally, the assembly of series thyristor modules realizes the thyristor valve. The number of sections in a module and the number of modules in series in a valve mainly depend on the overall DC voltage.

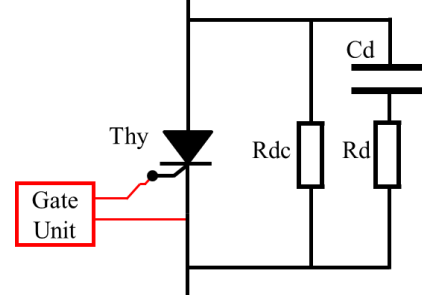


Fig. 1 - Electrical circuit of an actual thyristor level.

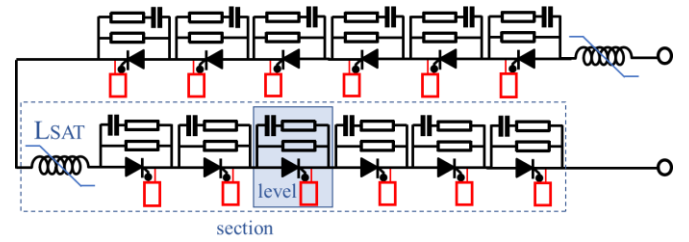


Fig. 2 - Electrical circuit of an actual thyristor valve module made of two 6-level sections in series, with their own saturable inductor each.

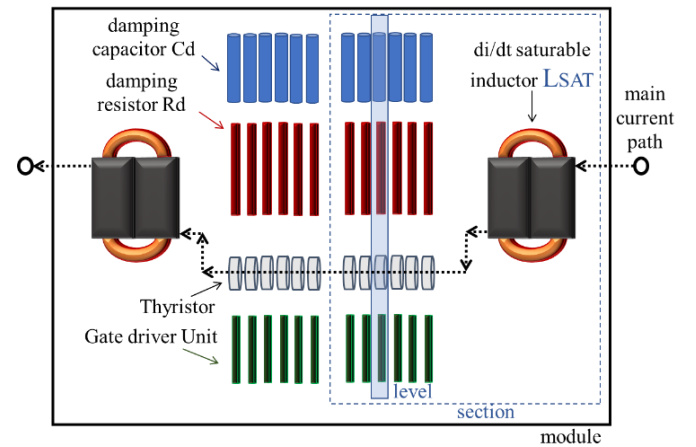


Fig. 3 - Layout of an actual thyristor valve module made of two 6-level sections in series, with their own saturable inductor each.

Considering actual valves, it is possible to note that about the 20% of the volume is occupied by the thyristors and by the relevant gate driver units, while the remaining space is taken by the auxiliary passive components and by the cooling system.

The passive components on which this research work is mostly focused are the di/dt saturable inductor (L_{SAT}) and the damping capacitors of the damping branch (C_d), aiming to investigate their potential size reduction or elimination.

The saturable inductor provides di/dt limiting during the initial stage of turn-on commutations, to protect thyristors from the discharge of the external stray capacitance (C_{STRAY}). This equivalent parasitic capacitance includes the contributions of the electric circuit that the valve is connected to.

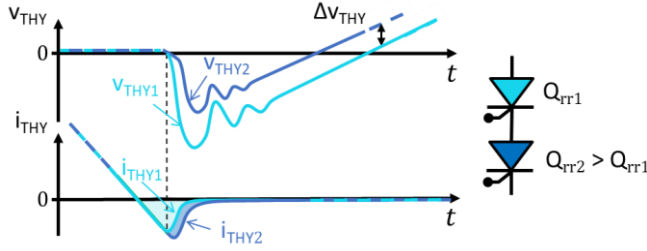


Fig. 4 – Currents and voltages of two series thyristors with different recovery charge values: typical waveforms during the turn-off process.

Furthermore, in case of unusually high blocking voltages, a relevant di/dt appears, adding an extra contribution to the stray current.

The damping branch (R_d - C_d , and R_{dc}) aims to provide both damping and voltage sharing equalization during turn-off transients and steady state operation. However, such a damping branch has several drawbacks in terms of parameter uncertainties, cost, volume, and efficiency limits of the passive components. Fig. 4 illustrates the current-voltage transients during a turn-off event of two thyristors in series and with unequal reverse recovery charge. The difference in the reverse recovery charges is highlighted by the colored area under the curve of the negative current waveshapes. Such a difference leads to an unbalanced turn-off process for the two thyristors, which results in higher voltage across the thyristor with lower reverse recovery charge.

III. AUXILIARY ACTIVE CONTROL CIRCUITS

The development of two active control circuits is introduced in this section. These active circuits aim to perform the same functions of the actual passive ones, while reducing the size of L_{SAT} and C_d . The focus of the analysis is on the specific configurations presented in the two Alstom Grid/ General Electric patents [21] and [22].

The turn-on and turn-off active circuits are independently realized, by two parallel branches with an auxiliary switch and an auxiliary resistance in series for each circuit. In fact, the transients during turn-on and turn-off are different and it would be impossible to implement both a turn-on and turn-off active control exploiting the same branch. Two different values of auxiliary resistance with two different power ratings are required. Consequently, turn-on and turn-off active control systems are analyzed and validated by separate simulations and experimental tests.

A. Turn-on Active Control Technique

The aim of the turn-on active control is to protect thyristors from excessive di/dt , minimizing the energy stored by L_{SAT} during the turn-on and reducing the size of L_{SAT} in terms of volume and weight.

The operating principle of the turn-on active control is presented for a valve level in Fig. 5. It consists in the diversion of the initial current spike from the stray capacitance C_{STRAY} , and the capacitance of the damping circuit C_d . Fig. 6 illustrates the concept of a diversion event for the last thyristor of the series (the bottom one in Fig. 6), highlighting the reduction of the current flowing through the thyristor (red curve) compared to the current diverted in the auxiliary branch (magenta curve) during the turn-on. The overall stray current and the load current flowing in the circuit are highlighted with blue and black dashed lines, respectively.

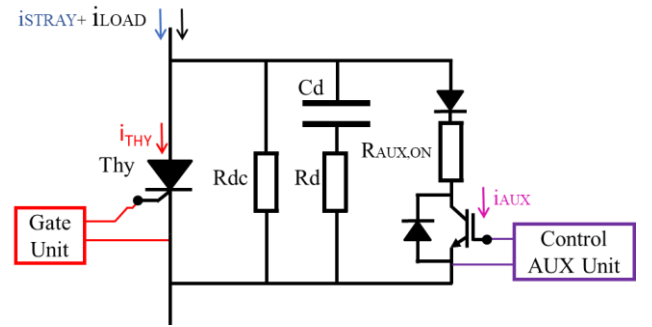


Fig. 5 - Electrical circuit of a valve level with the auxiliary active circuit for the turn-on control.

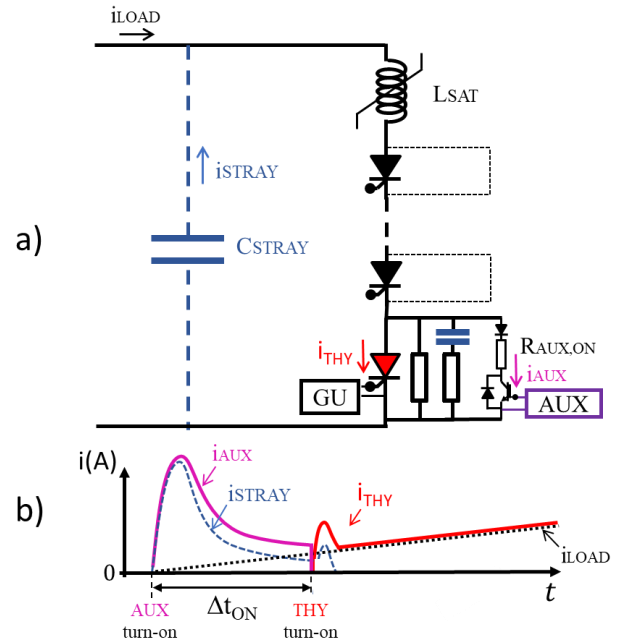


Fig. 6 - Electrical circuit of a valve, with highlighted the last level comprehensive of its auxiliary active circuit for the turn-on control (a) and expected current waveforms during the active diversion (b).

The diversion into the auxiliary branch is obtained by a turn-on of the auxiliary unit (AUX) before the turn-on of the main thyristor, which happens after a time interval Δt_{ON} named as diversion time [21].

To achieve a correct operation, the two parameters to be adjusted are the auxiliary turn-on resistance ($R_{AUX,ON}$) and the diversion time interval (Δt_{ON}). $R_{AUX,ON}$ is necessary to limit the current in the auxiliary switch and to dissipate the energy stored into the stray capacitances of the circuit. The value of $R_{AUX,ON}$ depends on the stray capacitance and its power rating must be established according to power losses during current diversion.

If the auxiliary switch is turned on a time interval Δt_{ON} (about 10 to 20 μs) before the turn-on of the main thyristor, the stray capacitances (e.g., C_{STRAY}) are discharged through the auxiliary resistance $R_{AUX,ON}$. During such a time interval, $i_{AUX} \approx i_{STRAY}$. It is necessary to find a trade-off between $R_{AUX,ON}$ and Δt_{ON} : increasing $R_{AUX,ON}$, the stray current waveform i_{STRAY} becomes lower and wider. For this reason, such an increase must be accompanied by an increase of the diversion time Δt_{ON} to allow the dissipation of most of the charge stored into the stray capacitances. However, the slower is the process the larger are the power losses. Consequently, $R_{AUX,ON}$ must be chosen as small as possible to obtain the quickest compensation process and the smallest losses. In addition, the minimum value of $R_{AUX,ON}$ is limited by the peak current, which depends on the stray currents. Generally, a detailed model of the converter would need to be considered, including all the relevant parasitic impedances. From the model it is possible to calibrate $R_{AUX,ON}$ and the corresponding diversion time interval Δt_{ON} . Once Δt_{ON} is determined, the control system turns out to be completely designed.

It is important to observe that delaying the thyristor turn-on does not fully eliminate the transient di/dt through the main thyristor during turn-on. For a complete release of the current stress during the transient, the diversion time interval Δt_{ON} would be theoretically infinite. When the gate driver is turned on, the residual discharge of the stray capacitances is no more limited by $R_{AUX,ON}$ and it discharges through the main thyristor. However, keeping the auxiliary branch on for a short time after the turn-on of the main thyristor helps to clamp the voltage across the thyristor during the spread of the current from a tiny area to the full surface of the device. After the spreading phase, the current of the thyristor equals the current of the load ($i_{THY} \approx i_{LOAD}$).

B. Turn-off Active Control Technique

The purpose of the turn-off active control is to ensure uniform voltage sharing in the blocking states, replacing, or reducing the damping capacitor (C_d). Voltage differences are caused by different reverse recovery charge (Q_{rr}) of thyristors in series (as shown in Fig.4), and the investigated technique has been called “faster device turn-off delay”. The principle of operation consists in connecting in parallel to the faster devices the respective auxiliary turn-off resistance ($R_{AUX,OFF}$) for proper time intervals. This strategy slows down the turn-off processes of the considered devices. In particular, this solution diverts part

of the reverse recovery current of the faster thyristor through the auxiliary circuit in order to slow down its turn-off process. Therefore, the turn-off active control mainly affects the turn-off of the faster devices, i.e., the ones with smaller Q_{rr} [22]. Fig. 7 shows an auxiliary branch connected in parallel to a valve level, while the concept of active voltage sharing process is illustrated in Fig. 8.

The developed technique is implemented with a PI (proportional-integral) closed loop control to determine the duty cycle of the auxiliary branch (i.e., Δt_{OFF} in Fig. 8). The PI regulator has the advantage of compensating the steady state error very effectively and the drawback of requiring a certain time interval before reaching the steady state (e.g., at first start-up of the system, and in case of sudden changes in the parameters of the devices during operation). Three parameters must be calibrated: the two PI gains and the $R_{AUX,OFF}$ value. The PI gains depend on $R_{AUX,OFF}$, while $R_{AUX,OFF}$ is a compromise between the value that gives a fast compensation process and the one that ensures no dangerous voltage steps. It is worth to highlight that the choice of $R_{AUX,OFF}$ and the active control tuning are function of the circuit parameters, which can change during operation. The design of the active system must consider such a variation range to reach the desired dynamic performance, whereas the steady-state equalization remains effective.

Different control strategies could be proposed and compared for further improvements in future research.

The active control aims to manage the turn-off auxiliary branch to reduce the size of the damping capacitor C_d .

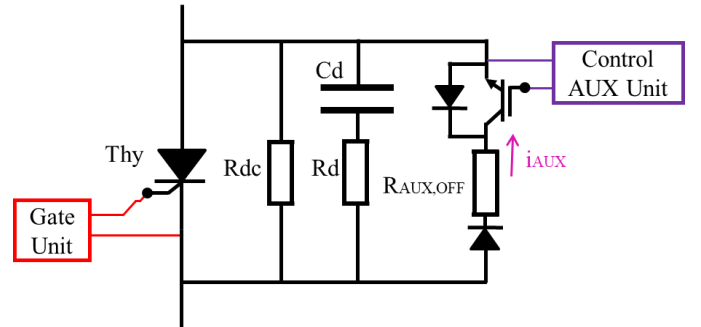


Fig. 7 – Electrical circuit of a valve level with the auxiliary active circuit for the turn-off control.

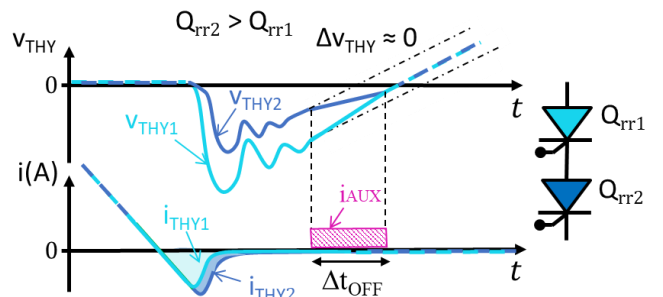


Fig. 8 – Current and voltage waveforms expected from the active compensation of the voltage differences during turn-off.

In both simulations and experimental tests, different combinations of the damping parameters have been compared to reduce the Cd value as much as possible without losing uniform voltage sharing. In the blocking diagram of Fig. 9, the “faster device turn-off delay” method is summarized. Such a method consists of measuring thyristor voltages in a discrete way, once every time the thyristor is turned off (after a sufficient time delay, from the zero crossing of the thyristor current, to make the reverse voltage independent of the turn-off transient), calculating the average voltage and voltage differences ($\Delta V_{THY,k}$), and eventually deciding the compensation time interval $\Delta t_{OFF,k}$ for the k -th thyristor of the series, addressed as “delay” value.

Voltages are measured after the negative current peak, and voltage unbalances among the devices in series ($\Delta V_{THY,k}$) are calculated as the differences between each voltage ($V_{THY,k}$) and the average one. Once the voltage unbalance for each thyristor level is available, it is elaborated by the PI control, which determines the time “delay” $\Delta t_{OFF,k}$, i.e., the time interval during which the auxiliary switch remains on. If this time is zero, the auxiliary circuit is not activated during the turn-off.

During the PI control transient, the voltage sharing of the thyristors is not uniform but, once the PI regulators reach suitable output values, the voltage sharing of the thyristors after the turn-off transient becomes uniform. The steady state “delay” related to each thyristor mainly depends on the reverse recovery charges Q_{rr} and, regardless their differences, the active control allows to approximately eliminate voltage unbalances at steady state. Both the frequency of the control algorithm and the one of the voltage measurements equal the operating frequency of the thyristor valves, which leads to low requirements in terms of computational time.

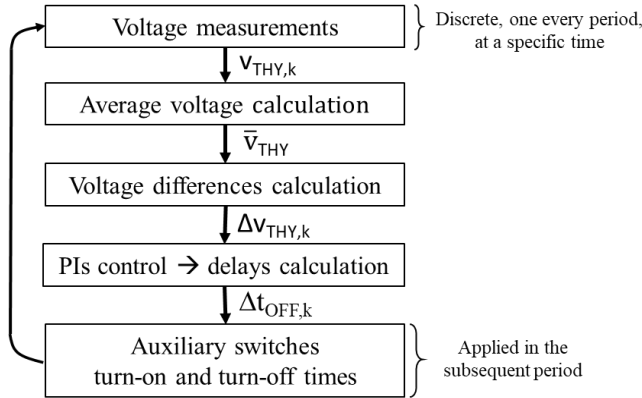


Fig. 9 – Block diagram of the “faster device turn-off delay” method.

IV. RESULTS

Simulations and reduced scale experiments have been carried out to validate the presented active control methods. Reduced scale experiments have advantages in terms of safety, cost, speed, and flexibility and represent the real scale operation with a satisfactory approximation. Fig. 10 show the experimental setup. The thyristors used for obtaining the results presented in the paper are Vishay VS-50RIA80, 800V, 50A, with a non-

uniform voltage sharing after turn-off which is attributed to a difference in the reverse recovery charges of about 13%.

In the experimental circuit, L_{SAT} was eliminated, as the effects of C_{STRAY} are not important in a reduced scale. The damping passive components Cd-Rd have been properly selected according to the experimental test to be carried out and their values have been chosen to validate the behavior of the device in a working operation, similar to the one of a full-scale system.

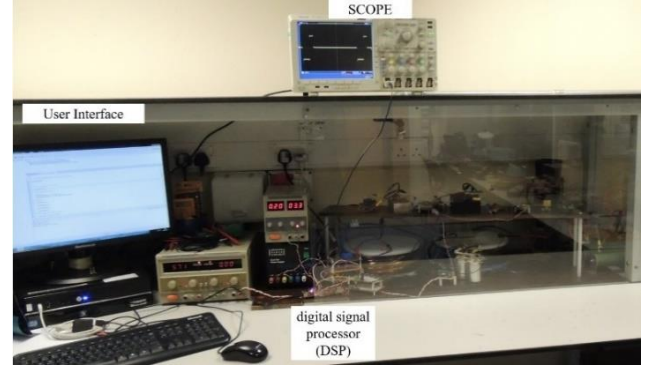


Fig. 10 – Experimental setup.

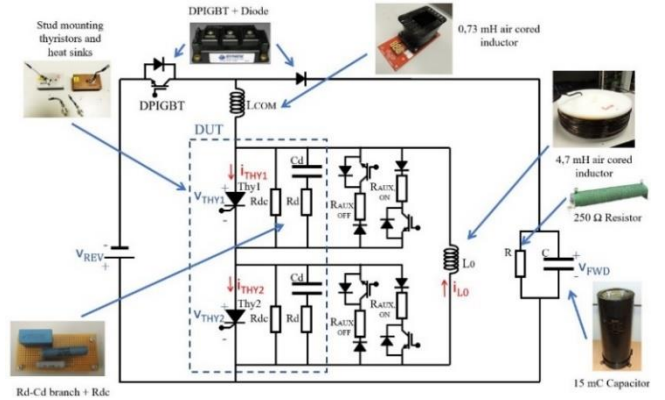


Fig. 11 – Circuit and components used for double pulse test validation of two series thyristors behavior.

A. Double Pulse Test Circuit

Fig. 11 shows the double pulse test circuit used for carrying out the experimental tests.

The control of the Double Pulse test IGBT (DFIGBT, as identified in Fig. 11) determines the state of the circuit.

Neglecting the effect of the Device Under Test (DUT) and the auxiliary circuits, the operating principle of the circuit is similar to a buck-boost converter which produces the desired voltage V_{FWD} at the terminals of the RC parallel branch.

In this operating condition, the DUT behaves mainly as an open circuit:

$$i_{DUT} \cong 0 \quad (1)$$

$$v_{DUT} = v_{THY1} + v_{THY2} \quad (2)$$

The DUT voltage is function of the i_{L_0} current as follows:

$$v_{DUT} = -L_0 \frac{di_{L_0}}{dt} \quad (3)$$

The dominating equation when the DPIGBT is on is:

$$\frac{di_{L_0}}{dt} \cong \frac{V_{REV}}{L_{COM} + L_0} \quad (4)$$

The dominating equation when the DPIGBT is off is:

$$\frac{di_{L_0}}{dt} = \frac{-V_{FWD}}{L_{COM} + L_0} \quad (5)$$

After the desired V_{FWD} voltage is reached, the DUT and auxiliary circuits are activated to analyze the effect of the auxiliary circuits on the behavior of the thyristors during turn-on and turn-off. When the DUT is conducting current, its dominating equations are:

$$v_{DUT} > 0 (\cong 0) \quad (6)$$

$$i_{DUT} \cong i_{L_0} \quad (7)$$

Considering a double pulse test, the operation of the circuit without the activation of the auxiliary circuits takes place through the following five steps:

1. The DPIGBT is turned on and current flows through the $V_{REV} - L_{COM} - L_0$ path until the desired current value for the forward conduction state of the DUT is reached. During this time interval, the dominating equations are (1)-(4);
2. When the aimed current value for the forward conduction state is obtained, the DPIGBT is turned off and current flows through the $V_{FWD} - L_{COM} - L_0$ loop until the DUT is turned on. During this time interval, the dominating equations are (1)-(3) and (5);
3. When the DUT is turned on, the additional current loop becomes the DUT - L_0 and L_0 behaves as a current source. The time interval between the DPIGBT turn-off and the DUT turn-on is as short as possible, to maintain current close to the value reached at the DPIGBT turn-off instant. During the DUT conduction, its current decreases according to the DUT on-state voltage, usually negligible compared to the reverse and forward voltage of the test circuit. In this time interval, the dominating equations are (3) and (6)-(7);
4. The turn-off of the thyristors (DUT) is obtained by turning the DPIGBT on again. This allows to measure the reverse recovery effect on the thyristor currents and voltages. Equations of interest after fast transients are as step 1.

5. The DPIGBT is turned off, to extinguish inductors residual current in the $V_{FWD} - L_{COM} - L_0$ loop. The main equations are the same of step 2, until the current becomes zero.

Depending on the experiment, a double pulse test might be a limit. For example, it cannot show the dynamic of the “turn-off delay” control method, which takes a certain number of cycles before reaching the steady state. This limit is overcome replacing the V_{FWD} power supply with an RC parallel branch, as in Fig. 11, and repeating steps 1, 2 and 3 periodically.

Concerning turn-on tests, it was not necessary to design the passive damping circuit Cd-Rd for voltage sharing purposes, as there is no need to connect many devices in series. As depicted in Fig. 4, the initial current spike during turn-on comes from both the stray capacitance and the damping capacitance. Therefore, the damping branch was used as the source of the current spike during turn-on, as there is no difference from the thyristor point of view. To provide a proper current spike waveform to be diverted, emulating the effect of both stray and damping circuits, the values $R_d = 12 \Omega$ and $C_d = 2 \mu F$ were selected. Regarding turn-off tests, the time constant of the damping circuit τ_d ($\tau_d = C_d \cdot R_d$) was considered about a tenth of the reverse recovery time. The Cd-Rd series combination is designed accordingly, also considering the voltage sharing requirements. The effective value of the reverse recovery time depends on the forward conduction current, which determines the amount of reverse recovery charge, and the turn-off current slope (di/dt). Also, the reverse recovery time varies significantly with the voltage rating of the device. The typical reverse recovery time of a real scale thyristor is about 500 μs and a reference value for the damping parameters can be $C_d = 1 \mu F$ and $R_d = 50 \Omega$ [6], [23]. For the considered reduced scale thyristors, the reverse recovery time is about 50 μs . Therefore, the damping parameters were chosen to obtain a time constant (τ) one tenth of the full-scale device ($\tau = 5 \mu s$): C_d was reduced ten times, leaving R_d to the same value, according to the need of reducing C_d to shrink the real scale valve. In this case, the reduced scale parameters became: $C_d = 100 \text{ nF}$, $R_d = 50 \Omega$.

For both turn-on and turn-off tests, the described experimental circuit is operated periodically, setting a period of 3 ms, i.e., a frequency of 333.3 Hz. Such a frequency is also the one of the voltage measurements and of the control algorithm.

B. Turn-on Control Method Results

Results of the turn-on control method are shown in Figs. 12-14. Fig. 12 shows voltage and current waveforms of the turn-on process without any current diversion, while Fig. 13 illustrates how such waveforms change after current diversion, setting the auxiliary branch resistance $R_{AUX,ON}$ to 3.4 Ω and the turn on delay Δt_{ON} to 80 μs . Finally, Fig. 14 depicts the current spike diverted into the auxiliary branch. The results show that the high initial current is effectively diverted into the auxiliary branch with the result that, at the thyristor turn-on, most of the stray capacitance current has been extinguished. Therefore, a lower stress of the thyristor is expected, with benefits in terms of aging and lifetime of the valve.

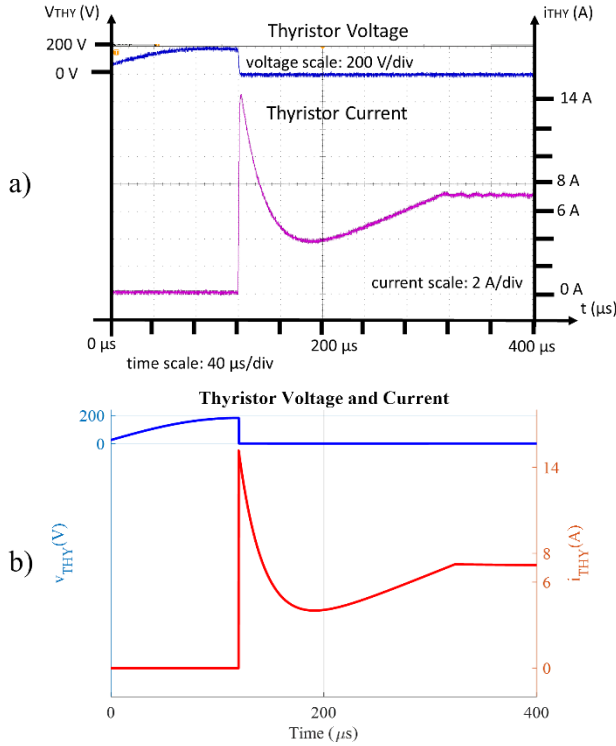


Fig. 12 – Turn-on process with no active control: current and voltage waveforms of the thyristor level. Experimental (a) and simulation (b) results.

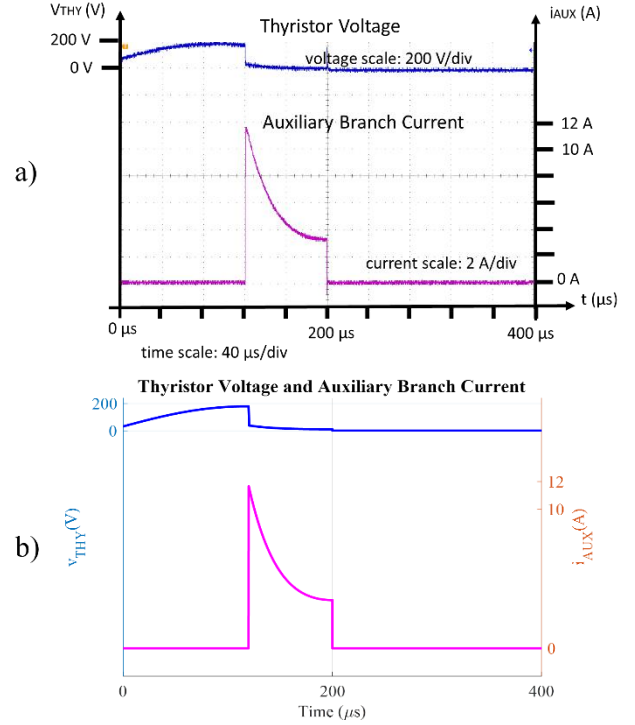


Fig. 14 – Turn-on process with active current diversion: waveforms of the thyristor voltage and of the current spike diverted into the turn-on auxiliary active branch. Experimental (a) and simulation (b) results.

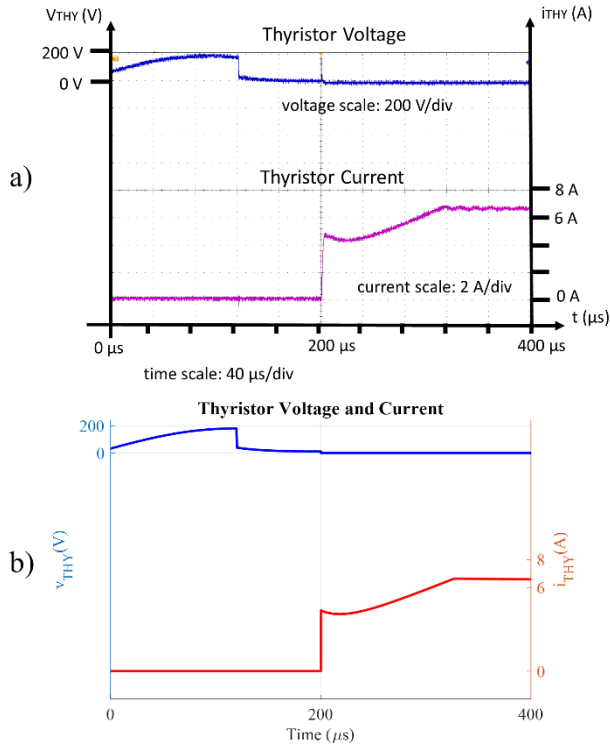


Fig. 13 – Turn-on process with active current diversion: current and voltage waveforms of the thyristor level. Experimental (a) and simulation (b) results.

C. Turn-off Control Method Results

Reduced scale results of the turn-off control method are illustrated in Figs. 15-17: the experimental ones on top (a) and the simulated ones at the bottom (b). Fig. 15 shows voltage and current waveforms of the turn-off process without any active voltage sharing, with $C_d = 100$ nF and $R_d = 50$ Ω . Fig. 16-17 illustrate the voltage and current waveshapes during the turn-off process with active balancing control of the auxiliary circuit. Fig. 16 shows how the voltage waveforms become more uniform once the active control is employed, with $R_{AUX,OFF} = 100$ Ω , to obtain the best compromise between the dv/dt rate and the balancing speed straight after the balancing process. Fig. 17 depicts the current spike diverted into the auxiliary branch, connected in parallel to the faster device.

The results show that the turn-off active circuit succeeds in keeping the series thyristors balanced straight after the turn-off transient. This enhancement is expected to reduce the size of the damping capacitances actually employed in thyristor valves and to decrease the number of valve levels needed in the overall architecture of HVDC converters, also in case of thyristors with significant tolerances on the reverse recovery charge values.

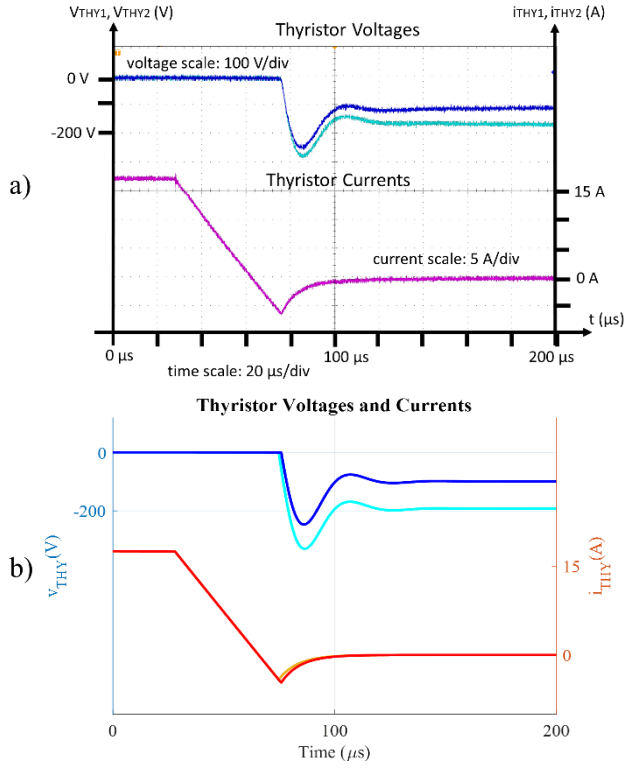


Fig. 15 – Turn-off process with no active control: current and voltage waveforms of the two series thyristors. Experimental (a) and simulation (b) results.

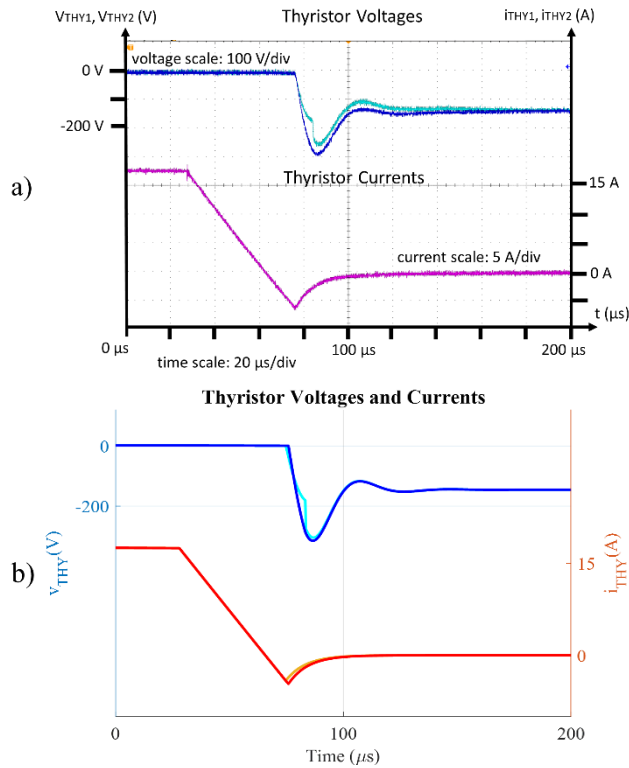


Fig. 16 – Turn-off process with active balancing control: current and voltage waveforms of the two series thyristors. Experimental (a) and simulation (b) results.

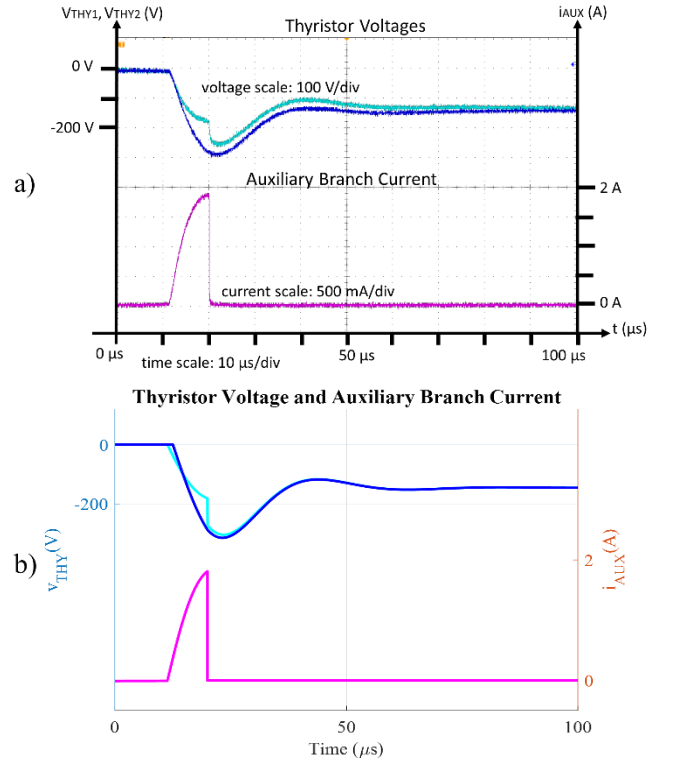


Fig. 17 – Turn-off process with active balancing control: waveforms of the thyristors' voltages, and current diverted into the turn-off auxiliary active branch. Experimental (a) and simulation (b) results.

V. CONCLUSIONS

The research work presented in this paper investigated the development of a smart thyristor valve for HVDC transmission. This architecture is expected to contribute to the reduction of the volume and weight of the existing auxiliary circuits, through the employment of active, instead of passive solutions. Such a reduction aims for a cost reduction of the overall valve and, thanks to a lower weight, also to a cost reduction of the mechanical structure needed to sustain the valve from the roof, for seismic protection.

The turn-on active control method diverts the current spike from the stray capacitance into the auxiliary branch during the initial part of the turn-on transient, while the turn-off active control method connects the auxiliary resistances in parallel to each thyristor level for proper time intervals during the turn-off transient, providing uniform voltage sharing.

Simulations and experiments have been conducted on a reduced scale prototype to validate the proposed actively controlled solutions. The good match obtained for the two active configurations validates the ideas contained in the two reference patents [21] and [22], that can be considered alternative solutions for the improvement of actual thyristor valves.

The expected advantages for a full scale valve are a much smaller saturating di/dt inductor [21] and a reduction between 70% and 90% of the required damping capacitance C_d and resistor R_d [22]. The presented analysis and experimental tests

represent a proof of concept of the use of active auxiliary circuits to partially replace passive ones, from a qualitative point of view. Although the assessment of the actual volume reduction would require data support, the advantage of the proposed solution mentioned in [21] - [22] lays in the reduction of bulky valve components (namely, the saturating inductor, damping capacitance, and damping resistor) whose qualitative encumbrance can be appreciated from Fig. 3. The layout of an H400 valve module, as in Fig. 3, is illustrated in [24] - [25]. It is also worth to highlight that the increase of system components may lead to a higher probability of faults. The overall reliability of the valve system, which is out of the scope of this paper, will require an in-depth analysis of the fault probability of each device and the investigation of possible post-fault strategies.

This research activity aims to contribute to the validation of an innovative solution for the development of high voltage thyristor valves. The proposed analyses provide the justification for the future design of a high voltage setup with a full-scale prototype. This realization will verify the effective cost, volume, and weight reduction of the proposed valve architecture compared to the ones available at current state of the art.

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REFERENCES

- [1] M. L. Woodhouse, "Voltage and Current Stresses on HVDC Valves," *IEEE Trans. Power Deliv.*, vol. 2, no. 1, pp. 199–206, 1987.
- [2] G. Pan, F. Chun-en, Z. Nanxun, L. Wei, and R. Xiao, "Research of grading for series-connected thyristor valves of solid-state transfer switch," in *2017 4th International Conference on Electric Power Equipment - Switching Technology (ICEPE-ST)*, 2017, pp. 444–447.
- [3] S. Xiao, J. Cao, and M. Donoghue, "Stray capacitance and compensation for the converter valves for ultra-high voltage HVDC application," in *2010 International Conference on Power System Technology*, 2010, pp. 1–7.
- [4] C. Liu, Y. Gou, Z. Yang, H. Yan, F. Zhuo, and F. Wang, "Research on Overvoltage Distribution of HVDC Converter Valve and Influence of Parasitic Capacitance in special environment," in *2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2019, pp. 178–182.
- [5] A. Jedidi, H. Garra, H. Morel, and K. Besbes, "A Novel Approach to Extract the Thyristor Design Parameters for Designing of Power Electronic Systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2174–2183, 2015.
- [6] R. Gou, "Research on 1100-kV/5500-A Ultra-High Voltage Thyristor Valve Key Technology and Its Application," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10524–10533, 2019.
- [7] Yingjie Tang, Zheng Xu, Huangqing Xiao, Bo Yue, Xuan Li, "Commutation overshoots based on a novel model for series thyristors during the turn-off process," *High Volt.*, vol. 5, no. 5, pp. 501–510, 2020.
- [8] Z. Dongye, L. Qi, X. Cui, P. Qiu, and F. Lu, "A New Approach to Model Reverse Recovery Process of a Thyristor for HVdc Circuit Breaker Testing," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1591–1601, 2021.
- [9] Yingjie Tang, Zheren Zhang, Zheng Xu, "Analysis and Design of Damping Circuit Parameters for LCC Valves Based on Broadband Model," *Energies*, vol. 13, p. 1059, 2020.
- [10] L. Qi *et al.*, "Parameter Extraction and Wideband Modeling of +- 1100 kV Converter Valve," *IEEE Trans. Power Deliv.*, vol. 32, no. 3, pp. 1303–1313, 2017.
- [11] H. Ito, A. Iwata, and A. Suzuki, "Novel low loss active voltage clamp circuit for series connection of GCT thyristors," in *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No. 02CH37289)*, 2002, vol. 2, pp. 636–641 vol.2.
- [12] Q. Chen, A. Huang, and S. Bhattacharya, "Analysis of static voltage balance of series connected self-power emitter turn-off thyristors," in *2010 IEEE Energy Conversion Congress and Exposition*, 2010, pp. 4547–4550.
- [13] S. Ji, T. Lu, Z. Zhao, H. Yu, and L. Yuan, "Series-Connected HV-IGBTs Using Active Voltage Balancing Control With Status Feedback Circuit," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4165–4174, 2015.
- [14] K. Shingu and K. Wada, "Digital control based voltage balancing for series connected SiC MOSFETs under switching operations," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 5495–5500.
- [15] J. Chivite-Zabalza, D. R. Trainer, J. C. Nicholls, and C. C. Davidson, "Balancing Algorithm for a Self-Powered High-Voltage Switch Using Series-Connected IGBTs for HVDC Applications," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8481–8490, 2019.
- [16] P. Briff, J. Chivite-Zabalza, J. Nicholls, and K. Vershinin, "Turn-Off Delay Compensation of Series-Connected IGBTs for HVDC Applications," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11294–11298, 2020.
- [17] M. H. Jodeyri and A. Dzus, "Thyristor valve for the 12-pulse converter for the Champa-Kurukshetra HVDC transmission scheme," in *2013 IEEE Innovative Smart Grid Technologies-Asia (ISGT Asia)*, 2013, pp. 1–6.
- [18] K. Zha, X. Wei, and G. Tang, "Research and Development of ± 800 kV/4750A UHVDC Valve," in *2012 Second International Conference on Intelligent System Design and Engineering Application*, 2012, pp. 1466–1469.
- [19] H. Huang, M. Uder, R. Barthelmeß, J. Dorn, "Application of high power thyristors in HVDC and FACTS systems," in *17th Conference of Electric Power Supply Industry (CEPSI)*, 2008, pp. 1–8.
- [20] M. Ashraf, A. Gunatilake, and N. MacLeod, "Development testing of ± 800 kV HVDC thyristor valves," in *2009 44th International Universities Power Engineering Conference (UPEC)*, 2009, pp. 1–5.
- [21] C. C. DAVIDSON, "Semiconductor Switching Circuit," Patent No. WO 2014/198730 A1. Dec. 18 2014.
- [22] C. C. DAVIDSON, "Semiconductor Switching String," Patent No. WO 2014/198734. Dec. 18 2014.
- [23] A. Grid, *HVDC Connecting to the Future*. ALSTOM Grid publisher, 2010.
- [24] M. H. Jodeyri and A. Dzus, "Thyristor valve for the 12-pulse converter for the Champa-Kurukshetra HVDC transmission scheme," 2013 IEEE Innovative Smart Grid Technologies-Asia (ISGT Asia), Bangalore, India, 2013, pp. 1–6.
- [25] Russell Preedy, Leader of Alstom Grid's Valve Design group in Stafford, UK, "Big new thyristor valves meet big new test centre." <https://www.think-grid.org/big-new-thyristor-valves-meet-big-new-test-centre> (accessed February 02 2023).



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