

Article

Seamless Transition Between Continuous and Discontinuous Modes Suitable for Natural-Sampled PWM in Variable-Frequency Two-Level VSI Operations

Davide Ferreli ^{1,2} , Gianluca Fichera ² , Mattia Ricco ¹ , Nicola Matteazzi ² and Riccardo Mandrioli ^{1,*} 

¹ Department of Electrical, Electronic, and Information Engineering, University of Bologna, 40136 Bologna, Italy

² Blue Matter srl, 41051 Castelnovo Rangone, Italy

* Correspondence: r.mandrioli@unibo.it; Tel.: +39-05120-93566

Abstract

In high-speed drive applications, including drone propulsion systems and high-speed spindle drives, switching frequency is often limited by thermal constraints or cost considerations when the adoption of wide-bandgap power devices is not economically justified. Under these conditions, natural-sampled PWM offers significant advantages over regular-sampled PWM, particularly at low switching-to-fundamental frequency ratios, by improving output waveform quality and reducing control-loop delay. This paper proposes an adaptive modulation strategy for two-level three-phase voltage-source inverters, enabling a seamless transition from space-vector PWM (SVPWM) to generalized discontinuous PWM (GDPWM). The proposed approach preserves the number of switching events by synchronizing the discontinuities of the modulation signals with the corresponding carrier peaks, thereby ensuring a consistent switching pattern while exploiting the benefits of discontinuous modulation.

Keywords: inverter; pulse width modulation; variable frequency

1. Introduction

In the field of electric drives, particularly in three-phase voltage source inverters (VSIs) continuous efforts are devoted to reduce ripple and total harmonic distortion (THD) [1]. The growing adoption of high-speed applications, such as drone propulsion systems and high-speed spindle drives, has led to operating conditions in which the fundamental frequency of the output currents can be orders of magnitude higher than in conventional drives [2,3]. Under these conditions, maintaining a sufficiently high modulation frequency ratio becomes increasingly challenging. At low switching-to-fundamental frequency ratios, harmonic distortion, output-voltage errors, and waveform degradation become increasingly significant, motivating dedicated compensation techniques and alternative PWM strategies specifically tailored for low-ratio operation [4–6]. This limitation is particularly relevant when wide bandgap (WBG) devices cannot be adopted because of cost constraints and conventional silicon devices impose thermal limits that prevent further increases in switching frequency [7,8]. In applications characterized by a low modulation frequency ratio, natural-sampled pulse-width modulation (NS-PWM) provides advantages over regular-sampled PWM (RS-PWM) [9]. In particular, it reduces total harmonic distortion and minimizes the delay introduced by the discretization process [10–12]. Conversely, the phase delay and waveform distortion associated with regular-sampled PWM become



Academic Editor: Murilo E. C. Bento

Received: 31 July 2026

Revised: 5 September 2026

Accepted: 7 September 2026

Published: 10 September 2026

Copyright: © 2026 by the authors.

Licensee MDPI, Basel, Switzerland.

This article is an open access article distributed under the terms and conditions of the [Creative Commons Attribution \(CC BY\)](https://creativecommons.org/licenses/by/4.0/) license.

less significant only as the modulation frequency ratio increases [13]. Besides the sampling method, the modulation strategy also plays a key role in the performance of three-phase VSIs, also in terms of THD reduction. Space vector pulse-width modulation (SVPWM) is widely adopted as the industrial standard because of its good harmonic performance and voltage utilization. However, alternative modulation methods are available, including generalized discontinuous pulse-width modulation (GDPWM) [14,15]. By clamping one phase for 120° of the fundamental period, GDPWM reduces the switching activity by approximately one third, resulting in a significant reduction in switching losses. Moreover, above a given modulation index threshold, denoted as m_{th} , GDPWM can achieve lower THD than SVPWM when the switching frequency is increased by a factor of 1.5, while still maintaining lower switching losses depending on the power factor [16,17]. In addition to the sampling and modulation strategies, variable switching frequency (VSF) techniques have been shown to further improve drive performance by reducing current ripple and THD through the adaptation of the switching frequency according to the fundamental frequency during operation [18]. Based on these considerations, some studies have investigated the feasibility of online transitions between modulation strategies, particularly from SVPWM to GDPWM when the modulation index exceeds the threshold m_{th} [19–23]. In RS-PWM, this transition is generally straightforward. Some of these approaches have also been extended to variable switching frequency operation [24]. However, the additional challenges arising from NS-PWM have not been fully addressed. This work contributes to this area by demonstrating the feasibility of a transition from SVPWM to GDPWM under NS-PWM, including operation with variable switching frequency. In addition, dedicated solutions are proposed to prevent the current spikes associated with GDPWM operation, ensuring current continuity during both modulation transitions and intrinsic GDPWM discontinuities. The proposed approach is especially beneficial in applications characterized by a low switching-to-fundamental frequency ratio, where the advantages of natural sampling are more pronounced [25]. Without specific countermeasures, uncontrolled variations in the modulation signal in NS-PWM introduce local discontinuities in the switching pattern, leading to current distortion. Two events are particularly critical and require dedicated solutions: the transition from SVPWM to GDPWM and the intrinsic vertical discontinuities of GDPWM associated with the transition between discontinuous pulse-width modulation max (DPWMAX) and discontinuous pulse-width modulation min (DPWMIN). Different GDPWM schemes can be generated by properly selecting the clamping interval and the alternation pattern between DPWMAX and DPWMIN [26]. Among the most popular GDPWM schemes are DPWM0, DPWM1, DPWM2, and DPWM3. These vertical discontinuities correspond precisely to the transitions between the DPWMAX and DPWMIN operating modes. Without appropriate compensation, both events generate noticeable current spikes at the transition instants. To address these issues, this paper introduces a dedicated homologous peak commutation strategy. The proposed approach ensures that transitions occur only at carrier peaks that coincide with future GDPWM discontinuities. This feature is particularly important when a switching-frequency scaling factor of $d = 1.5$ is adopted, since it prevents the quarter-period desynchronization that would otherwise degrade current quality. The approach is also compatible with variable switching frequency operation, enabled by a dedicated synchronization strategy that preserves the phase relationship among the carrier, the GDPWM trigger signal, and the modulating signals. Several implementation aspects that have not been previously discussed in the literature are identified and compensated. To the best of the authors' knowledge, the proposed homologous peak commutation strategy, capable of preserving current continuity during both modulation transitions and the intrinsic GDPWM discontinuities, is presented here for the first time. This paper presents an extension of the seamless transition concept

from SVPWM to GDPWM to the NS-PWM domain, which is particularly advantageous at low modulation frequency ratios. In particular, the challenges associated with both the transition process and the implementation of GDPWM under NS-PWM operation have been identified. These challenges do not arise in conventional RS-PWM implementations and manifest as duty-cycle errors and current spikes. Such phenomena are analyzed and effectively mitigated through the proposed synchronization strategies. Furthermore, the proposed framework extends the transition concept to variable switching-frequency operation while highlighting the importance of the tuning factor $d = 1.5$ during the transition to GDPWM, owing to its beneficial trade-off between harmonic performance and switching losses. This paper is organized as follows. Section 2 reviews the theoretical background and the main concepts relevant to the proposed approach. Section 3 presents the control strategy and homologous peak commutation, describing the transition mechanism between modulation methods and the measures required to implement discontinuous modulation with NS-PWM while preserving current continuity. Section 4 provides numerical validation through MATLAB/Simulink simulations. Section 5 presents the experimental validation on a scaled test setup. Finally, Section 6 summarizes the main conclusions of the work.

2. Background and Theoretical Framework

The operating principle of a two-level VSI is based on the controlled switching of its inverter legs [27]. Each leg $x \in \{1, 2, 3\}$ is described by the binary switching function g_{xA} , which connects the corresponding output either to the positive dc-link rail V_{dc} or to the negative dc-link rail. The voltages measured between the inverter outputs and the negative dc-link rail, referred to as pole voltages and denoted by v_{1n} , v_{2n} , and v_{3n} , can assume only two discrete levels, namely V_{dc} and 0. For the analysis of three-phase systems, however, it is more convenient to consider the line-to-line voltages

$$\begin{aligned} v_{12} &= v_{1n} - v_{2n}, \\ v_{23} &= v_{2n} - v_{3n}, \\ v_{31} &= v_{3n} - v_{1n}. \end{aligned} \quad (1)$$

and the corresponding phase voltages e_1 , e_2 , and e_3 . For a balanced three-phase load connected in star configuration, the neutral voltage with respect to the negative dc-link rail is given by

$$v_{n0} = -\frac{v_{1n} + v_{2n} + v_{3n}}{3}. \quad (2)$$

The phase voltages can therefore be expressed as

$$\begin{aligned} e_1 &= v_{1n} + v_{n0}, \\ e_2 &= v_{2n} + v_{n0}, \\ e_3 &= v_{3n} + v_{n0}. \end{aligned} \quad (3)$$

A conceptual topology of a three-phase inverter with the presented annotation is in Figure 1.

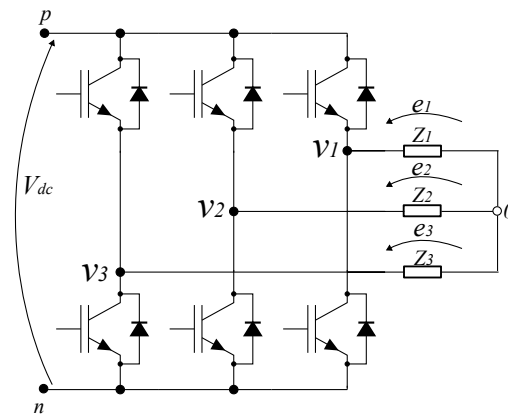


Figure 1. Conventional three-phase two-level voltage source inverter (VSI) topology with a generic load connected in star configuration.

The objective of PWM is to synthesize a continuous low-frequency voltage waveform, called fundamental frequency, by suitably switching between the discrete voltage levels available at the inverter output. Although the instantaneous output voltage is discontinuous, its average value over a switching period T_{sw} can be accurately controlled through the duty cycle. Considering a generic switching period, the duty cycle δ is defined as

$$\delta = \frac{T_{on}}{T_{sw}}, \quad 0 \leq \delta \leq 1, \quad (4)$$

where T_{on} is the conduction interval of the upper switch. The average pole voltage is therefore

$$V_{avg} = \delta V_{dc}. \quad (5)$$

By continuously varying the duty cycle, the inverter generates a waveform containing the desired fundamental component together with high-frequency harmonics. The quality of the reconstructed waveform depends strongly on the switching frequency $f_{sw} = 1/T_{sw}$. In general, higher switching frequencies shift the harmonic content towards higher frequencies, simplifying the filtering action naturally provided by the machine impedance. Besides the switching frequency, the waveform quality is also influenced by the sampling method adopted by the PWM algorithm. Among the most common approaches are RS-PWM and NS-PWM [28,29]. In RS-PWM, the modulating signal is updated once or twice during each switching period and then held constant until the next update. Conversely, in NS-PWM, the switching instants are ideally determined by the actual intersections between the carrier and the modulating signal. As a result, NS-PWM provides a more accurate reconstruction of the reference waveform and introduces less control delay [30]. These advantages become increasingly significant as the ratio between the switching frequency and the fundamental frequency decreases, whereas they become negligible at high modulation frequency ratios [25]. For a three-phase VSI, the modulating signals are defined as

$$\mathbf{u}_x = \begin{cases} u_1 = m \cos(\vartheta) + \gamma \\ u_2 = m \cos\left(\vartheta - \frac{2\pi}{3}\right) + \gamma, \\ u_3 = m \cos\left(\vartheta + \frac{2\pi}{3}\right) + \gamma \end{cases} \quad (6)$$

where m is the modulation index, defined as

$$m = \frac{\sqrt{2}V_{ac}}{V_{dc}}, \quad (7)$$

with V_{ac} denoting the root-mean-square (RMS) value of the phase voltage. In a balanced system, the same modulation index is applied to all three phases. Different modulation strategies can be obtained by properly selecting the common-mode term γ , which determines the resulting PWM strategy, including continuous and discontinuous modulation schemes [31]. Common γ choices are

$$\begin{aligned} \gamma_{SPWM} &= 0 \\ \gamma_{SVPWM} &= -\frac{\max[\mathbf{u}_x] + \min[\mathbf{u}_x]}{2} \\ \gamma_{DPWMAX} &= 1 - \max[\mathbf{u}_x] \\ \gamma_{DPWMIN} &= -1 - \min[\mathbf{u}_x] \\ \gamma_{GDPWM} &= g \gamma_{DPWMAX} + (1 - g) \gamma_{DPWMIN} \end{aligned} \quad (8)$$

The signal g is a trigger signal used to alternate between DPWMAX and DPWMIN, or equivalently, to switch the clamping interval between the upper and lower clamping windows. Different alternation patterns generate different variants of GDPWM; in this paper, DPWM1 is the default choice and terms DPWM1 and GDPWM are from now on considered interchangeable. For the purpose of this work, g must be properly synchronized with the carrier and the modulating signal, and a detailed description will be provided in the next section. SVPWM is the most adopted modulation strategy in industrial applications [32]. The space-vector and carrier-based formulations of SVPWM are mathematically equivalent, the latter being obtained through the injection of a suitable common-mode signal into the sinusoidal modulating references. Although SVPWM is often derived using geometrical considerations [33], the carrier-based implementation provides an equivalent and often more convenient formulation for industrial implementation. This formulation is particularly convenient because it allows SVPWM and GDPWM to be described within a unified framework. A view of SVPWM and DPWM1 modulating signals are presented respectively in Figure 2 and Figure 3.

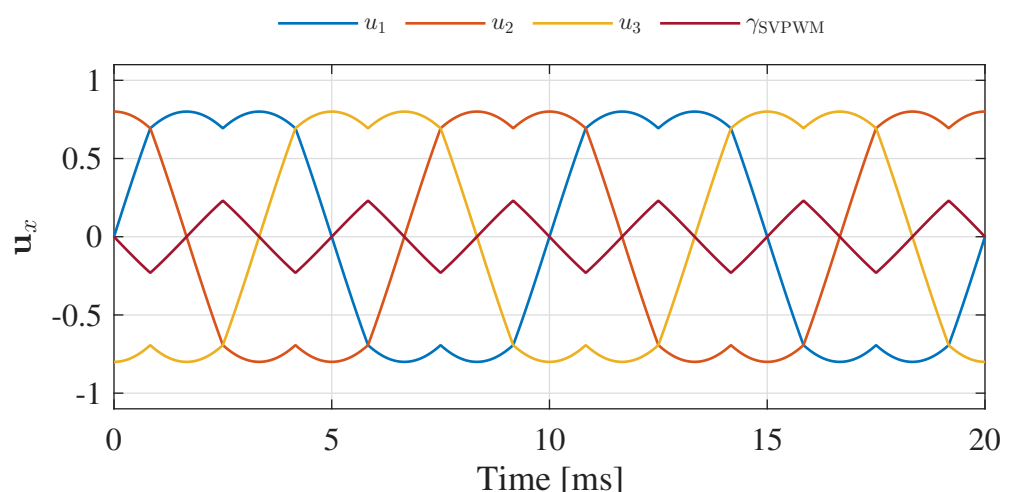


Figure 2. SVPWM modulating signals (u_1 , u_2 , and u_3) and corresponding common-mode injection signal γ_{SVPWM} .

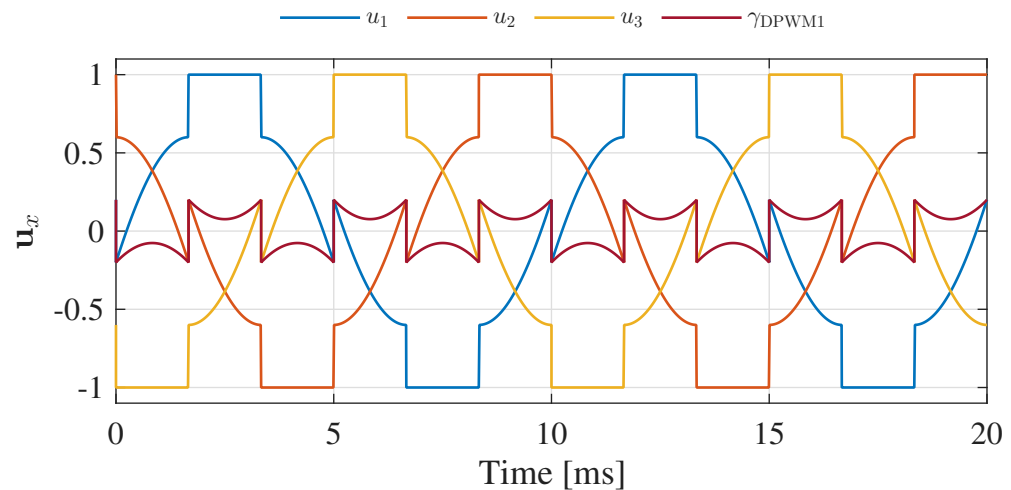


Figure 3. DPWM1 modulating signals (u_1 , u_2 , and u_3) and corresponding common-mode signal γ_{DPWM1} .

SVPWM and GDPWM exhibit different THD performance as a function of the modulation index. Above a modulation-index threshold of approximately $m_{\text{th}} = 0.75$, GDPWM can achieve lower total harmonic distortion while also reducing switching losses due to its clamped intervals [34]. In the generalized formulation, the parameter d acts as a tunable switching-frequency scaling factor that can be adjusted to balance switching losses and harmonic performance when transitioning from SVPWM to GDPWM. Therefore, d can be regarded as an additional degree of freedom that allows the modulation strategy to be tailored according to the design objective, such as minimizing switching losses or reducing current and voltage distortion. This factor modified the f_{sw} . The introduction of this factor is motivated by the intrinsic clamping intervals of GDPWM. Since one inverter leg remains clamped for part of the fundamental period, the switching events count is naturally reduced with respect to SVPWM. Consequently, the switching frequency can be increased through the factor d to partially compensate for the reduced switching activity while preserving comparable switching losses and potentially improving harmonic performance depending on the value. For $d = 1$, the modulation achieves the maximum reduction in switching activity, decreasing switching losses by up to 50% compared to SVPWM. When $d = 1.5$, the total number of switching events remains approximately unchanged, compensating for the 120° clamping interval introduced by GDPWM while improving harmonic performance and still providing a slight reduction in switching losses. For $d = 2$, switching losses become comparable to those of SVPWM, whereas harmonic performance is further improved [31]. Since the primary objective of this study is to reduce the THD without increasing switching losses, the case $d = 1.5$ is of particular interest. As will be shown in the following sections, however, this value requires specific implementation considerations. The THD_r is commonly used to quantify the harmonic content of a signal with respect to its fundamental component and is defined as

$$\text{THD}_r = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_{1,\text{RMS}}} \quad (9)$$

where $V_{1,\text{RMS}}$ is the RMS value of the fundamental component and V_h is the RMS value of the h -th harmonic component. Another factor that can significantly affect waveform quality is the dead-time effect [35]. Since the switches of the same inverter leg must operate in a complementary manner to avoid shoot-through conditions, a short delay, commonly referred to as dead time, is introduced between the turn-off of one device and the turn-on of its complementary switch. Although necessary for safe operation, dead time

introduces voltage errors and current distortion. The voltage error introduced by dead time depends on both the dead-time duration and the switching period. To compensate for this effect, the modulating signal can be expressed as the sum of the original reference and a compensation term

$$u_x^* = u_x + \Delta u_x. \quad (10)$$

The dead-time voltage error depends on the sign of the phase currents and can be expressed as

$$u_{d,x} = \Delta V_d \left\{ -\text{sign}(i_x) + \frac{\text{sign}(i_1) + \text{sign}(i_2) + \text{sign}(i_3)}{3} \right\}, \quad (11)$$

where

$$\Delta V_d = \frac{t_d}{T_{sw}} V_{dc}. \quad (12)$$

In some drive applications, additional improvements in harmonic performance can be achieved by varying the switching frequency during operation. This approach, commonly referred to as VSF, allows the switching frequency to adapt to the operating conditions while maintaining a desired relationship with the fundamental frequency [36]. In this work, among the various methods available for implementing VSF operation, the triangular carrier signal is generated as

$$c = \frac{2}{\pi} \arcsin(\sin \theta_c), \quad (13)$$

where θ_c denotes the carrier phase angle, which will be properly defined in the next section. The arcsine operator is required to transform the monotonically increasing phase angle θ_c into a normalized triangular waveform suitable for carrier-based PWM generation. Based on the concepts reviewed above, the objective of this work is to investigate the feasibility of a transition from SVPWM to GDPWM driven by the modulation index under variable switching frequency operation and NS-PWM. The analysis revealed that a direct transition from SVPWM to GDPWM produces significant current spikes unless appropriate synchronization strategies are adopted. In particular, without the synchronization mechanisms presented in the next section, the abrupt change in the modulation strategy introduces duty-cycle errors that lead to local voltage discontinuities and current distortions at the transition instant. Furthermore, it was observed that the introduction of the frequency scaling factor $d = 1.5$ at the transition instant creates additional challenges. Without a dedicated implementation, referred to in this work as homologous peak commutation, multiple current spikes appear during the subsequent GDPWM operation, potentially degrading the resulting THD. The nature of the duty-cycle error is visible in Figure 4 in which the three pole voltages obtained in the synchronized case (red) are compared with those obtained in the asynchronous case (green). The lower plots show the corresponding modulating and carrier signals. For conceptual clarity, the DPWM1 discontinuities have been forced to occur at the middle of a carrier half-period in the asynchronous case by introducing an initial carrier phase shift equal to half a carrier semi-period. This configuration was intentionally adopted to provide a clearer visualization of the duty-cycle error mechanism. An analogous condition occurs when the synchronization between the GDPWM discontinuities and the carrier peaks is not properly maintained. In particular, as rigorously demonstrated in the next section, the introduction of the scaling factor $d = 1.5$ may lead to a half-carrier semi-period displacement between the discontinuities and the carrier peaks if appropriate synchronization measures are not implemented. In contrast, the discontinuities are aligned with a carrier peak in the synchronized case. Focusing on the carrier interval surrounding the discontinuity, namely the switching period delimited by the carrier peaks immediately before and after the discontinuity, duty-cycle errors can be clearly observed. In particular, the pole voltage v_{1n} exhibits rapid switching events in the asynchronous case due to

multiple intersections between the modulating signal and the carrier at the discontinuity instant. These events are not present in the synchronized case. The duty-cycle error is even more evident in the pole voltage v_{3n} , where an undesired voltage pulse is generated, resulting in a non-zero duty cycle during the switching period containing the discontinuity. In contrast, in the synchronized case the duty cycle during the same switching period is equal to zero. These differences illustrate how an unsynchronized DPWM1 discontinuity modifies the generated duty cycle and introduces voltage errors. It is worth noting that such duty-cycle errors are localized phenomena and occur only in correspondence with the GDPWM discontinuities, namely during the transitions between DPWMAX and DPWMIN. Outside these transition instants, the synchronized and asynchronous implementations generate identical duty cycles.

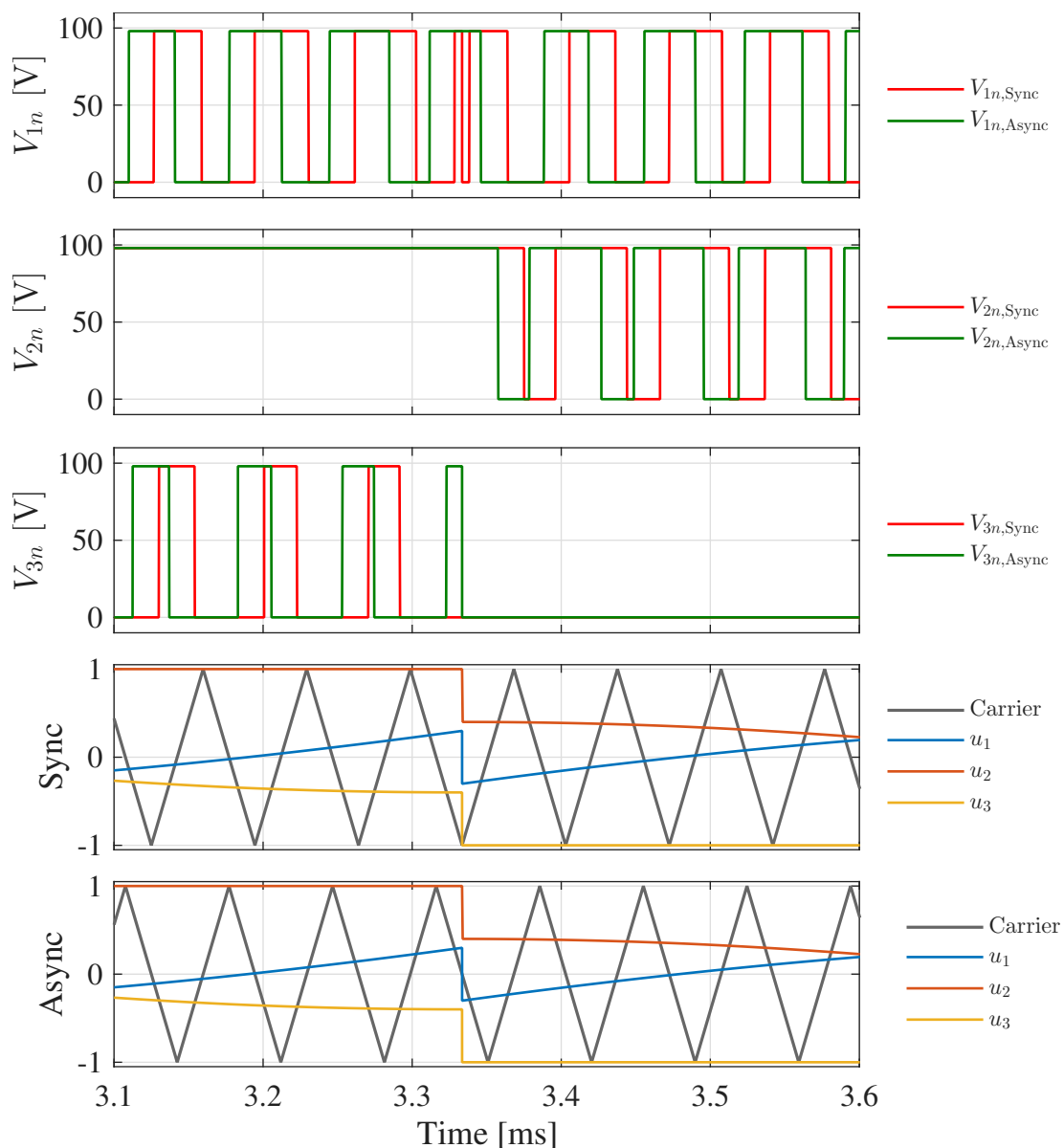


Figure 4. Comparison between synchronized and asynchronous operation. The (**upper plots**) show the pole voltages v_{1n} , v_{2n} , and v_{3n} , while the (**lower plots**) report the corresponding modulating signals. In the synchronized case, the DPWM1 discontinuities are aligned with the carrier peaks. In the asynchronous case, the discontinuities occur at the middle of a carrier half-period, producing a duty-cycle error visible on v_{3n} .

The following section presents the proposed synchronization methods designed to preserve current continuity and prevent duty-cycle errors by aligning the modulation discontinuities with the carrier peaks during both the SVPWM-to-GDPWM transition and the intrinsic GDPWM discontinuities. Furthermore, when a frequency scaling factor of $d = 1.5$ is adopted, an additional measure, referred to as homologous peak commutation, must be implemented to preserve the synchronization between the carrier extrema and the subsequent GDPWM discontinuities. The proposed approach extends the applicability of GDPWM to the NS-PWM domain under variable switching-frequency operation while maintaining current continuity and avoiding synchronization-related distortions.

3. Proposed Synchronization and Transition Strategy

The primary challenge associated with transitions between different modulation strategies is the preservation of current continuity. A direct transition performed when the modulation index exceeds the threshold m_{th} in NS-PWM generally results in current spikes and waveform distortion. By forcing the commutation to occur only at the top or bottom peaks of the triangular carrier, the modulation change takes place when the carrier comparison process is effectively reset. Under this condition, each modulating signal interacts only once with a given carrier ramp, avoiding multiple intersections with the same ascending or descending segment. When the transition is performed at a carrier peak, the duty cycle of the following half-period is entirely computed according to the new modulation strategy. As a result, two different modulation methods are never mixed within the same pulse-generation interval, ensuring a smooth transition from the average-voltage perspective. In the proposed framework, to preserve synchronization between the modulating signals and the carrier, the fundamental frequency f is treated as the reference quantity from which all the remaining signals are derived, specifically the trigger and the carrier. The implementation of GDPWM under VSF operation requires particular attention. Since GDPWM alternates between DPWMAX and DPWMIN, the trigger signal g must operate at three times the fundamental frequency in order to maintain the correct positioning of the clamped intervals. Therefore, the trigger signal can be generated as

$$g = \text{sign} \left[\cos \left(\theta_{g0} + 6\pi \int_0^t f(\tau) d\tau \right) \right]. \quad (14)$$

The parameter θ_{g0} represents the phase shift of the trigger signal and can be used to position the clamped intervals according to the operating conditions. Accordingly, the carrier phase angle is defined as

$$\theta_c = \theta_{c0} + 2\pi \int_0^t 6kf(\tau) d\tau. \quad (15)$$

To guarantee synchronization between the carrier and the GDPWM discontinuities, the initial carrier phase must satisfy

$$\theta_{c0} = \theta_{t0} \pm k\pi, \quad k \in \mathbb{Z}. \quad (16)$$

This framework enables both SVPWM and GDPWM operation under variable fundamental and switching frequency conditions while preserving synchronization among the carrier, the trigger signal g , and the modulating signals. The proposed transition involves not only a change in the modulation strategy but also a simultaneous adjustment of the switching frequency. To maintain comparable switching losses while improving current quality during GDPWM operation, a frequency scaling factor d is introduced. In the SVPWM region,

$d = 1$, whereas in the GDPWM region $d = 1.5$ is adopted. Consequently, the switching frequency becomes

$$f_{sw} = 6kfd. \quad (17)$$

Different values of d lead to different trade-offs between switching losses and harmonic performance. During the transition from SVPWM to DPWM1, the value $d = 1.5$ was selected because it compensates for the reduction in effective switching activity introduced by the intrinsic 120° clamping interval, thereby improving THD while maintaining approximately the same effective switching frequency as in SVPWM. However, the introduction of a non-integer scaling factor such as $d = 1.5$ during the transition introduces an additional synchronization constraint. In a variable switching frequency regime, the carrier and modulation signals must preserve a precise phase relationship. The discontinuities inherent to GDPWM, corresponding to the transitions between DPWMAX and DPWMIN, are intentionally aligned with specific carrier peaks. If the transition from $d = 1$ to $d = 1.5$ occurs at an unsuitable carrier peak, the subsequent carrier periods become shorter and the GDPWM discontinuities may no longer coincide with the carrier extrema. This loss of synchronization reintroduces the current spikes that carrier-synchronized GDPWM is intended to eliminate. To preserve this synchronization during the transition, the proposed Homologous Peak Commutation strategy is introduced. The conceptual implementation is visible in Figure 5.

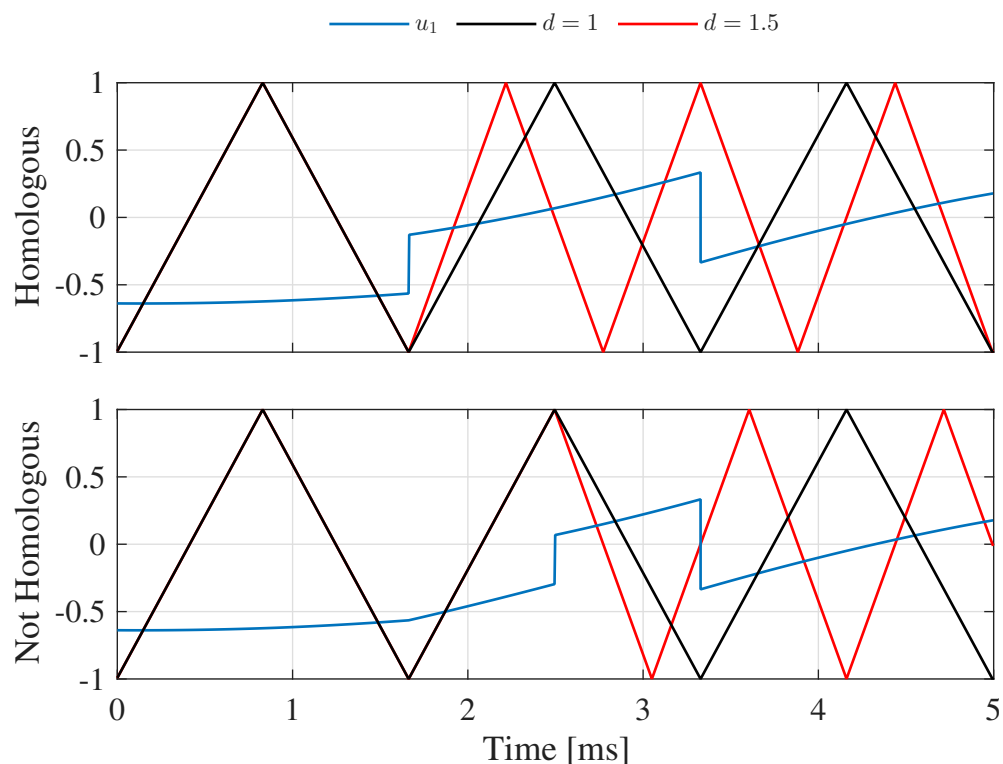


Figure 5. Homologous Peak Commutation principle. **(Top):** transition performed on a carrier peak homologous to the future GDPWM discontinuities, preserving synchronization after the change from $d = 1$ to $d = 1.5$. **(Bottom):** non-homologous transition producing a quarter-period desynchronization between the carrier and the GDPWM discontinuities.

According to this approach, the commutation cannot occur at an arbitrary carrier peak but must take place at a carrier peak belonging to the same “family” of peaks used by the future GDPWM discontinuities. The relationship is determined by the initial phase displacement between the carrier and the trigger signal. Depending on the selected phase

configuration, the six discontinuities occurring during one fundamental period are synchronized either with the carrier top peaks or with the carrier bottom peaks.

- If the GDPWM discontinuities are synchronized with the carrier top peaks, for example with

$$\theta_0 = \frac{\pi}{6}, \quad \theta_{g0} = \frac{\pi}{2}, \quad \theta_{c0} = \frac{\pi}{2},$$

the transition from SVPWM to GDPWM must occur at a top peak.

- Conversely, if the GDPWM discontinuities are synchronized with the carrier bottom peaks, for example with

$$\theta_0 = \frac{\pi}{6}, \quad \theta_{g0} = \frac{\pi}{2}, \quad \theta_{c0} = \frac{3\pi}{2},$$

the transition must occur at a bottom peak.

Let t_c denote the time interval between the transition instant and the first subsequent GDPWM discontinuity. Since both events are synchronized with carrier extrema, t_c can be expressed as

$$t_c = c \frac{T_{sw}}{2}, \quad c \in \mathbb{N}, \quad (18)$$

where c is the number of carrier half-periods separating the two events. After the frequency scaling factor is applied, the new carrier period becomes

$$T_{sw,d} = \frac{T_{sw}}{d}. \quad (19)$$

Therefore,

$$t_c = c d \frac{T_{sw,d}}{2}. \quad (20)$$

For any integer value of d , synchronization is naturally preserved because an integer number of carrier half-periods still fits within t_c . However, for the specific case $d = 1.5$,

$$t_c = c \frac{T_{sw,d}}{2} \left(1 + \frac{1}{2}\right) = c \left(\frac{T_{sw,d}}{2} + \frac{T_{sw,d}}{4}\right). \quad (21)$$

For odd values of c , the additional term introduces a phase displacement equal to one fourth of the carrier period. This causes the GDPWM discontinuities to lose synchronization with the carrier peak. To avoid this condition, c must be constrained to even values. In practical terms, this requirement is equivalent to performing the transition only on carrier peaks homologous to those used by the GDPWM discontinuities. Under this condition,

$$t_c = c T_{sw}, \quad (22)$$

and the frequency increase associated with $d = 1.5$ produces only a half-period shift, which does not compromise synchronization. Consequently, the carrier extrema and GDPWM discontinuities remain aligned throughout the transition process. The consequences of synchronization loss can be understood by examining the interaction between the GDPWM discontinuities and the carrier signal. When the transitions between DPWMAX and DPWMIN do not occur at a carrier peak, a condition that may arise after the introduction of the scaling factor $d = 1.5$ without the proposed homologous peak commutation strategy, the discontinuity is shifted approximately to the middle of a carrier half-period. Under this condition, the modulating signal changes while the carrier comparison process is still ongoing rather than at a carrier reset point. Consequently, the pulse width generated during that switching period does not correspond to either the pre-transition or the post-transition reference. The resulting average pole voltage is therefore affected by an error, producing a

local discontinuity in the phase voltages and, consequently, phase-current spikes. Repeated occurrences of this phenomenon increase the harmonic content of the current and degrade the overall waveform quality.

4. Numerical Validation and Performance Evaluation

To validate the proposed adaptive modulation strategy and the synchronization mechanisms presented in the previous section, a comprehensive MATLAB/Simulink model was developed. The model consists of a three-phase two-level VSI supplying a balanced RL-RC load, representing a simplified equivalent of motor stator windings. The simulation setup was designed to reproduce realistic operating conditions and provide a suitable framework for assessing the phenomena discussed throughout this work. All the analytical formulations introduced in the proposed control strategy, including the synchronization constraints and the homologous peak commutation mechanism, were directly implemented in the simulation model. Unless otherwise specified, the fundamental frequency was set to $f \geq 300$ Hz, consistently with the operating conditions of high-speed drive applications. The only exception is the test investigating the intrinsic GDPWM discontinuities, where a fundamental frequency of 50 Hz and a frequency ratio $k = 8$ are intentionally adopted to facilitate the observation of the current spikes generated when the proposed homologous peak commutation strategy is not applied, therefore, to ensure consistency, the simulations were also carried out using those same parameter values. The dc-link voltage was set to $V_{dc} = 98$ V. The load parameters were selected to emulate the experimental setup adopted in this work. Furthermore, the ratio between switching and fundamental frequency was intentionally kept low by selecting $k = 4$. This choice is consistent with the application scenario considered in this paper, where the reduced switching-to-fundamental frequency ratio makes the use of NS-PWM particularly advantageous and highlights the synchronization issues addressed by the proposed approach. A fixed simulation time step of $T_s = 10^{-8}$ s was adopted. The main simulation parameters are summarized in Table 1.

Table 1. Simulation parameters.

Parameter	Symbol	Value	Unit
DC-link voltage	V_{dc}	98	V
RL circuit	R	727	m Ω
	L	1.73	mH
RC circuit	R_0	6.6	Ω
	C_0	45	μ F
Frequency ratio	k	4	–

The main contribution of this work concerns the dynamic transition between SVPWM and GDPWM according to the modulation index threshold m_{th} . The first set of simulations was therefore aimed at evaluating the effect of the transition timing. In NS-PWM, if the transition is triggered immediately when the modulation index crosses the threshold, without waiting for a carrier peak, the inverter undergoes an instantaneous change in modulation logic. This condition generates a significant current spike at the transition instant due to the abrupt modification of the duty-cycle calculation, this is visible in Figure 6, which alters the average voltage applied during that switching interval. By introducing carrier-synchronized commutation, the transition is delayed until the next carrier peak, preventing it from occurring at an arbitrary point within the carrier period and forcing it to take place only at carrier peaks. To better highlight the effect of the synchronization mechanism, the analysis was performed for $d = 1$. Under these conditions, the transition occurs seamlessly and the phase current remains continuous without observable spikes.

This result confirms that carrier-synchronized commutation effectively removes the current discontinuity associated with a direct modulation change.

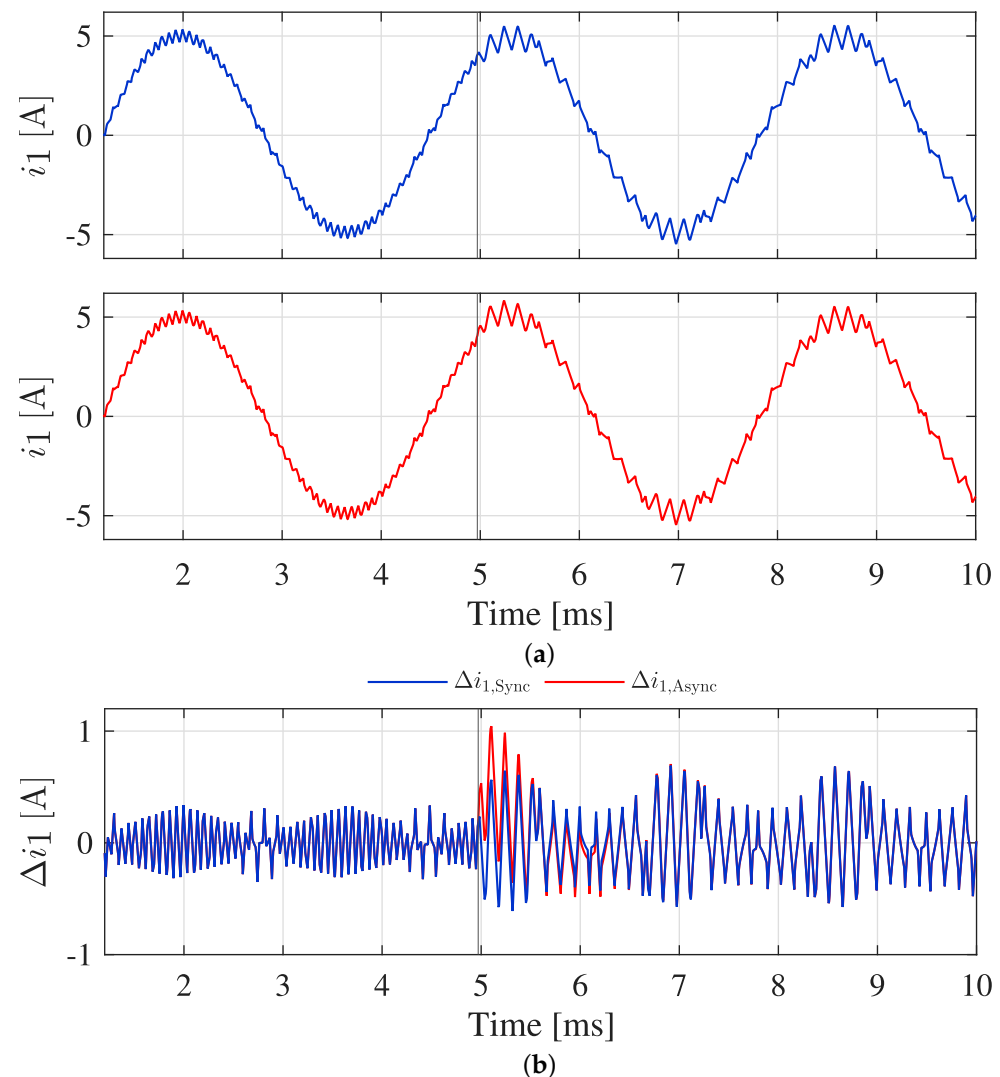


Figure 6. Comparison of (a) phase-current i_1 and (b) phase-current-ripple Δi_1 waveforms obtained with synchronous (blue) and asynchronous (red) transitions from SVPWM to DPWM1. In the synchronized case, the transition is delayed until a carrier peak after the modulation index exceeds the threshold $m_{th} = 0.72$. In the asynchronous case, the transition is performed immediately when the threshold is crossed, without carrier synchronization. The proposed synchronization strategy significantly reduces the current spike generated at the transition instant. The transition instant is highlighted by the vertical light-gray line.

As a consequence of the proposed transition strategy, the THD performance of the combined modulation scheme was re-evaluated over the entire modulation-index range. The results, shown in Figure 7, confirm that the transition mechanism allows the converter to preserve the best available harmonic performance of each modulation strategy, enabling the lowest THD operation across the complete operating range. For modulation indices below the transition threshold, a lower THD could be theoretically achieved by increasing the switching frequency in SVPWM. However, this improvement would be obtained at the expense of higher switching losses. The factor $d = 1.5$ is of particular interest during the transition to DPWM1 because it compensates for the reduction in switching activity introduced by the intrinsic 120° clamping interval, thereby improving THD while preserving approximately the same effective switching frequency as in SVPWM operation. However,

as demonstrated in this work, the adoption of this scaling factor also introduces additional synchronization challenges. In particular, if the transition is not properly synchronized, a loss of alignment between the GDPWM discontinuities and the carrier peaks occurs. The proposed homologous peak commutation strategy was specifically developed to overcome this issue and preserve current continuity while retaining the benefits associated with $d = 1.5$.

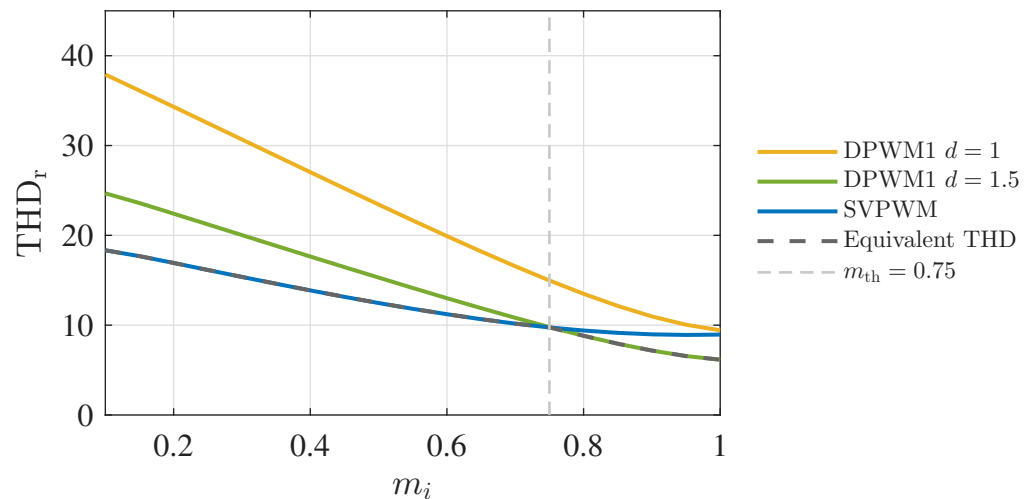


Figure 7. THD as a function of the modulation index m_i for SVPWM and DPWM. The results show that, above a given modulation threshold, transitioning from SVPWM to DPWM with a frequency scaling factor $d = 1.5$ provides lower THD.

Following the transition from SVPWM to GDPWM, a second aspect must be considered, namely the current spikes associated with the intrinsic discontinuities of GDPWM when the Homologous Peak Commutation strategy is not applied. As discussed in the previous section, a loss of synchronization causes the GDPWM discontinuities to occur at the middle of a carrier half-period rather than at a carrier peak. Under this condition, duty-cycle errors are introduced, producing local discontinuities in the phase voltages and consequently phase current spikes. A specific focus of the numerical analysis was the introduction of the frequency scaling factor $d = 1.5$ during GDPWM operation. This test was conducted to verify the necessity of the proposed Homologous Peak Commutation strategy. The results confirm the theoretical analysis. When the transition is performed on a non-homologous carrier peak while simultaneously changing from $d = 1$ to $d = 1.5$, a phase desynchronization is introduced. The resulting offset corresponds to one quarter of the carrier period, causing all subsequent GDPWM discontinuities to lose alignment with the carrier. As a consequence, periodic voltage and current distortions appear throughout the discontinuous modulation interval. These distortions manifest as current spikes, clearly visible in Figure 8, occurring at specific GDPWM discontinuities, precisely where the duty-cycle errors are generated. Such events increase the harmonic content of the current and can negatively affect both THD and converter losses.

As a consequence of the proposed Homologous Peak Commutation strategy, current continuity is preserved and the harmonic performance is improved, as shown in Figure 9. The results indicate that the benefit provided by the proposed synchronization method becomes increasingly significant as the switching-to-fundamental frequency ratio decreases, namely for lower values of m_f . Under these operating conditions, the duty-cycle errors generated by asynchronous GDPWM discontinuities have a greater impact on the output waveform, making the proposed synchronization strategy particularly effective. It is also worth noting that the THD improvement exhibits an approximately linear dependence on the modulation index m_i over the considered operating range.

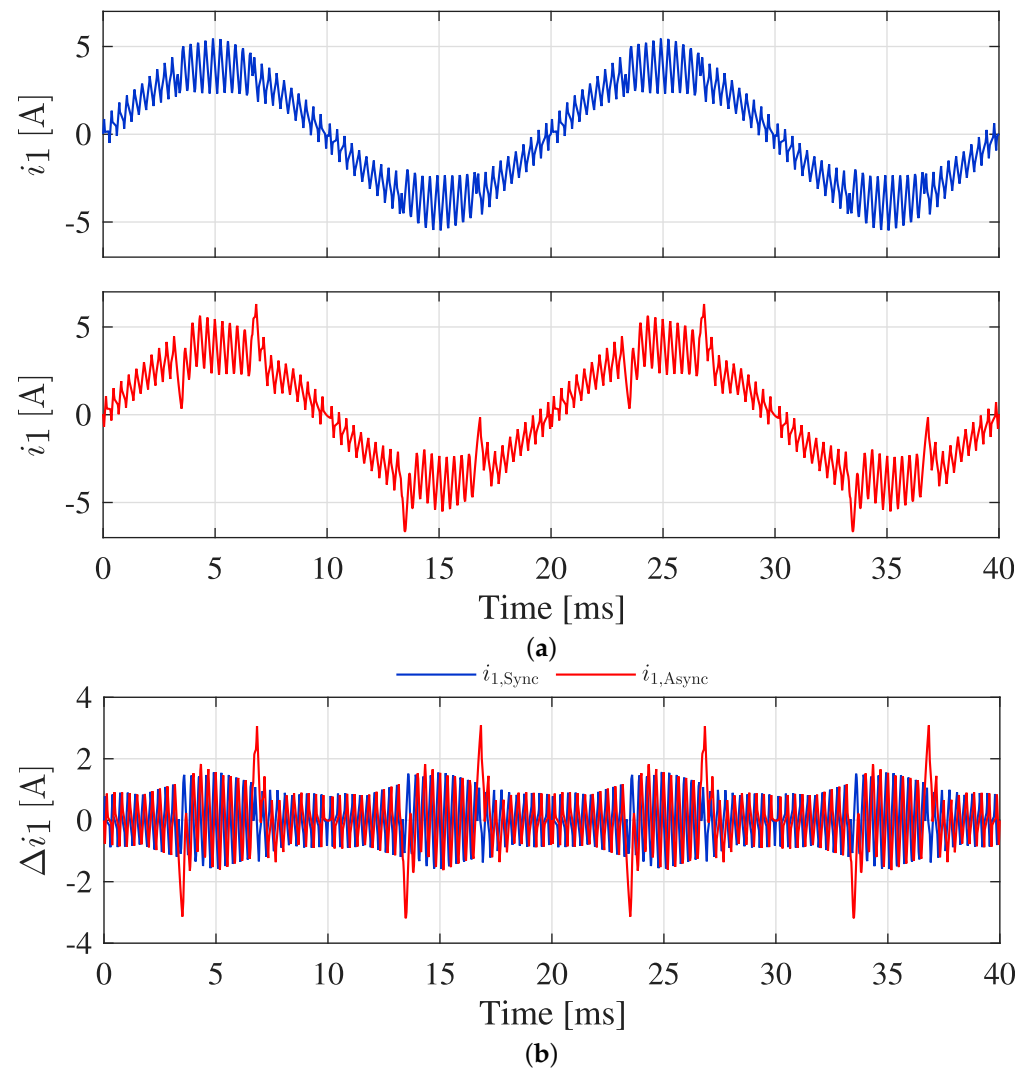


Figure 8. Comparison of (a) phase-current i_1 and (b) phase-current-ripple Δi_1 waveforms obtained with synchronous (blue) and asynchronous (red) GDPWM operations. In the asynchronous case, clearly visible current spikes appear at the DPWM1 discontinuities due to the loss of synchronization between the discontinuities and the carrier peaks. The lower plot compares the normalized current ripple, highlighting the additional distortion introduced by the asynchronous implementation.

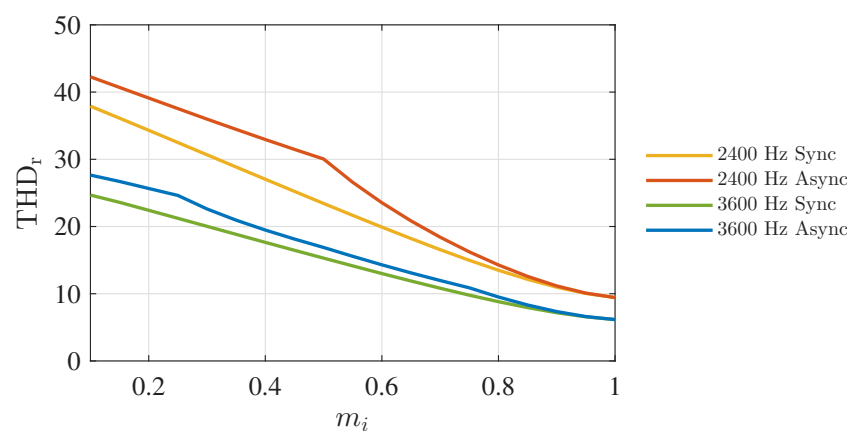


Figure 9. THD as a function of the modulation index m_i for different switching frequencies under synchronized and asynchronous operation. The asynchronous implementation has higher THD due to the current spikes generated at the DPWM1 discontinuities. The impact of these spikes becomes more pronounced at lower switching frequencies, where the resulting duty-cycle errors contribute more significantly to the overall harmonic distortion.

Finally, the robustness of the complete control architecture was assessed under fully dynamic operating conditions by simultaneously varying the modulation index and the fundamental frequency. During the simulation, shown in Figure 10, the fundamental frequency was increased from 280 Hz to 380 Hz, while the modulation index was ramped from 0.5 to 0.95. Under these conditions, the controller successfully managed the following actions:

- Continuous adaptation of the switching frequency f_{sw} as a function of the fundamental frequency f .
- Dynamic transitions between SVPWM and GDPWM when the modulation index crossed the threshold m_{th} in both directions.
- Instantaneous scaling of the switching-frequency ratio through the factor d , resulting in $k \cdot d = 6$ during GDPWM operation. Although the carrier frequency is increased through the factor $d = 1.5$ when DPWM1 is implemented, the effective switching frequency remains unchanged due to the intrinsic 120° clamping interval of DPWM1. As a consequence, this increase does not result in a corresponding increase in switching losses [31].

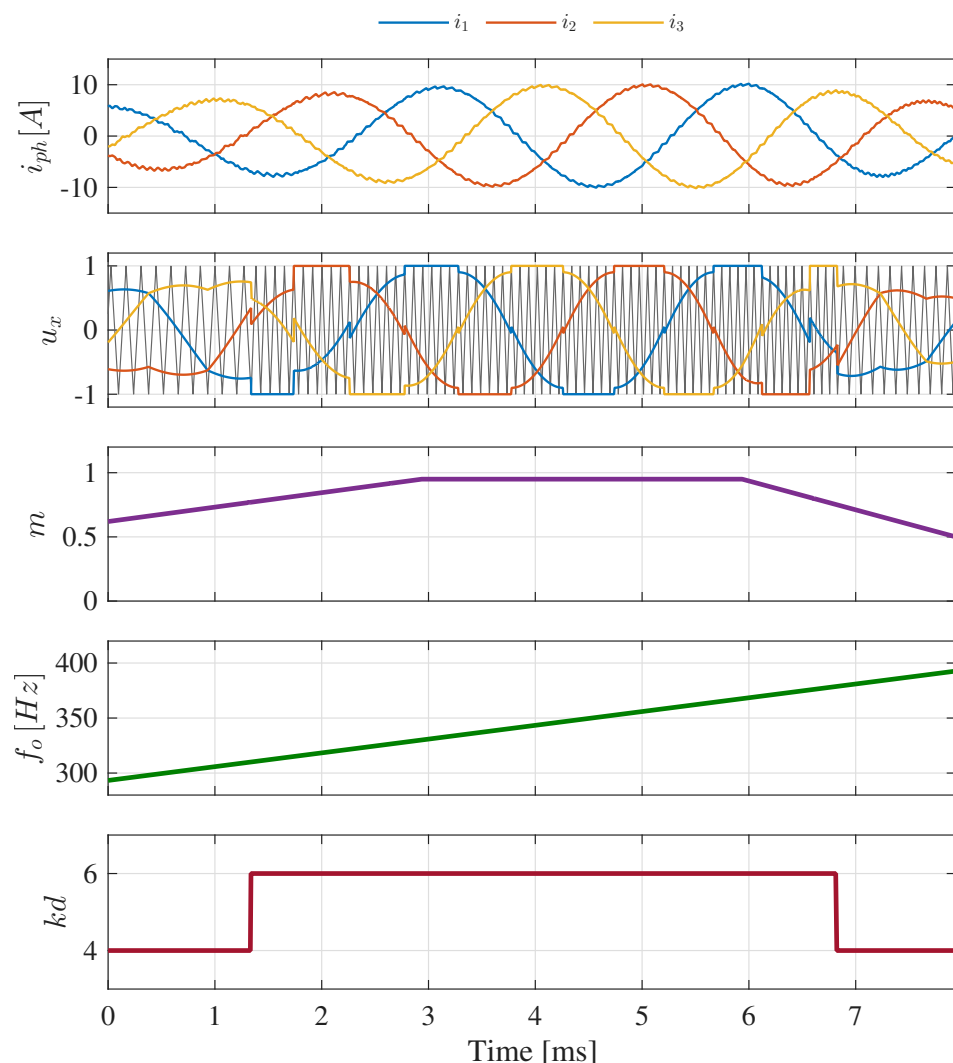
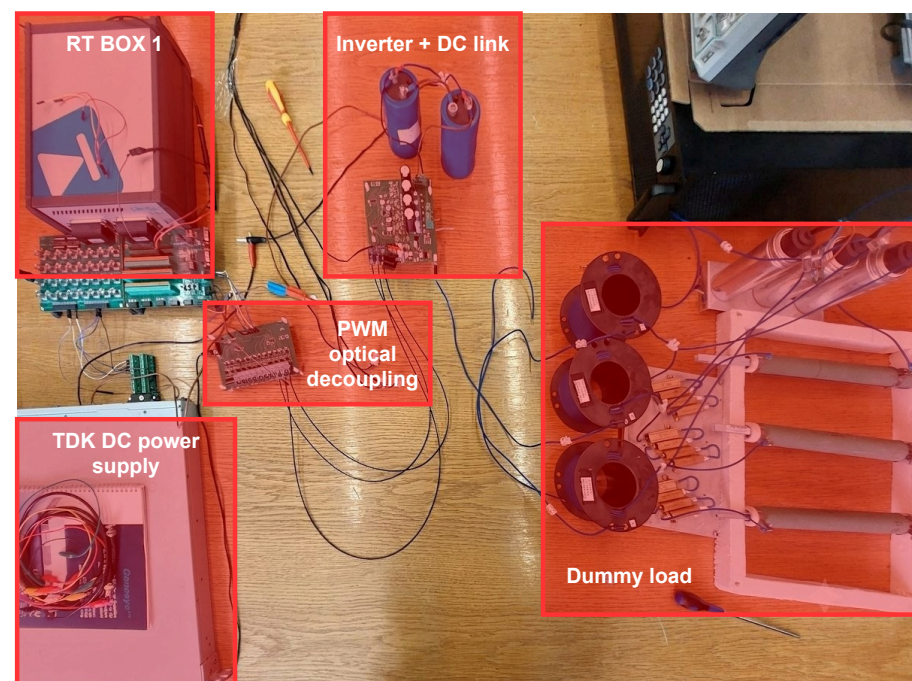


Figure 10. Transition from SVPWM to GDPWM in a variable switching-frequency domain with a simultaneous variation in the modulation index, using $m_{th} = 0.85$, $k = 4$, and $d = 1.5$. From (top) to (bottom): (1) phase currents during the full dynamic transition, (2) modulating signals and carrier waveform, (3) modulation index trajectory, (4) fundamental frequency profile, and (5) time evolution of the kd product.

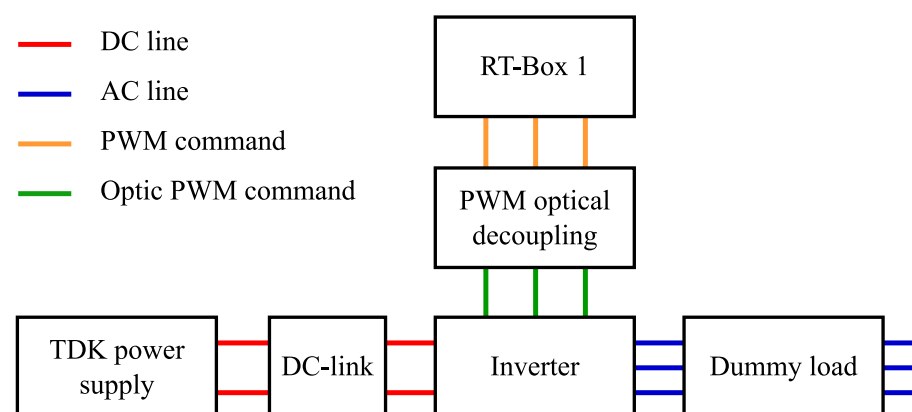
The simulation results demonstrate that the phase currents remain balanced and free of transition-related spikes throughout the entire operating range. Furthermore, synchronization among the carrier, the modulating signals, and the GDPWM discontinuities is preserved under all tested conditions, confirming the effectiveness of the proposed control strategy, even in high-speed applications characterized by a low switching-to-fundamental frequency ratio.

5. Experimental Validation of the Proposed Strategy

In this section, experimental results are presented to validate the analytical considerations and the proposed modulation strategies under real operating conditions. Experimental validation is essential to assess the real-time feasibility of the proposed control algorithms and their interaction with physical power electronic hardware. For this purpose, the complete control scheme was implemented within the PLECS environment. The experimental platform is based on a PLECS RT Box [37], which operates as a real-time controller. The setup is visible in Figure 11.



(a)



(b)

Figure 11. (a) Bird's-eye view of the experimental setup. (b) Block schematic of the experimental setup.

The experimental setup consists of a three-phase two-level VSI based on silicon IGBT devices supplied by an adjustable dc power supply (GEN100-33, 100 V, 33 A, TDK-Lambda Corporation, Tokyo, Japan [38]). The inverter is driven by the PWM signals generated by the RT Box. A significant characteristic of the adopted inverter is the presence of a hardware dead time equal to $t_d = 4 \mu\text{s}$. This value is not a design choice of the proposed control strategy but rather a hardware-intrinsic characteristic of the adopted laboratory inverter. Although required to prevent shoot-through conditions, dead time introduces nonlinear distortions in the output voltage. Dead-time compensation was therefore implemented according to the formulations introduced in the background section. The inverter feeds a three-phase passive load composed of magnetically independent air-core inductors connected in series with a three-phase RC network. The phase currents are measured using Hall-effect current probes. Experimental waveforms were acquired using a digital oscilloscope (DS1054Z, Rigol, Beijing, China [39]) at a sampling rate of 5 MHz without filtering and subsequently processed (plotted) in MATLAB 2025b. The load can be represented as a series RL circuit followed by a parallel RC branch for each phase. The adopted parameters are consistent with the simulation:

- Series RL load with $R = 727 \text{ m}\Omega$ and $L = 1.73 \text{ mH}$.
- Parallel RC load with $R_0 = 6.6 \Omega$ and $C_0 = 45 \mu\text{F}$.

The DC-link voltage was set to 70 V. This value was obtained by scaling the simulation voltage of 98 V to ensure safe operation of the experimental setup. Preliminary analytical and simulation investigations consistently showed that, under asynchronous operating conditions, the resulting duty-cycle errors could generate significant voltage and current spikes. Such transients may compromise the reliable operation of the power converter and expose the hardware to excessive electrical stress. For this reason, a lower DC-link voltage was adopted during the experimental validation. In the present application, $k = 8$ was selected as a compromise between waveform visibility and operating conditions representative of the targeted application. In particular, a fundamental frequency of 50 Hz was adopted; this choice is dictated by the inherent characteristics of the laboratory load. Nevertheless, the resulting modulation frequency ratio m_f remains relatively low, even with $k = 8$, when compared with those typically encountered in conventional industrial drive applications. Although this choice facilitates waveform observation, it still results in a relatively low switching-to-fundamental frequency ratio, with the switching frequency never exceeding 3.6 kHz. Consequently, the experimental conditions remain consistent with the low- m_f operating regime considered throughout this work. The algorithm used for the experimental tests was directly derived from the simulation model using the embedded C-code generation capabilities of PLECS. During the operation, the RT Box achieved an average simulation time step of approximately 3 μs . Given a switching frequency of 3.6 kHz, which corresponds to a carrier period of approximately 277.77 μs , the modulating signals are updated more than 90 times per carrier period. This represents a significant oversampling rate compared to the standard double sampling per carrier period typical of RS-PWM. Considering that even without rigorous code optimization and without leveraging specialized hardware such as FPGAs for PWM signal generation it was possible to achieve a massive oversampling rate, it is reasonable to conclude that the intrinsic discretization of the microcontroller aligns more closely with a theoretical NS-PWM rather than with the forced sampling of a RS-PWM in this specific implementation. Table 2 resumes the main test parameter.

Table 2. Experimental setup circuitual parameters.

Parameter	Symbol	Value	Unit
DC-link voltage	V_{dc}	70	V
dead time	t_d	4	μs
RL circuit	R	727	$\text{m}\Omega$
	L	1.73	mH
RC circuit	R_o	6.6	Ω
	C_o	45	μF
Frequency ratio	k	8	-

The main objective of the test was to verify the occurrence of current spikes associated with the intrinsic DPWM1 discontinuities when they occur at the middle of a carrier half-period. This condition represents the most critical operating scenario, since the resulting current spikes are not only larger in magnitude but also occur four times per fundamental period. Conversely, the current spike associated with the transition from SVPWM to DPWM1, although potentially significant, is typically observed only when the modulation index crosses the threshold value $m_{th} = 0.72$. To this end, two different control configurations were implemented. In the first configuration, referred to as the symmetric case, the transition from SVPWM to DPWM1 is performed together with the frequency scaling factor $d = 1.5$ while correctly applying the Homologous Peak Commutation strategy. Under these conditions, the DPWM1 discontinuities remain synchronized with the carrier extrema and occur exclusively at the carrier top peaks or bottom peaks, depending on the selected initial carrier phase. In the second configuration, referred to as the asymmetric case, the Homologous Peak Commutation strategy is not applied. As a consequence, the DPWM1 discontinuities occur at the middle of the carrier half-period, generating the duty-cycle errors discussed in the previous section. The experimental results obtained for both the symmetric and asymmetric configurations are reported for modulation indices ranging from $m = 0.5$ to $m = 0.8$. The comparison between the two cases is shown in Figure 12.

The THD values corresponding to the experimental results for modulation indices ranging from 0.1 to 0.9 are presented in Table 3. The results are consistent with the numerical analysis shown in Figure 9. In particular, the synchronized implementation exhibits lower THD than the asynchronous one over the entire investigated modulation-index range, confirming the effectiveness of the proposed synchronization strategy in mitigating the current spikes associated with unsynchronized GDPWM discontinuities. Furthermore, the relative THD improvement follows a similar trend to that observed in the numerical results, increasing from low modulation-index values up to approximately $m_i = 0.5$, where the maximum benefit is achieved, and then gradually decreasing as the modulation index approaches unity.

Table 3. THD calculated from the experimental waveforms at various m_i .

m_i	Asynchronous THD (%)	Synchronous THD (%)	THD Reduction (%)
0.1	38.14	34.40	9.824
0.2	29.74	26.65	10.38
0.3	26.18	22.54	13.88
0.4	23.23	19.29	16.96
0.5	21.13	16.53	21.77
0.6	16.42	14.26	13.17
0.7	12.81	11.77	8.145
0.8	9.906	9.453	4.571
0.9	7.764	7.660	1.350

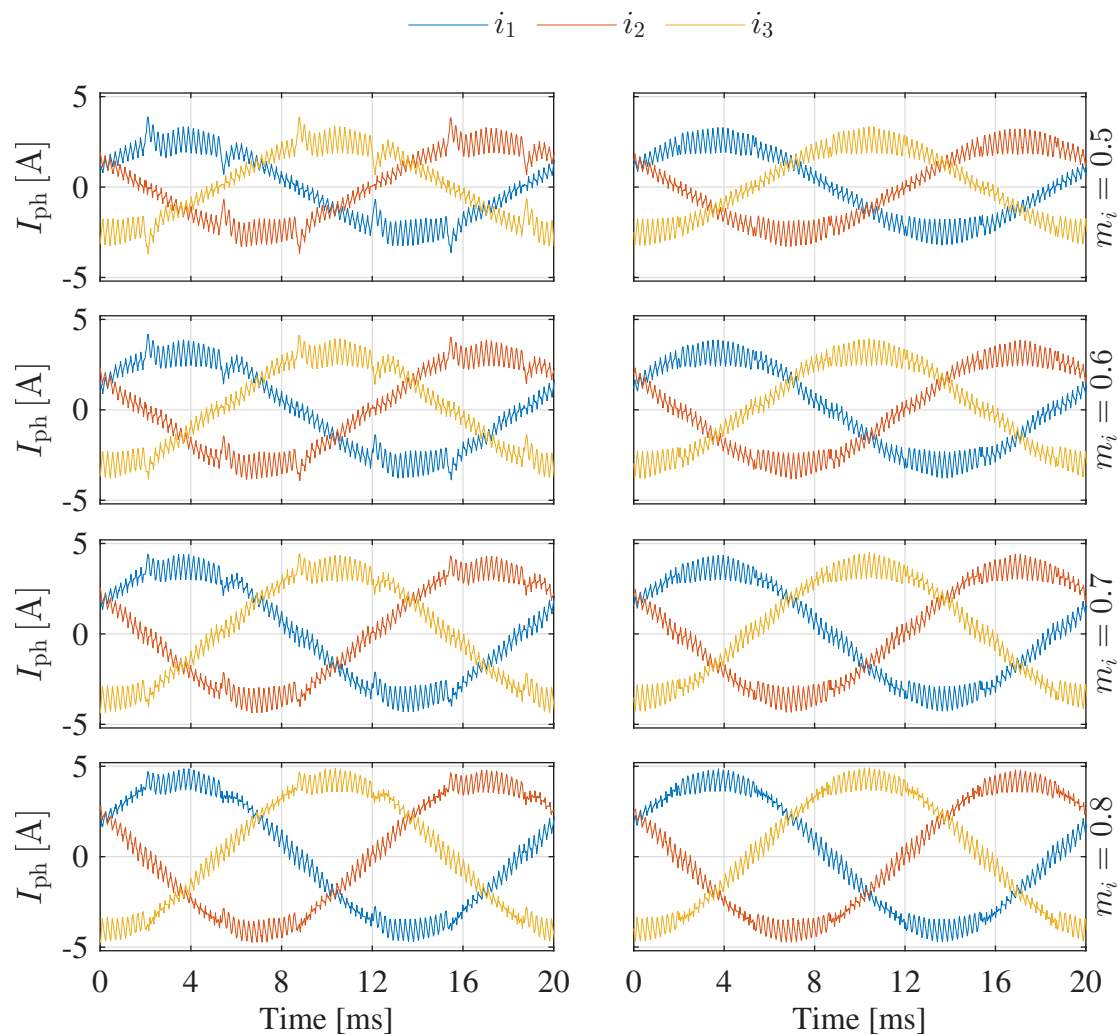


Figure 12. Experimental comparison between asynchronous (**left column**) and synchronized (**right column**) DPWM1 operation for modulation indices ranging from $m_i = 0.5$ to $m_i = 0.8$. In the asynchronous case, current spikes are clearly visible due to the lack of synchronization between the DPWM1 discontinuities and the carrier peak. In the synchronized case, the proposed Homologous Peak Commutation strategy eliminates these disturbances, preserving current continuity over the entire operating range.

Another significant result is the experimental validation of the transition between SVPWM and DPWM1; the effect of the transition on the three-phase currents is visible in Figure 13. The figure reports the experimental transition from SVPWM to DPWM1 obtained by varying the modulation index from $m_i = 0.6$ to $m_i = 0.8$, while maintaining the transition threshold at $m_{th} = 0.7$. The modulation-index variation is applied at $t = 30$ ms, causing the control algorithm to commute from SVPWM to DPWM1 once the threshold is exceeded. The transition is completed without observable current discontinuities or current spikes, confirming the effectiveness of the proposed synchronization strategy under dynamic operating conditions. These results experimentally validate the feasibility of a seamless transition between continuous and discontinuous modulation strategies and further demonstrate the robustness of the proposed implementation in a realistic operating scenario.

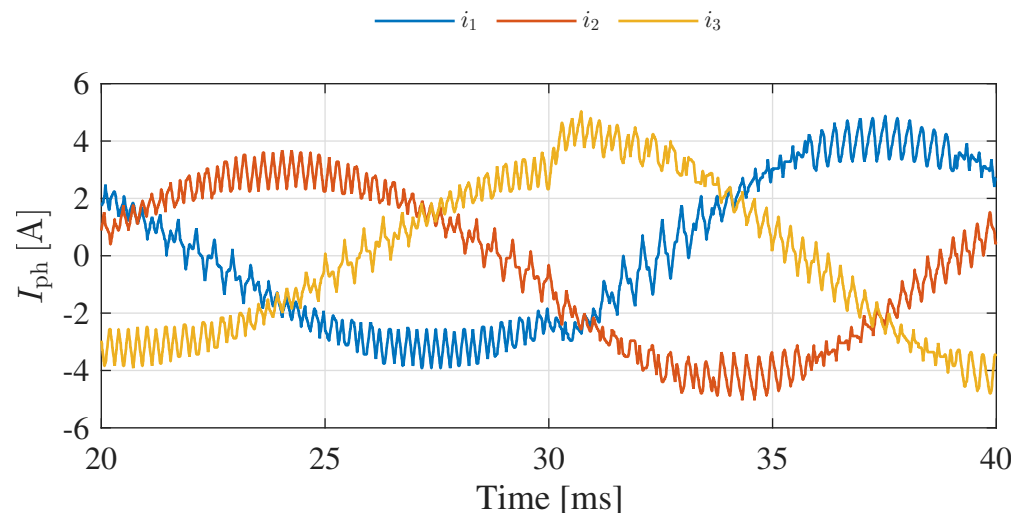


Figure 13. Experimental transition from SVPWM to DPWM1. The modulation index is varied from $m_i = 0.6$ to $m_i = 0.8$, causing the commutation from SVPWM to DPWM1 when the threshold $m_{th} = 0.7$ is exceeded. No observable current spikes or discontinuities are generated during the transition, confirming the effectiveness of the proposed synchronization strategy.

6. Conclusions

This work has been developed in the context of high-speed drive applications, where the switching-to-fundamental frequency ratio is typically low and the advantages of NS-PWM over RS-PWM become increasingly significant. Within this operating scenario, the feasibility of a transition between SVPWM and DPWM1 under variable switching-frequency operation has been investigated and experimentally validated. The proposed approach extends the implementation of online modulation transitions to the NS-PWM domain. During the analysis, several synchronization issues, not previously addressed in the literature, were identified and resolved. In particular, a dedicated synchronization strategy among the carrier, the modulating signals, and the GDPWM trigger signal was introduced, enabling seamless transitions between SVPWM and DPWM1 without generating current spikes at the transition instant. A second contribution concerns the analysis of the intrinsic DPWM1 discontinuities when a frequency scaling factor $d = 1.5$ is adopted to compensate for the reduced switching activity introduced by the clamped intervals. It was demonstrated that, without the proposed Homologous Peak Commutation strategy, the resulting loss of synchronization generates recurring duty-cycle errors, leading to voltage discontinuities and current spikes during normal operation. The proposed synchronization method effectively eliminates these distortions by maintaining the alignment between the GDPWM discontinuities and the carrier extrema. Numerical and experimental results confirmed the validity of the proposed approach. The developed control strategy preserves current continuity during both modulation transitions and intrinsic DPWM1 discontinuities while maintaining compatibility with variable switching-frequency operation. Furthermore, the elimination of asynchronous discontinuity events leads to an improvement in current quality and THD, which becomes increasingly significant as the switching-to-fundamental frequency ratio decreases. The experimental validation further confirmed the theoretical and numerical findings. In particular, the measurements showed that, when the proposed Homologous Peak Commutation strategy is not implemented, current spikes appear at the DPWM1 discontinuities due to the loss of synchronization between the discontinuities and the carrier extrema. Conversely, when the proposed synchronization method is applied, these spikes are effectively eliminated, preserving current continuity under real operating conditions. These results provide experimental evidence of the practical effectiveness of the proposed approach and confirm the validity of the theoretical analysis.

These results demonstrate that synchronized transitions between SVPWM and DPWM1 can be reliably implemented in NS-PWM-based high-speed drive applications, extending the operating range of discontinuous modulation techniques while preserving waveform quality and reducing the adverse effects associated with asynchronous modulation changes. Future research will investigate computationally efficient implementations capable of reproducing the benefits of NS-PWM with reduced oversampling requirements, including carrier-synchronized approaches based on the analytical estimation of carrier–modulating signal intersection points. Such techniques could improve the practical applicability of the proposed strategy on embedded control platforms while preserving the advantages of natural-sampled operation.

Author Contributions: Conceptualization, D.F., G.F., M.R., N.M. and R.M.; methodology, M.R. and R.M.; software, D.F. and G.F.; validation, M.R., N.M. and R.M.; formal analysis, D.F., G.F. and R.M.; investigation, D.F., G.F. and R.M.; resources, M.R., N.M. and R.M.; data curation, D.F.; writing—original draft preparation, D.F. and G.F.; writing—review and editing, D.F., G.F., M.R., N.M. and R.M.; visualization, D.F. and G.F.; supervision, M.R., N.M. and R.M.; project administration, R.M.; funding acquisition, N.M. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data is contained within the article.

Conflicts of Interest: Authors Davide Ferreli, Gianluca Fichera and Nicola Matteazzi were employed by Blue Matter srl. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

VSI	Voltage Source Inverter
THD	Total Harmonic Distortion
WBG	Wide Bandgap
PWM	Pulse-Width Modulation
NS-PWM	Natural-Sampled Pulse-Width Modulation
RS-PWM	Regular-Sampled Pulse-Width Modulation
SPWM	Sinusoidal Pulse-Width Modulation
SVPWM	Space Vector Pulse-Width Modulation
GDPWM	Generalized Discontinuous Pulse-Width Modulation
DPWM	Discontinuous Pulse-Width Modulation
DPWMAX	Discontinuous Pulse-Width Modulation Maximum
DPWMIN	Discontinuous Pulse-Width Modulation Minimum
VSF	Variable Switching Frequency
RMS	Root Mean Square
RL	Resistor–Inductor
RC	Resistor–Capacitor

References

1. Grandi, G.; Loncarski, J.; Srndovic, M. Analysis and Minimization of Output Current Ripple for Discontinuous Pulse-Width Modulation Techniques in Three-Phase Inverters. *Energies* **2016**, *9*, 380. [[CrossRef](#)]
2. Li, B.; Zhu, J.G.; Liu, C.; Li, Y.; Zhao, F.; Jiang, Q. Design and Comparative Study of Ultrahigh-Speed Permanent Magnet Motors with Different Soft Magnetic Materials. *IEEE Trans. Magn.* **2023**, *59*, 1–5. [[CrossRef](#)]

3. Zhou, P.; Gerada, D.; Xu, Z.Q.; Gerada, C. High-Speed Permanent Magnet Electrical Machines—Applications, Key Issues and Challenges. *CES Trans. Electr. Mach. Syst.* **2018**, *2*, 23–33. [[CrossRef](#)]
4. Wang, Q.; Yang, S.; Wang, Y. Harmonic Distortion Analysis and Suppression for Asynchronous SVPWM at Low Sampling-to-Fundamental Frequency Ratios. *IEEE Trans. Power Electron.* **2025**, *40*, 9723–9736. [[CrossRef](#)]
5. Jo, S.I.; Lee, W.J. Compensation Method of PWM Inverter Output Voltage under Low Sampling-to-Fundamental Frequency Ratio Operating Conditions. *J. Power Electron.* **2023**, *23*, 904–912. [[CrossRef](#)]
6. Riedemann, J.; Zhu, Z.Q.; Stone, D.A.; Foster, M.P.; Greenough, J.; Takemoto, K.; Ivanovic, D.; Bateman, B. A Novel PWM Strategy Capable to Operate in Overmodulation Range with Low Switching-to-Fundamental Frequency Ratio. *IEEE Trans. Transp. Electr.* **2025**, *11*, 1106–1116. [[CrossRef](#)]
7. Kaminski, N. State of the Art and the Future of Wide Band-Gap Devices. In Proceedings of the 2009 13th European Conference on Power Electronics and Applications, Barcelona, Spain, 8–10 September 2009; pp. 1–9.
8. Morya, A.K.; Gardner, M.C.; Anvari, B.; Liu, L.; Yepes, A.G.; Doval-Gandoy, J.; Toliyat, H.A. Wide Bandgap Devices in AC Electric Drives: Opportunities and Challenges. *IEEE Trans. Transp. Electr.* **2019**, *5*, 3–20. [[CrossRef](#)]
9. Stumpf, P.; Járđán, R.; Nagy, I. Comparison of Naturally Sampled PWM Techniques in Ultrahigh Speed Drives. In Proceedings of the 2012 IEEE International Symposium on Industrial Electronics, Hangzhou, China, 28–31 May 2012; pp. 246–251.
10. Bowes, S.R. New sinusoidal pulsewidth-modulated inverter. In *Proceedings of the Institution of Electrical Engineers*; IET: Hertfordshire, UK, 1975.
11. Muñoz-Ramírez, M.; Valderrama-Blavi, H.; Rivera, M.; Restrepo, C. An Approach to Natural Sampling Using a Digital Sampling Technique for SPWM Multilevel Inverter Modulation. *Energies* **2019**, *12*, 2925. [[CrossRef](#)]
12. Stumpf, P.; Járđán, R.K.; Nagy, I. DC components and subharmonics generated by naturally sampled PWM techniques. In Proceedings of the IECON 2012–38th Annual Conference on IEEE Industrial Electronics Society, Montreal, QC, Canada, 25–28 October 2012; pp. 327–332. [[CrossRef](#)]
13. Bowes, S.; Lai, Y.S. The relationship between space-vector modulation and regular-sampled PWM. *IEEE Trans. Ind. Electron.* **1997**, *44*, 670–679. [[CrossRef](#)]
14. Ojo, O. The Generalized Discontinuous PWM Scheme for Three-Phase Voltage Source Inverters. *IEEE Trans. Ind. Electron.* **2004**, *51*, 1280–1289. [[CrossRef](#)]
15. Zeng, Z.; Li, Z.; Goetz, S.M. Optimal Discontinuous Space Vector PWM for Zero-Sequence-Circulating Current Reduction in Two Paralleled Three-Phase Two-Level Converter. *IEEE Trans. Ind. Electron.* **2021**, *68*, 1252–1262. [[CrossRef](#)]
16. Hava, A.; Kerkman, R.; Lipo, T. A high-performance generalized discontinuous PWM algorithm. *IEEE Trans. Ind. Appl.* **1998**, *34*, 1059–1071. [[CrossRef](#)]
17. Zhang, P.; Wang, S.; Li, Y. Generalized N-State Random Pulse Position Discontinuous PWM for High-Frequency Harmonics Reduction and Performance Improvement at High Modulation Ratios. *IEEE Trans. Power Electron.* **2024**, *39*, 13659–13671. [[CrossRef](#)]
18. Mandrioli, R.; Viatkin, A.; Hammami, M.; Ricco, M.; Grandi, G. Variable Switching Frequency PWM for Three-Phase Four-Wire Split-Capacitor Inverter Performance Enhancement. *IEEE Trans. Power Electron.* **2021**, *36*, 13674–13685. [[CrossRef](#)]
19. Lahu, S.; Deepak, N.; Kanagaraj, R. Real-Time Transition from Continuous PWM to Discontinuous PWM Technique. In Proceedings of the 2024 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), Bangalore, India, 12–14 July 2024; pp. 1–6.
20. Venkatesh, A.; Schnell, A.; Hashemi-Zadeh, A.; Goetz, S.M. Seamless Transition Strategy for Multi-Mode PWM in Two-Level Inverter-Fed High-Speed Drives. In Proceedings of the IECON 2025–51st Annual Conference of the IEEE Industrial Electronics Society, Madrid, Spain, 14–17 October 2025; pp. 1–6.
21. Zhang, H.; Liu, W.; Chen, Z.; Jiao, N. Smooth Transition of Multimode Synchronous Modulation for IPMSM Sensorless Drives in Rail-Transit Applications. *IEEE Trans. Ind. Electron.* **2021**, *68*, 128–138. [[CrossRef](#)]
22. Xue, Y.; Li, H.; Wu, Y.; Wang, L.; Zhang, H. A Novel Pulse Width Modulation Strategy Used for Permanent Magnet Synchronous Motor Drives. In Proceedings of the 2024 IEEE 10th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Chengdu, China, 17–20 May 2024.
23. Qin, Z.; Wang, H.; Blaabjerg, F.; Loh, P.C. The Feasibility Study on Thermal Loading Control of Wind Power Converters with a Flexible Switching Frequency. In Proceedings of the 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, Canada, 20–24 September 2015; pp. 485–491.
24. Ibrahim, A.; Sujod, M. Variable Switching Frequency Hybrid PWM Technique for Switching Loss Reduction in a Three-Phase Two-Level Voltage Source Inverter. *Measurement* **2019**, *151*, 107192. [[CrossRef](#)]
25. Deslauriers, I.; Avdiu, N.; Ooi, B. Naturally Sampled Triangle Carrier PWM Bandwidth Limit and Output Spectrum. *IEEE Trans. Power Electron.* **2005**, *20*, 100–106. [[CrossRef](#)]
26. Nguyen, M.H.; Kwak, S.; Choi, S. Modified Discontinuous Pulsewidth Modulation Approach with Independent Phase Loss Adjustment for Voltage Source Converters. *IEEE Access* **2023**, *11*, 115529–115555. [[CrossRef](#)]

27. Holtz, J. Pulsewidth Modulation for Electronic Power Conversion. *Proc. IEEE* **1994**, *82*, 1194–1214. [[CrossRef](#)]
28. Walker, G.R. Digitally Implemented Naturally Sampled PWM Suitable for Multilevel Converter Control. *IEEE Trans. Power Electron.* **2003**, *18*, 1322–1329. [[CrossRef](#)]
29. Suryavalli, U.; Hari, V.S.S.P.K. Influence of Sampling Method and Frequency Ratio on PWM Voltage Harmonics in Two-Level Voltage Source Inverters. *IEEE Trans. Ind. Electron.* **2025**, *72*, 8778–8788. [[CrossRef](#)]
30. Bowes, S.R.; Bird, B.M. Novel approach to the analysis and synthesis of modulation processes in power convertors. In *Proceedings of the Institution of Electrical Engineers*; IET: Hertfordshire, UK, 1975.
31. Mandrioli, R.; Viatkin, A.; Hammami, M.; Ricco, M.; Grandi, G. A Comprehensive AC Current Ripple Analysis and Performance Enhancement via Discontinuous PWM in Three-Phase Four-Leg Grid-Connected Inverters. *Energies* **2020**, *13*, 4352. [[CrossRef](#)]
32. van der Broeck, H.W.; Skudelny, H.C.; Stanke, G.V. Analysis and realization of a pulsewidth modulator based on voltage space vectors. *IEEE Trans. Ind. Appl.* **1988**, *24*, 142–150. [[CrossRef](#)]
33. O'Rourke, C.J.; Qasim, M.M.; Overlin, M.R.; Kirtley, J.L. A Geometric Interpretation of Reference Frames and Transformations: dq0, Clarke, and Park. *IEEE Trans. Energy Convers.* **2019**, *34*, 2070–2083. [[CrossRef](#)]
34. Hava, A.M.; Kerkman, R.J.; Lipo, T.A. Simple Analytical and Graphical Methods for Carrier-Based PWM–VSI Drives. *IEEE Trans. Power Electron.* **1999**, *14*, 49–61. [[CrossRef](#)]
35. Jeong, S.G.; Park, M.H. The Analysis and Compensation of Dead-Time Effects in PWM Inverters. *IEEE Trans. Ind. Electron.* **1991**, *38*, 108–114. [[CrossRef](#)]
36. Zhou, L.; Preindl, M. Variable Switching Frequency Techniques for Power Converters: Review and Future Trends. *IEEE Trans. Power Electron.* **2023**, *38*, 13211–13234. [[CrossRef](#)]
37. Plexim GmbH. *RT Box: Real-Time Simulator for Power Electronics—Product Documentation and Datasheet*; Plexim GmbH: Zurich, Switzerland, 2025.
38. TDK-Lambda Corporation. *Genesys GEN100-33 Programmable DC Power Supply Datasheet*; TDK-Lambda Corporation: Tokyo, Japan, 2024.
39. Rigol Technologies. *DS1054Z Digital Oscilloscope User's Guide and Datasheet*; Rigol Technologies: Beijing, China, 2024.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.