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The Role of Frequency and Duty Cycle on the Gate Reliability of p-GaN HEMTs

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***Abstract*— In this letter, we present an extensive analysis on the role of both switching frequency (ranging from 100 kHz to 1 MHz) and duty cycle (from 10% to 90%) on the time-dependent gate breakdown of high electron mobility transistors (HEMTs) with Schottky metal to p-GaN gate. More specifically, results show how the gate lifetime of GaN HEMTs increases by reducing the frequency and the duty cycle of the stressing gate signal (V_G). Such behavior is ascribed to the OFF-time, which is responsible to alter the electrostatic potential in the p-GaN layer during the rising phases of V_G (from OFF- to ON-state). Findings of this analysis are useful both for further technology improvement and for GaN-based power circuit designers.**

***Index Terms* — GaN HEMTs, Gate Reliability, Schottky Gate, Pulsed Gate Stress, Switching Conditions.**

I. Introduction

TO date the use of AlGaN/GaN High Electron Mobility Transistors (HEMTs) is spreading on several power applications, including adapters, power supplies, photovoltaic inverters, battery charges, etc. The interest in such devices is due to their capability to manage high power densities and high frequencies with higher efficiency with respect to the Si-based technology competitor [1]-[4].

The normally-OFF GaN HEMT controlled by a Schottky metal to p-GaN gate structure is considered as one of the best solutions offering the best trade-off between performance, reliability and cost [5]-[8]. However, the complexity of the two back-to-back diodes composing the gate structure, is responsible for performance and reliability concerns mostly caused by the charging and/or discharging processes of the semi-floating p-GaN layer [9]-[16].

For these reasons, many challenges have been faced in finding experimental methodologies and physical-statistical approaches to better evaluate the gate reliability [9]-[25]. However, as any technology attracting attention due to its wide use, reliability should be assessed, as far as possible, under operating conditions similar to those experienced in a real application.

The time-dependent gate breakdown (TDGB) under DC stress condition has been widely discussed [17]-[23], whereas, to the best of our knowledge, only few papers report TDGB analysis under pulsed stress condition. The latter is of paramount importance since, in switching power applications, the GaN transistor's gate is repeatedly switched, at relatively high frequency, between relatively high (ON-state) and low voltage values (OFF-state).

In [24], the Mean Time to Failure (MTTF) of the gate has been investigated under pulsed stress tests in a frequency range between 10 kHz and 100 kHz. It turns out that, under such conditions, the gate robustness is weakly affected by the switching frequency.

In [25], we recently reported a TDGB analysis under pulsed stress conditions, exploring higher switching frequencies up to 3.3 MHz. By combining experiments and TCAD simulations, it has been demonstrated that the TTF may be strongly affected by the switching phases. More specifically, it emerged that the OFF-time and the slew rate affect the electrostatic potential of the p-GaN layer and the gate current during the transition phases, respectively, eventually altering the related degradation rate.

In this paper, the analysis reported in [25] is extended by exploring different switching frequencies and duty cycles. Furthermore, the lifetime extrapolated by means of AC-stress performed at different gate voltages is compared with the DC case, highlighting aspects which are important for both technology manufacturers and GaN-based circuits designers.

II. Experimental Details

The considered test structures are HEMTs with Schottky metal to p-GaN gate, fabricated by imec on a 200-mm Silicon substrate. The schematic cross-section can be found in [26].

The transition layer consists of a 200-nm thick AlN nucleation layer, a 0.33-μm (Al)GaN superlattice layer and a 0.5-μm C-doped GaN back barrier. On top of it, the heterojunction is realized by a 200-nm unintentional doped GaN channel layer and a 16-nm thick AlGaN barrier with

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23.5% Aluminum (Al) content. Finally, an 80-nm thick p-GaN layer doped with a Magnesium concentration of 3×10^{19} cm^{-3}, followed by metal forms the Schottky gate junction. The devices under test (DUTs), designed ad-hoc for gate reliability analysis, feature a symmetrical structure with equal gate-to-source and gate-to-drain distance ($L_{GS} = L_{GD}$) of 1.25 µm. The gate width (W_G) and length (L_G) are 10 µm and 0.5 µm, respectively. The gate breakdown voltage is ~ 11 V.

The role of the frequency and duty cycle on the TDGB has been investigated by applying consecutive square-wave pulses at the gate terminal with a Pulse Wave Generator (PWG), while the source and drain contacts are shorted to a single channel Source Measure Unit (SMU), which imposes 0 V. From the SMU the gate leakage current is indirectly monitored to detect the gate time to failure (TTF), defined as the time at which the current suddenly increases above 1 mA. Furthermore, the applied gate signals during the tests are monitored with a high-resolution digital oscilloscope which ensures an appropriate 50 Ohm impedance matching. Further details on the experimental setup can be found in [25].

The stressing gate signal features different frequencies (from 100 kHz to 1 MHz) and duty cycles (from 10% to 90%), while the slew rate (or transition time t_{TR}) is fixed at 5 ns. Finally, a stress temperature of 150 °C is adopted for all the experiments, as it represents the maximum operating junction temperature for commercial GaN-based FETs.

III. Results and Discussion

Fig. 1 shows the contour plot of the MTTF as a function of both frequency (f) and duty cycle (D), by applying a stressing waveform with amplitude V_G = 9.4 V. The MTTF represent the mean value calculated over the time-to-breakdown of 10 devices. It emerges that, by increasing the frequency and/or the duty cycle, the gate MTTF decreases.

In order to identify the cause of such behavior, the MTTF reported in Fig. 1 is plotted as a function of the ON-time (T_{ON}) and the OFF-time (T_{OFF}) in Fig. 2(a) and Fig. 2(b), respectively. It is worth noting that T_{ON} and T_{OFF} represent the semi-periods in which devices are kept in the ON- and OFF-state, respectively. Different groups featuring a similar T_{OFF} have been identified and represented by a different color in order to highlight the lack of the MTTF dependency on T_{ON}. On the contrary, by focusing on a fixed T_{ON} (e.g. 1 µs) a clear T_{OFF} dependency shows up, i.e. the shorter T_{OFF}, the shorter MTTF. The latter is further confirmed by Fig. 2(b), where MTTF is plotted as a function of the T_{OFF}, independently of the T_{ON}.

In [25] TCAD simulations have highlighted that, in the transition phase from OFF- to ON-state, the semi-floating p-GaN layer exhibits an electrostatic potential (V_{pGaN}) peak. The magnitude of such peak is ruled by T_{OFF}, i.e., it decreases by reducing T_{OFF}. As a consequence, the voltage drop on the Schottky depletion region ($V_{Schottky} = V_G - V_{pGaN}$) during the transition phase increases by reducing T_{OFF}. The latter, combined with the relatively high gate current occurring during the switching phase [25], causes a shorter TTF.

These mechanisms explain the behavior of the MTTF shown in Fig 1. In fact, as confirmed by Fig. 3, increasing f and D, the T_{OFF} decreases causing a shorter MTTF. The role of

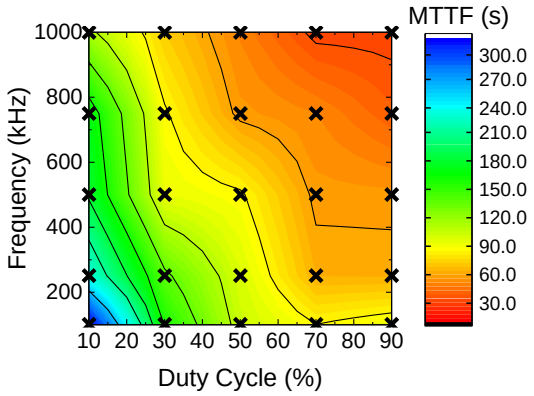

Fig. 1. Contour plot showing the dependency of the gate MTTF on both the frequency and the duty cycle at V_G = 9.4 V and T = 150 °C. 10 devices per group have been stressed to extrapolate the MTTF. The symbols "X" represent the implemented stress conditions.

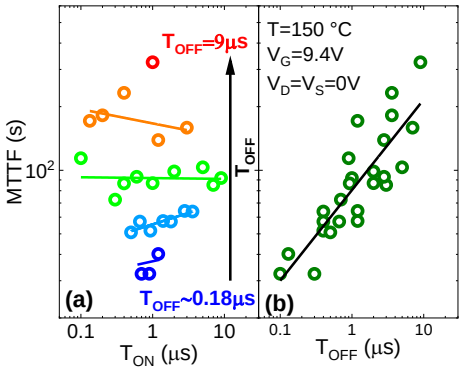

Fig. 2.(a) ON-Time and (b) OFF-Time dependency of the MTTF at V_G = 9.4 V and T = 150 °C. Each MTTF point is the result of 10 stressed devices.

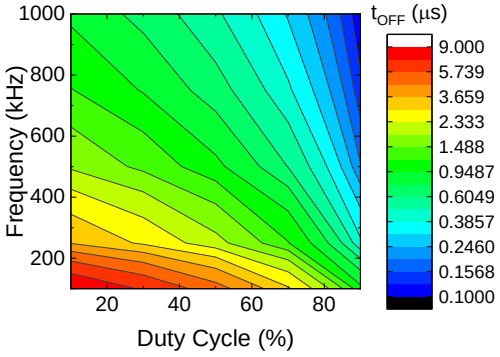

Fig. 3. Contour plot showing how the OFF-Time changes with both the frequency and the duty cycle.

T_{OFF} on the electrostatic potential peak is ascribed to time-dependent charging and/or discharging processes occurring in the p-GaN layer, which alter the mobile charge and, hence, its electrostatic potential [16]. Indeed, as shown in [25], the latter changes after the device is turned-OFF, taking tens of microseconds before reaching a quasi-steady state. As a result, the related peak after the switching-ON transition is determined by the electrostatic potential level reached at the end of T_{OFF}. The latter, as shown in [25], should be longer than 5 µs to have an imperceptible impact on the electrostatic potential peak and hence a negligible effect on the gate TTF.

From Fig. 1, it is possible to identify a best and a worst case for the gate MTTF, i.e. {f = 100 kHz; D = 10%} and {f = 1 MHz; D = 90%}, respectively. Such cases have been explored at different gate voltages in order to extrapolate the gate

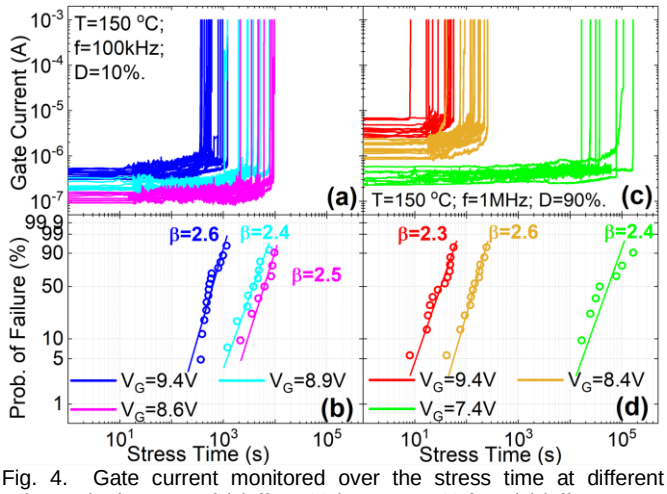

Fig. 4. Gate current monitored over the stress time at different voltages in the case of (a) {f = 100 kHz; D = 10%} and (c) {f = 1 MHz; D = 90%} with the corresponding Weibull plots (b) and (d), respectively.

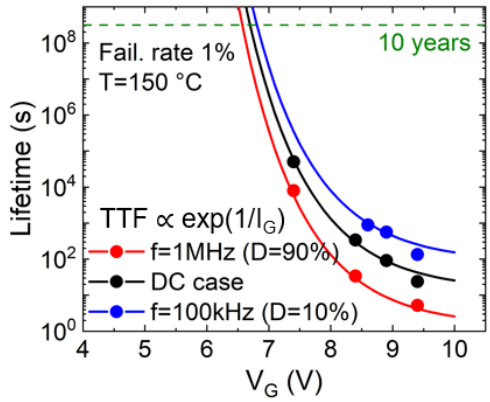

Fig. 5. Lifetime comparison under three different stress conditions: f = 1 MHz and D = 90% (red), DC (black), f = 100 kHz and D = 10% (blue). "TTF ∝ exp (1/I_G)" fitting model [21] has been adopted for all conditions. Failure criterion: 1% at 150 °C extrapolated from the Weibull plots.

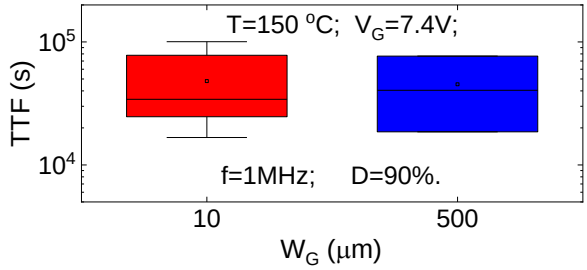

Fig. 6. Area (gate width) dependency of the gate TTF at V_G = 7.4 V, f = 1 MHz, D = 90% and T = 150 °C.

lifetime. Results are reported in Fig. 4. In particular, Fig. 4(a) and 4(b) show the gate current monitored during the stress time and the related Weibull plot in the case of {f = 100 kHz ; D = 10%}, respectively, whereas Fig. 4(c) and 4(d) report same information in the case of {f = 1 MHz ; D = 90%}. In both cases, an abrupt failure and a similar shape parameter (β) ranging between 2.3 and 2.6 is observed, suggesting intrinsic breakdown.

The gate lifetime has been extrapolated and compared, as reported in Fig. 5, with the one predicted by means of standard Constant Voltage Stress (DC) tests. The TTF values are extrapolated from Weibull plots of Fig. 4(b) and 4(d) considering as failure criterion a failure rate equal to 1%. The model in which *TTF* is proportional to *exp (1/I_G)* has been adopted as a fitting means for all the considered cases, DC and pulsed. This model has been proposed in [21] to reproduce the relationship between gate TTF and V_G when the breakdown occurs in the isolation regions rather than in the active gate area. This mechanism has been reported to occur under DC gate stress at relatively high temperatures (T > 80 °C) [21, 22]. It is possible to confirm the presence of this mechanism also in the case of pulsed gate stress. In fact, the observed V_G dependency of the TDGB is the same as for DC case (Fig. 5). Moreover, a lack of area dependency of the gate TTF has been observed also in this context and reported in Fig. 6, in the case of V_G = 7.4 V, f = 1 MHz and D = 90 %.

Finally, Fig.5 shows how the case with f = 1 MHz and D = 90% gives rise to a slightly smaller extrapolated maximum V_G with respect to DC case. When T_{OFF} is relatively short, as explained before, the electrostatic potential of the p-GaN layer is altered during the switching phase, increasing the related degrading effect. The latter is minimized/negligible for longer T_{OFF}. In fact, it is worth noting that the maximum extrapolated gate voltage ensuring 10 years of lifetime related to the case with f = 100 kHz and D = 10% is slightly higher with respect to the one extrapolated under DC stress conditions since, in this case, the TTF is mainly ascribed to the total ON-time in which the device is subject to a positive and relatively high V_G (sum of T_{ON} up to failure).

Moreover, from the percolation theory [27-29], when a defective region is subjected to relatively high electric field, new defects/traps are created in addition to pre-existent ones. Once a critical number of defects forms close each other, a conductive path is created with subsequent layer/device breakdown. Such degradation mechanisms are time dependent. Unlike DC case, under pulsed stress condition the time necessary to reach the failure (i.e., the creation of enough new defects) might be longer since the stress time is continuously interrupted (OFF-time), possibly leading to longer TTF by increasing the relaxation time.

IV. Conclusion

In this work, the effects of the switching frequency and the duty cycle on the time-dependent gate breakdown of GaN HEMTs with a Schottky metal to p-GaN gate structure have been investigated by means of pulsed gate stress tests.

The Time-to-Failure decreases by increasing the frequency and/or the duty cycle, since they induce a shortening of the OFF-time of the square-wave applied to the gate, which in turn alters the electrostatic potential of the semi-floating p-GaN layer during the switching phases.

In addition, a comparison between gate lifetime extrapolated under DC and pulsed stress conditions has been reported. This highlighted that whatever the stressing conditions are, the relationship between gate TTF and V_G at high temperature can be modeled with the same fitting law proposed in [21]. Moreover, results have shown how switching frequency and duty cycle impact on the gate lifetime, providing an important information for technology manufacturers as well as for GaN-based circuits designers.

REFERENCES

[1] K. J. Chen *et al*., "GaN-on-Si Power Technology: Devices and Applications," in *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 779-795, March 2017, doi: 10.1109/TED.2017.2657579.

[2] O. Ambacher et al.,"Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures" , Journal of Applied Physics 85 , 3222-3233 (1999), doi:10.1063/1.369664.

[3] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155-2163, May 2014.doi:10.1109/TPEL.2013.2268900

[4] R. Rupp, T. Laska, O. Häberlen and M. Treu, "Application specific trade-offs for WBG SiC, GaN and high-end Si power switch technologies," *2014 IEEE International Electron Devices Meeting*, 2014, pp. 2.3.1-2.3.4, doi: 10.1109/IEDM.2014.7046965.

[5] D. Marcon, M. Van Hove, B. De Jaeger, N. Posthuma, D. Wellekens, S. You, X. Kang, Tian-Li Wu, M. Willems, S. Stoffels, and S. De- coutere "Direct comparison of GaN-based e-mode architectures (re- cessed MISHEMT and p-GaN HEMTs) processed on 200mm GaN-on-Si with Au-free technology", Proc. SPIE 9363, Gallium Nitride Materials and Devices X, 936311, 2015, doi:10.1117/12.2077806.

[6] G. Greco, F. Iucolano, F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate", Materials Science in Semiconductor Processing, vol. 78, pp. 96-106 (2018), doi:10.1016/j.mssp.2017.09.027.

[7] C. S. Suh and U. K. Mishra, "P-GaN/AlGaN/AlN/GaN enhancement-mode field effect transistor," U.S. Patent 20 080 296 618 A1, 2008.

[8] N. E. Posthuma et al., "An industry-ready 200 mm p-GaN E-mode GaN-on-Si power technology," 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2018, pp. 284-287, **doi:** 10.1109/ISPSD.2018.8393658.

[9] I. Hwang *et al*., "p-GaN Gate HEMTs With Tungsten Gate Metal for High Threshold Voltage and Low Gate Current," in *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 202-204, Feb. 2013, doi: 10.1109/LED.2012.2230312.

[10] L. Sayadi, G. Iannaccone, S. Sicre, O. Häberlen and G. Curatola, "Threshold Voltage Instability in p-GaN Gate AlGaN/GaN HFETs," in *IEEE Transactions on Electron Devices*, vol. 65, no. 6, pp. 2454-2460, June 2018, doi: 10.1109/TED.2018.2828702.

[11] S. Stoffels *et al*., "Failure mode for p-GaN gates under forward gate stress with varying Mg concentration," *2017 IEEE International Reliability Physics Symposium (IRPS)*, 2017, doi: 10.1109/IRPS.2017.7936310.

[12] J. Wei *et al*., "Charge Storage Mechanism of Drain Induced Dynamic Threshold Voltage Shift in ${p}$ -GaN Gate HEMTs," in *IEEE Electron Device Letters*, vol. 40, no. 4, pp. 526-529, April 2019, doi: 10.1109/LED.2019.2900154.

[13] J. He, G. Tang, and K. J. Chen, "VTH instability of p-GaN gate HEMTs under static and dynamic gate stress," *IEEE Electron Device Lett.*, vol. 39, no. 10, pp. 1576–1579, Oct. 2018, doi: 10.1109/LED.2018.2867938.

[14] X. Tang *et al.*, "Demonstration of electron/hole injections in the gate of *p*-GaN/AlGaN/GaN power transistors and their effect on device dynamic performance," in *Proc. 31st Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2019, pp. 415–418, doi: 10.1109/ISPSD.2019.8757614.

[15] X. Li *et al*., "Observation of Dynamic V_{TH} of p-GaN Gate HEMTs by Fast Sweeping Characterization," in *IEEE Electron Device Letters*, vol. 41, no. 4, pp. 577-580, April 2020, doi: 10.1109/LED.2020.2972971.

[16] A. N. Tallarico *et al*., "TCAD Modeling of the Dynamic ΔV_{TH} Hysteresis Under Fast Sweeping Characterization in p-GaN Gate HEMTs," in *IEEE Transactions on Electron Devices*, vol. 69, no. 2, pp. 507-513, Feb. 2022, doi: 10.1109/TED.2021.3134928.

[17] T.-L. Wu et al., "Forward bias gate breakdown mechanism in enhancement-mode p-GaN gate AlGaN/GaN high-electron mobility transistors," IEEE Electron Device Lett., vol. 36, no. 10, pp. 1001–1003, Oct. 2015. doi: 10.1109/LED.2015.2465137.

[18] I. Rossetto et al., "Time-dependent failure of GaN-on-Si power HEMTs with p-GaN gate," IEEE Trans. Electron Devices, vol. 63, no. 6, pp. 2334–2339, Jun. 2016. doi: 10.1109/TED.2016.2553721.

[19] S. Stoffels et al., "Failure mode for p-GaN gates under forward gate stress with varying Mg concentration," in Proc. IRPS, Apr. 2017, pp. 4B-4.1–4B-4.9. doi: 10.1109/IRPS.2017.7936310.

[20] P. Moens and A. Stockman, "A Physical-Statistical Approach to AlGaN/GaN HEMT Reliability," *2019 IEEE International Reliability Physics Symposium (IRPS)*, 2019, doi: 10.1109/IRPS.2019.8720521.

[21] M. Millesimo *et al*., "High-Temperature Time-Dependent Gate Breakdown of p-GaN HEMTs," in *IEEE Transactions on Electron Devices*, vol. 68, no. 11, pp. 5701-5706, Nov. 2021, doi: 10.1109/TED.2021.3111144.

[22] A. N. Tallarico *et al*., "Gate Reliability of p-GaN HEMT With Gate Metal Retraction," in *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4829-4835, Nov. 2019, doi: 10.1109/TED.2019.2938598.

[23] A. N. Tallarico et al., ''Investigation of the p-GaN gate breakdown in forward-biased GaN-based power HEMTs,'' IEEE Electron Device Lett., vol. 38, no. 1, pp. 99-102, Jan. 2017, doi :10.1109/LED.2016.2631640.

[24] J. He, J. Wei, S. Yang, Y. Wang, K. Zhong and K. J. Chen, "Frequency- and Temperature-Dependent Gate Reliability of Schottky-Type p-GaN Gate HEMTs," in *IEEE Transactions on Electron Devices*, vol. 66, no. 8, pp. 3453-3458, Aug. 2019, doi: 10.1109/TED.2019.2924675.

[25] M. Millesimo *et al*., "Gate Reliability of p-GaN Power HEMTs Under Pulsed Stress Condition," *2022 IEEE International Reliability Physics Symposium (IRPS)*, Dallas (Texas), March 2022, doi: 10.1109/IRPS48227.2022.9764592.

[26] A. N. Tallarico et al., "Role of the AlGaN barrier on the long-term gate reliability of power HEMTs with p-GaN gate", Microelectronics Reliability, vol. 114, no. 113872, Nov. 2020, doi:10.1016/j.microrel.2020.113872.

[27] J. Suñé, I. Placencia, N. Barniol, E. Farrés, F. Martín, and X. Aymerich,"On the breakdown statistics of very thin SiO2 films," Thin Solid Films, vol. 185, no. 2, pp. 347-362, Mar. 1990, doi :10.1109/16.853050.

[28] S. W. Kenkel and J. P. Straley, "Percolation Theory of Nonlinear Circuit Elements", Phys. Rev. Lett., vol. 49, pp. 767-770, (1982), doi: 10.1103/PhysRevLett.49.767

[29] M. Houssa, T. Nigam, P.W. Mertens, and M. M. Heyns, "Soft breakdown in ultrathin gate oxides: Correlation with the percolation theory of nonlinear conductors", Appl. Phys. Lett. 73, 514-516 (1998),doi: 10.1063/1.121918.