25th IMEKO TC4 International Symposium
23rd International Workshop on ADC and DAC Modelling and Testing
IMEKO TC-4 2022
Brescia, Italy / September 12-14, 2022

Static Characterization of the X-Hall Current Sensor in BCD10 Technology

Gian Piero Gibiino[1], Marco Crescentini[1,2], Marco Marchesi[3], Marco Cogliati[3], Aldo Romani[1,2], Pier Andrea Traverso[1]

[1]*Dept. Electrical, Electronic, and Information Engineering (DEI), University of Bologna, Italy*
[2]*Advanced Research Center on Electronic Systems (ARCES), University of Bologna, Italy*
[3]*STMicroelectronics, Analog and Smart Power Technology R&D, Cornaredo, Italy*

***Abstract* – This work presents on-wafer characterization measurements of the X-Hall current sensor architecture implemented in 90-nm BCD10 silicon process by STMicroelectronics. With respect to a previous implementation, technological improvements in terms of active region, isolation layers, and metal stack configuration result in a substantially improved sensitivity. In addition, it is reported that the sensitivity can be further improved by applying a negative voltage to the depletion layer.**

I. INTRODUCTION

Current sensors are critical components of modern power electronic circuits and systems. They are used in many different applications, e.g., in the control feedback loop of power converters [1, 2], for monitoring and diagnostic purposes in complex power systems [3, 4], or in metering functions for smart grids and smart homes [5, 6]. The target application sets particular specifications on current sensors, which are ideally required to be small, lossless, accurate, broadband, low-power, or display a combination of such features [7, 8]. Recent research works targeting accuracy and broadband behavior have proposed lossless current sensing solutions based on magnetic approaches for silicon chip implementation [9, 10, 11, 12, 13, 14].

Among these, the X-Hall sensor [15, 14] demonstrated wide bandwidth and minimum space occupation, although suffering from limited sensitivity and suboptimal offset reduction. The improvement of these two static parameters can be addressed at a process technology level by employing selected solutions such as an active region with reduced implants, the substitution of field oxide with shallow trench isolation, and the miniaturization of the metal stack.

This article presents the experimental characterization of an X-Hall sensor implemented in Silicon 90-nm BCD10 technology, which is a more advanced process technology with respect to previous implementations [14]. Section I summarizes the main theory behind the X-Hall sensor and it outlines the major technological features of the BCD10 technology. Section II describes the experimental setup, while Section III discusses the experimental results, comparing the performances against the X-Hall sensor implemented in the previous generation of the BCD process.

II. DESCRIPTION OF THE SENSOR

A. X-Hall sensor topology

The device-under-test (DUT) is a current sensor based on the X-Hall topology, which was firstly proposed in [16]. As shown in Fig. 1, the active region is realized by adopting a lowly-doped n-type well (Fig. 1b), typically used in the BCD process technology as body region for high-voltage devices. Such an active region is shaped as an octagon (Fig. 1a) and it features eight contacts, namely four large contacts (T, B, L, R) for biasing the probe, and four small contacts (1, 2, 3, 4) for the readout of the Hall voltage (Fig. 1c).

The X-Hall probe is DC-biased to overcome the methodological limit of current-spun Hall sensors [11, 17] and thus to maximize the bandwidth. The biasing is applied by feeding two bias currents through two opposite bias contacts (i.e., B and T), while the other two bias contacts (i.e., L and R) are connected to a low-impedance node, typically a ground node. This configuration creates a uniform current distribution in the active region, while polarizing the probe in four orthogonal directions [14]. The application of two opposite bias currents leads to the generation of two output voltages V_A and V_B showing an opposite Hall effect:

$$V_A = V_H + V_{OS,plate}^{(A)}; \tag{1}$$

$$V_B = -V_H + V_{OS,plate}^{(B)}; \tag{2}$$

where $V_{OS,plate}^{(A)}$ and $V_{OS,plate}^{(B)}$ are additive offset voltages. Since there is a unique active region, it is reasonable to assume that these two offset voltages will have the same sign.

The cross-like short-circuit of the sense contacts (Fig. 1d) imposes specific boundary conditions to the charge distribution, implying:

$$V_A = V_B = V_{probe}; \tag{3}$$

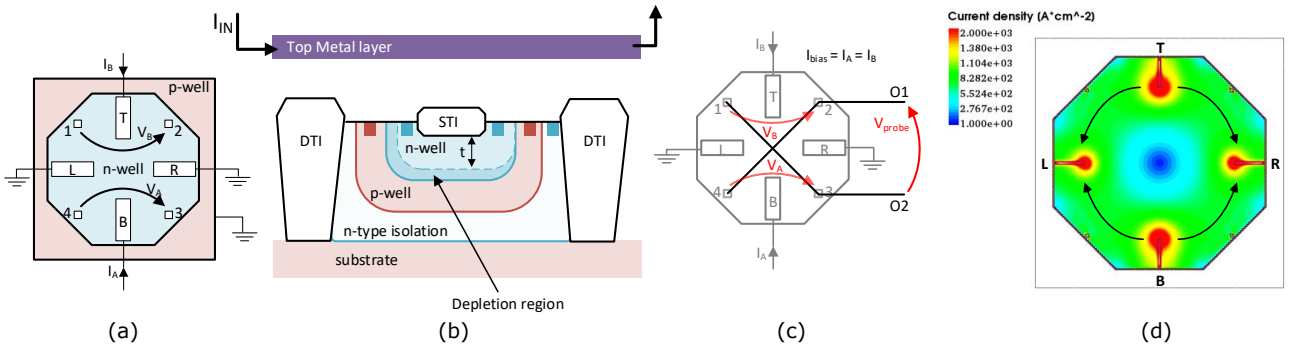

Fig. 1. (a) Top-view of the X-Hall probe displaying the connections of the contacts. (b) Cross-section of the X-Hall probe implemented in BCD10 technology. (c) Cross-like short-circuit of the sense contacts for static offset cancellation. (d) Current density distribution inside the X-Hall sensor obtained by TCAD simulation.

which results in the minimization of the offset voltage. Indeed, the only value for $V_{OS,plate}^{(A)}$ and $V_{OS,plate}^{(B)}$ theoretically satisfying the relationships in (1), (2), and (3) is zero. In practice, there will always be local defects asymmetrically affecting V_A and V_B, so that a residual additive offset ΔV_{OS} will likely be present in the actual sensor device.

Therefore, the output voltage V_{probe} can be written as

$$V_{probe} = V_H + \Delta V_{OS}; \tag{4}$$

where the Hall voltage V_H is related to the bias current I_{bias} and the incident magnetic field B_z by the current-related sensitivity S_I [8]:

$$V_H = S_I I_{bias} B_z. \tag{5}$$

The general expression for the current-related sensitivity is

$$S_I = G_H \frac{r_H}{nqt}; \tag{6}$$

where G_H is the geometrical correction factor, r_H is the Hall factor, t is the effective thickness of the active region, and q is the electron charge [8, 18]. The current-related sensitivity expresses the gain factor of the Hall probe to the magnetic input, while the the overall sensitivity S of the sensor is defined as

$$S = G_{IB} S_I I_{bias}; \tag{7}$$

where G_{IB} is the current-to-magnetic field gain [8].

As usually done in BCD technologies, the active region is isolated from the p-type substrate by a surrounding p-type well (Fig. 1b). This configuration creates a depletion layer involving the junction-field effect, eventually causing nonlinearity due to the modulation of the effective thickness of the active region [18, 8]. In this context, the application of negative voltages on the p-type layer allows to further shrink the effective thickness t and achieve higher sensitivity values.

B. Prototype in BCD10 technology

The DUT is implemented in the STMicroelectronics 90-nm BCD10 technology using the 60-V tolerant n-type diffusion as active layer. With respect to the previous implementation in BCD8 [14], the active layer is covered by a shallow trench isolation (STI) instead of field oxide. This solution reduces the effective thickness, which should lead to higher sensitivity. Moreover, the sensor is laterally isolated using deep-trench isolation (DTI) regions allowing to place the probe closer to high-voltage devices. Finally, the metal stack has smaller dimensions, reducing the distance between the top metal layer and the active region.

This configuration enhances the incident magnetic field on the X-Hall probe for the input current flowing through the 260-μm-wide copper trace realized on the top metal layer [8], eventually improving the overall sensitivity. The active region was designed as an octagon shape inscribed into a circle of 40-μm radius, leading to an active area that is 10% bigger than in the previous version in [14]. This should further increase the sensitivity [19], while also reducing the mean value of the incident magnetic field.

III. MEASUREMENT SET-UP

The block diagram of the on-wafer measurement set-up is reported in Fig. 2a, while a photo of the X-Hall die is reported in Fig. 2b. The die features 22 pads contacted by a custom 22-needle DC probe system. Two slots of a modular DC supply (Agilent N6705B) are used to provide the global device supply (V_{DD}) and to bias the p-ring layer (V_p). The X-Hall device is biased by means of a Source-Measure Unit (Keithley 2450 SMU with accuracy 0.012% and 6.5-digit resolution), allowing to directly impose the bias current (I_{bias}) in the mA range, and sense the bias voltage (V_{bias}) in the V range.

The measurand current (I_{in}) flowing through the metal strip is generated by applying a DC voltage (V_{in}) on a 10-Ω power resistor by means of an additional slot of the modular DC supply. A digital multimeter (Agilent 34401A fea-

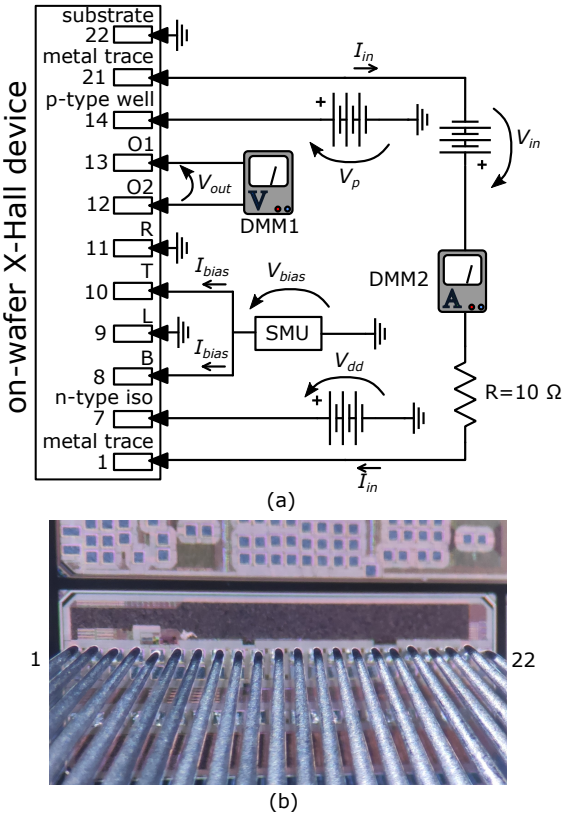

Fig. 2. (a) On-Wafer measurement set-up. (b) Photo of the X-Hall sensor die contacted with a 22-needle DC probe system.

turing 6.5-digit resolution) in ampermeter mode (DMM2 in Fig. 2) is used to retrieve the value of I_{in}, which should be precisely known to accurately characterize the sensitivity of the sensor. The output voltage (V_{out}) is acquired by another digital multimeter (Agilent 34401A, DMM1 in Fig. 2) in voltmeter mode.

IV. EXPERIMENTAL RESULTS

A. Sensitivity and offset

The static characteristics for the DUT biased at $I_{bias} = 1.5$ mA, estimated over the input range of ± 0.5 A for one DUT sample, is reported in Fig. 3a. Ten acquisitions for each input current value have been performed, resulting in an estimated overall sensitivity $\hat{S} = 487$ μV/A with expanded uncertainty $U(\hat{S}) = 3$ μV/A (95% confidence level), and an estimated output-referred residual offset $\Delta\hat{V}_{OS} = 116$ μV with expanded uncertainty $U(\Delta\hat{V}_{OS}) = 1$ μV (95% confidence level). The static characteristic is substantially linear over the entire input range, with a maximum deviation from the linear relationship of 15 μV. The estimated input resistance is 2.24 kΩ, in agreement with the nominal value of 2.5 kΩ.

The measurement procedure over a reduced input range

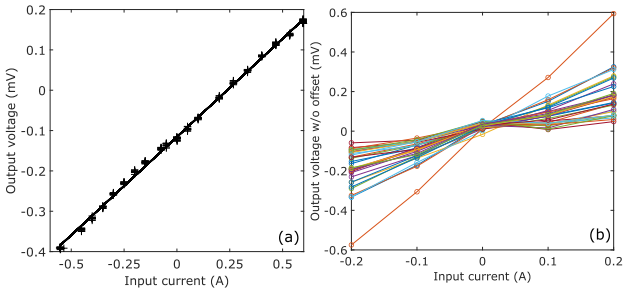

Fig. 3. (a) Static characteristics of a single sample of the DUT biased with I_{bias} = 1.5 mA. (b) Normalized static characteristics of 36 samples of the DUT (different colours for the different samples).

was repeated over a population of 36 DUTs placed on the same wafer, resulting in the static characteristics shown in Fig. 3b, while the process dispersion of sensitivity, offset, and Hall resistance are reported in Fig. 4. The average sensitivity over the entire test population is 0.9 mV/A, whereas the average offset is 384 μV with a standard deviation of 700 μV.

Table 1 compares the above results with those of the same device realized in BCD8 technology as retrieved from [14]. In particular, considering that in [14] the X-Hall sensor was biased at 500 μA, the values reported in Table 1 are the result of an extrapolation to I_{bias} = 1.5 mA. The BCD10 device demonstrated an average improvement of the overall sensitivity by a factor of 28%, which can be attributed to the combination of the larger active area, reduced thickness, and the closeness of the metal trace. To better assess the actual source of sensitivity improvement and identify the G_{IB} factor and Hall sensitivity S_I, it would be necessary to package the devices and provide a controlled magnetic input. However, this is out of the scope of the present work and will be investigated in the future.

The output-referred offset of the X-Hall device in BCD8 technology reported in Table 1 was extrapolated for $I_{bias} = 1.5$ mA multiplying by a factor 3 the value in [14]. The novel DUT in BCD10 technology demonstrated an higher mean residual offset but a similar process spread. This result suggests the possible presence of a systematic error in the silicon process that should be further investigated and likely be tackled in future realizations. Whereas state-of-the-art spun Hall sensors report a sensitivity up to 964 V/AT and offset as low as 15 μV [20], these cannot typically feature MHz-range bandwidths and, anyway, differ from this prototype in terms of technology, sensing methodology, biasing, and layout, which do not allow for a fair comparison.

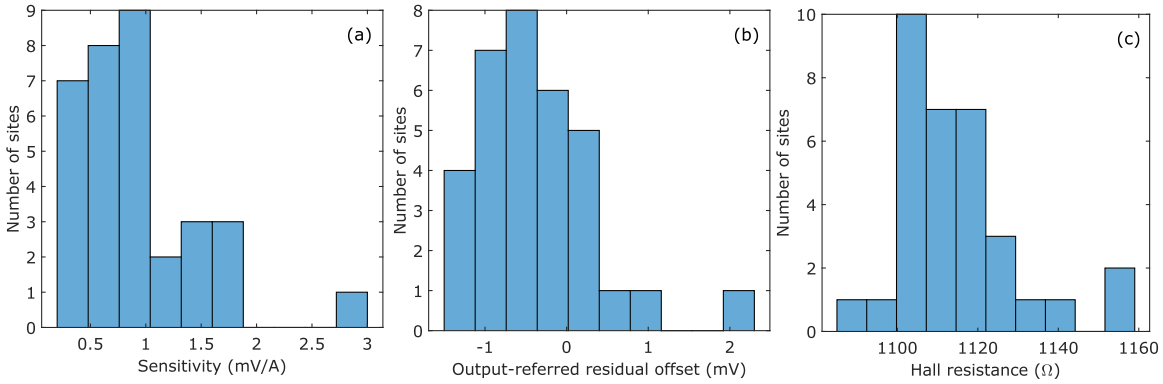

Fig. 4. Distribution of (a) sensitivity, (b) output-referred offset, and (c) input resistance for the DUT in BCD10 technology.

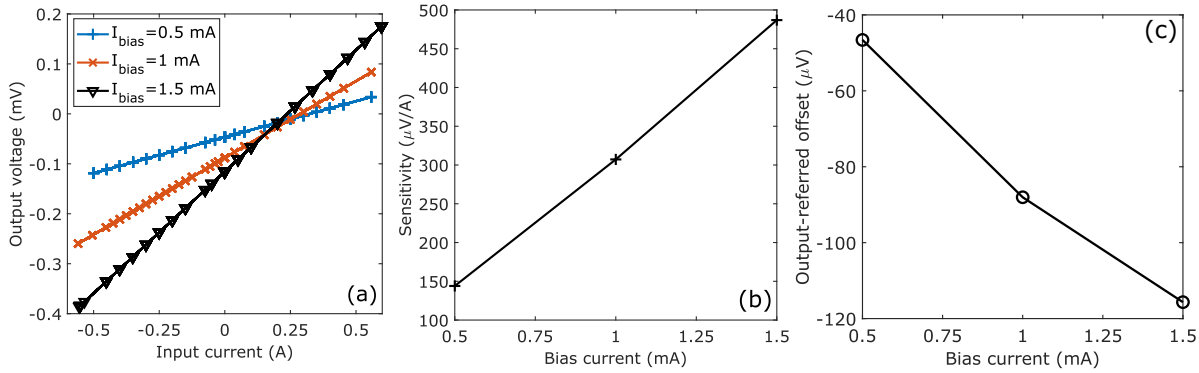

Fig. 5. Effect of the bias current on (a) output voltage, (b) sensitivity, and (c) offset for the DUT in BCD10 technology.

	$\hat{S}$ (mV/A)	$\hat{V}_{OS}$ (μV)	$\sigma(V_{OS})$ (μV)	R_{IN} (kΩ)
BCD8	0.7	195	700	2.5
BCD10	0.9	384	700	2.2

Table 1. Performance comparison between BCD8 and BCD10 technologies.

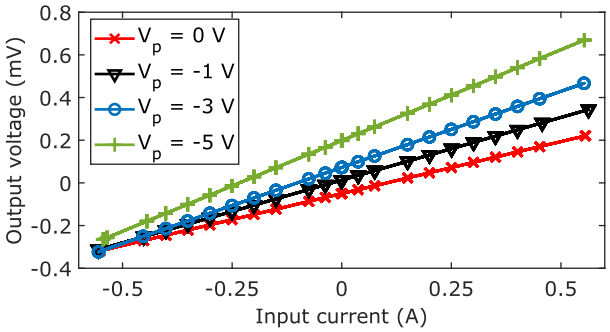

Fig. 6. Static characteristic of a single sample of the DUT in BCD10 technology for different polarization voltages of the p-type encapsulation well.

B. *Effect of polarization*

To prove the linear extrapolation procedure, the static characteristic of a single sample in BCD10 technology was estimated for three values of I_{bias}, namely 500 μA, 1 mA, and 1.5 mA. Sensitivity and residual offset are estimated from the characteristic and reported in Fig. 5, demonstrating a substantially linear relationship. As can be clearly seen, higher values of I_{bias} improve the sensitivity, but they also increase the residual offset, hindering the accuracy.

Finally, the effect of the depletion region on the effective thickness t was investigated by repeating the measurement procedure with different negative voltages applied to the p-type well. The measured static characteristics and the estimated sensitivity and offset performance are reported in Figs. 6 and 7, respectively. The application of negative voltages nearly doubles the sensitivity for an applied voltage of $V_p = -6$ V. However, as expected, the thinner active region also causes an higher offset, limiting the effectiveness of the methodology.

Future work will involve the evaluation of the long-term drifts of the residual offset as well as the temperature dependency, which typically are the most critical aspects.

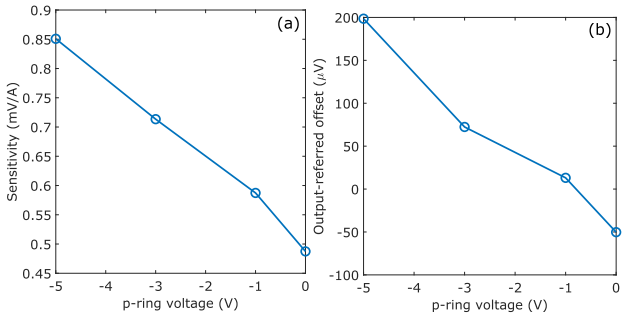

Fig. 7. Effect of the polarization voltage of the p-type well on (a) sensitivity and (b) residual output-referred offset.

ACKNOWLEDGMENT

This work was jointly supported by the European Union's Horizon 2020 research and innovation program, under the Electronic Components and Systems for European Leadership (ECSEL) Joint Undertaking, and from Germany, Slovakia, Netherlands, Spain, and Italy under grant agreement No. 876868.

REFERENCES

[1] H. Wang, X. Hu, Q. Liu, G. Zhao, D. Luo, An On-Chip High-Speed Current Sensor Applied in the Current-Mode DC–DC Converter, IEEE Transactions on Power Electronics 29 (9) (2014) 4479–4484.

[2] A. B. Jorgensen, S. Beczkowski, C. Uhrenfeldt, N. H. Petersen, S. Jorgensen, S. Munk-Nielsen, A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices, IEEE Transactions on Power Electronics 34 (3) (2019) 2494–2504.

[3] S. Zhao, F. Blaabjerg, H. Wang, An overview of artificial intelligence applications for power electronics, IEEE Transactions on Power Electronics 36 (4) (2021) 4633–4658.

[4] M. Pizzotti, M. Crescentini, A. N. Tallarico, A. Romani, An Integrated DC/DC Converter with Online Monitoring of Hot-Carrier Degradation, Institute of Electrical and Electronics Engineers (IEEE), 2020, pp. 562–565.

[5] L. Peretto, The role of measurements in the smart grid era, IEEE Instrumentation and Measurement Magazine 52 (10) (2010) 22–25.

[6] D. Bellasi, M. Crescentini, D. Cristaudo, A. Romani, M. Tartagni, L. Benini, A Broadband Multi-Mode Compressive Sensing Current Sensor SoC in 0.16um CMOS, IEEE Transactions on Circuits and Systems I: Regular Papers 66 (1) (2019) 105–118.

[7] P. Ripka, Electric current sensors: a review, Measurement Science and Technology 21 (11) (2010) 112001.

[8] M. Crescentini, S. F. Syeda, G. P. Gibiino, Hall-effect current sensors: Principles of operation and implementation techniques, IEEE Sensors Journal 22 (11) (2022) 10137–10151.

[9] V. Mosser, N. Matringe, Y. Haddab, A Spinning Current Circuit for Hall Measurements Down to the Nanotesla Range, IEEE Transactions on Instrumentation and Measurement 66 (4) (2017) 637–650.

[10] T. Funk, B. Wicht, A fully integrated DC to 75 MHz current sensing circuit with on-chip Rogowski coil, in: Proc. IEEE Custom Integrated Circuits Conference (CICC), IEEE, San Diego, 2018, pp. 1–4.

[11] M. Crescentini, M. Marchesi, A. Romani, M. Tartagni, P. A. Traverso, A broadband, on-chip sensor based on hall effect for current measurements in smart power circuits, IEEE Transactions on Instrumentation and Measurement 67 (6) (2018) 1470–1485.

[12] Y. Li, M. Motz, L. Raghavan, A Fast T&H Overcurrent Detector for a Spinning Hall Current Sensor With Ping-Pong and Chopping Techniques, IEEE Journal of Solid-State Circuits 54 (7) (2019) 1852–1861.

[13] A. Jouyaeian, Q. Fan, M. Motz, U. Ausserlechner, K. A. A. Makinwa, A 25A Hybrid Magnetic Current Sensor with 64mA Resolution, 1.8MHz Bandwidth, and a Gain Drift Compensation Scheme, in: 2021 IEEE International Solid- State Circuits Conference (ISSCC), Vol. 64, IEEE, 2021, pp. 82–84.

[14] M. Crescentini, et al., The x-hall sensor: Toward integrated broadband current sensing, IEEE Transactions on Instrumentation and Measurement 70 (2020) 1–12.

[15] M. Crescentini, et al., A broadband current sensor based on the x-hall architecture, in: IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS), 2019, pp. 807–810.

[16] M. Crescentini, M. Biondi, M. Marchesi, A. Romani, M. Tartagni, P. A. Traverso, Bandwidth enhancement in hall probe by x-hall DC biasing, Journal of Physics: Conference Series 1065 (2018) 052031.

[17] M. Crescentini, M. Marchesi, A. Romani, M. Tartagni, P. A. Traverso, Bandwidth Limits in Hall Effect-based Current Sensors, ACTA IMEKO 6 (4) (2017) 17.

[18] R. Popovic, Hall Effect Devices, CRC Press, U.S.A, 2003.

[19] M. Crescentini, M. Biondi, A. Romani, M. Tartagni, E. Sangiorgi, Optimum Design Rules for CMOS Hall Sensors, Sensors 17 (4) (2017) 765.

[20] Z. Zhang, F. Lyu, S. He, L. Li, J. Sha, H. Pan, Z. Zhang, Y. Pan, High Sensitivity Horizontal Hall Sensors in 0.35 um BCD Technology, in: 2015 Fifth International Conference on Instrumentation and Measurement, Computer, Communication and Control (IMCCC), IEEE, 2015, pp. 510–514.