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Magnetic sensors

A Comparative Study on Hall Plate Topologies in p-GaN Technology

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Abstract—Gallium nitride (GaN) power transistors are being increasingly used in high-power and high-frequency electronic systems due to their high breakdown field, high carrier density, and good thermal conductivity. Despite these advantages, system durability of GaN-based power systems is hindered by the necessity to work at variable operating conditions. The necessary real-time monitoring of the load current is normally implemented by using external shunt resistors, yet the implementation of GaN-based isolated current sensor would be beneficial to the final power system in terms of space occupation as well as cost. This letter describes the implementation of two Hall-effect devices in p-type GaN (p-GaN) technology, which can potentially be used as integrated current sensors in GaN monolithic implementation. These devices are experimentally characterized and compared in terms of sensitivity, offset, and input resistance. Some nonideality effects are also outlined, identifying future research directions.

Index Terms—Magnetic sensors, current sensors, gallium nitride (GaN), Hall effect, magnetic sensors.

I. INTRODUCTION

Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) are promising devices for power electronics applications due to their intrinsic advantages over conventional silicon [1], [2], [3], [4]. High breakdown field, excellent mobility, high carrier density, and good thermal conductivity are key GaN properties that facilitate the design of modern high-power-density systems. Indeed, the increasing demand for power switching applications—driven by the need for safety, reduced power consumption, and cost minimization—has generated significant interest in the development and manufacturing of enhancement-mode GaN-on-Si power transistors [5].

However, the durability of GaN-based systems is generally reduced due to variable operating conditions and related temperature or bias fluctuations. Therefore, these systems require real-time monitoring of the current load, as well as the temperature of active components, by incorporating external shunt resistors. Unfortunately, shunts dissipate power, leading to lower power density and efficiency [6], [7]. Circuit designers would greatly benefit from the ability to control and monitor circuit currents using monolithic integrated contactless current sensors [8]. These sensors should be capable of monitoring currents up to tens of amperes (i.e., magnetic fields in the order of tens of milliteslas) with an accuracy within a few percentage points [9], [10]. Therefore, Hall-effect current sensors could be a potential solution. In this letter, two common Hall plate topologies, implemented in enhancement-mode p-GaN technology, are experimentally characterized to assess potential limitations and tradeoffs.

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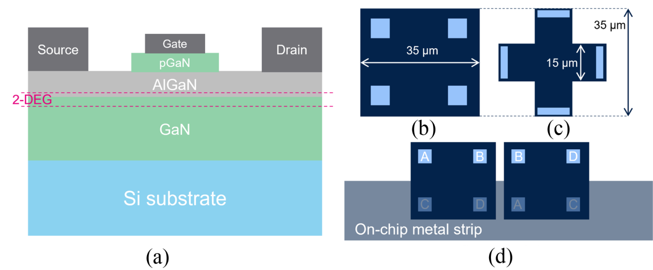

Fig. 1. (a) Cross section of a p-GaN over silicon technology. Top view of (b) square Hall plate and (c) cross Hall plate realized in this work. (d) Example of the pairing connection for the square Hall device with indication of the placement of the metal strip. Contacts with the same label are connected at the first metal level.

II. METHODOLOGY

A. Technology and Devices

Enhancement-mode p-GaN represents a promising technology because of the favorable tradeoff between reliability and cost. Indeed, standard silicon manufacturing technology and related facilities can be adapted to this new platform, ensuring a low cost of the fabrication process.

The enhancement-mode process by STMicroelectronics employed in this work features a p-type GaN (p-GaN) gate aluminium gallium nitride (AlGaN/GaN) HEMT grown by metal-organic chemical vapor deposition on a p-type Si substrate [cross-section in Fig. 1(a)]. The channel is composed of a low-C-doped ($\sim 10^{16}$ cm^{-3}) GaN layer. The AlGaN barrier layer features a 20%–22% Al concentration, and its thickness is in the 15–20-nm range. The p-type GaN layer is 100-nm thick, and has a nominal Mg doping concentration in the range of $10^{19} - 5 \times 10^{19}$cm^{-3}. To define the p-gate region, a Cl-based plasma

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etch was carried out [11]. The depletion region forming due to the p–i–n diode corresponding to the pGaN/AlGaN/GaN heterostructure effectively suppresses the bidimensional electron gas (2DEG) when no gate bias is applied, thus resulting in a positive threshold (normally off). Ohmic contacts were formed by Ti/Al-based metallization defined by means of a lift-off process [12]. The nominal 2DEG density and mobility are 8.6×10^{12} cm^{-2} and 1400 cm^2/(Vs), respectively [13].

For manufacturing the Hall devices, the Cl-based plasma etching of the p-GaN layer is extended across the whole area of the Hall plate. The Hall effect is realized on the 2DEG generated at the GaN–AlGaN interface by forcing a current through two electrodes while exposing the device to an off-plane magnetic field [14], [15]. The Lorentz force acts on the charge carriers, and the Hall voltage proportional to the magnetic field appears between two contacts orthogonal to the current flow. With respect to a Hall sensor realized in silicon technology, the GaN-based Hall sensor could operate at higher temperatures and extreme conditions. Moreover, it is not affected by the junction field effect [16], leading to a potentially low residual offset after the application of the spinning-current technique (SCT).

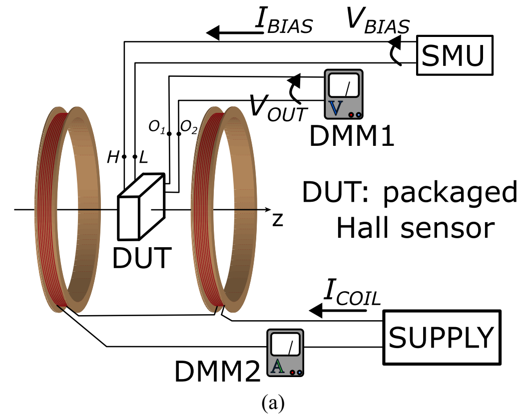
In this work, the two most popular Hall plate topologies [17] have been implemented, exploiting the 2DEG has sensing element. In the first topology, the 2DEG has been shaped as a square, and each of the four contacts has been placed in a corner of the square [see Fig. 1(b)]. The outer dimensions of the square are 35 µm × 35 µm (i.e., width $W = 35$ µm and length $L = 35$ µm). In the second topology, the 2DEG has been shaped as a cross, as depicted in Fig. 1(c). In this case, the outer dimensions of the sensor are 35 µm × 35 µm, while each branch of the cross is 15-µm wide (i.e., $W = 15$ µm, $L = 35$ µm). Both the topologies are fully symmetric, and each contact could be either used as a forcing or sensing contact. While the symmetric nature of the Hall plates in principle allows us to apply the SCT for offset reduction, it was not employed in this work [6], [18]. Each device-under-test (DUT) consists of two Hall plates of the same topology connected in parallel with a 90° relative spatial rotation, so to implement the pairing technique [19] [as shown in Fig. 1(d) for the square Hall plates]. In order to characterize the performance of the DUTs as integrated current sensors, an on-chip metal strip is realized on the top metal layer and placed above the DUTs, as shown in [6] and [20]. The DUTs are then packaged and placed on a printed circuit board for testing purposes.

B. Measurement Setup

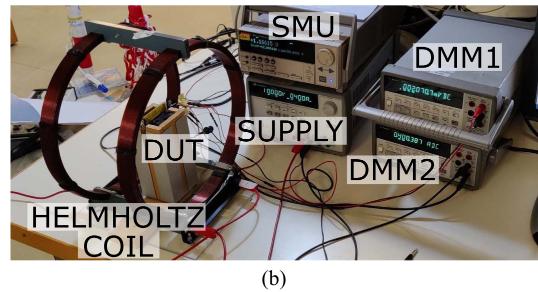
The block diagram and photo of the adopted measurement setup are shown in Fig. 2. A power supply (driven in current-limiting mode) is used to generate the measuring current flowing through the metal strip. In alternative, the same supply can be used to feed the Helmholtz coil which, in turn, will generate a predetermined magnetic field to be sensed by the DUT. A 6-1/2-digit Keysight 34 401 digital multimeter in ampermeter mode (DMM2 in Fig. 2) is placed in series to the power supply for an accurate measurement of the injected current. The DUT is biased in current-mode using a Keithley 2260B source-measure unit (SMU), which can accurately measure both the voltage and the current at the same port. The differential output voltage of the DUT is measured by means of a second Keysight 34401 (DMM1 in Fig. 2) configured in voltmeter mode.

III. EXPERIMENTAL RESULTS

Fig. 3 reports the static characteristics of both the topologies. These have been obtained by exciting the sensors with a uniform magnetic field created by the Helmholtz coil [see Fig. 3(a) and (b)] or by forcing a dc current to flow through the on-chip metal strip [see Fig. 3(c) and (d)]. The measured DUT output voltage is the sum of the Hall voltage V_H and the output-referred offset V_{OS}. The current bias value in Fig. 3 refers to the total bias current set by the SMU, which is uniformly divided between the two parallel Hall plates within the DUT.



(a)



(b)

Fig. 2. Block diagram (a) and photo (b) of the measurement setup.

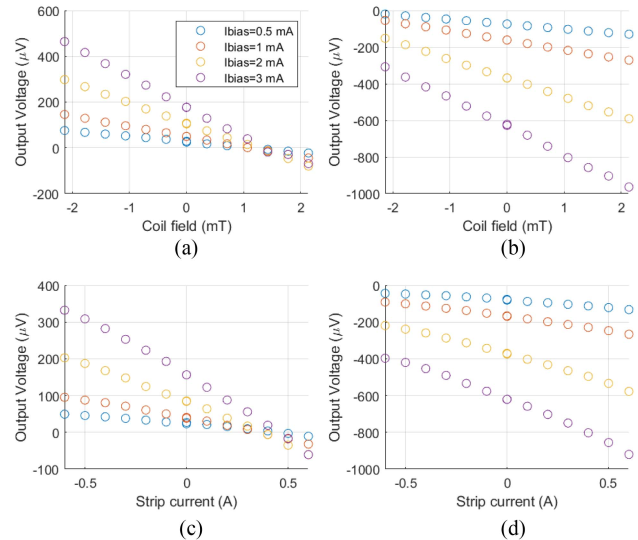


Fig. 3. Static characteristics measured at different values of I_{bias} by applying a uniform magnetic field on (a) square device and (b) cross device. Static characteristics measured at different values of I_{bias} by applying a controlled current on the on-chip metal strip for (c) square device and (d) cross device.

For the strip-based configuration case, the magnetic field has a non-negligible in-plane component, and the z-component of the field is not uniform over the device. The static characteristics in Fig. 3(c) and (d) display a nonlinearity error in the order of a few percentage points, likely related to the heat up of the Hall plate due to the Joule effect when high currents flow through the strip. Indeed, The

Table 1. State-of-the-Art Hall-Effect Sensors in AlGaN/GaN Technology.

Shape of the plate	Dimensions of the active area	Current-related Sensitivity $(\mathrm{VA^{-1}T^{-1}})$	Input-referred Magnetic Offset (mT)	Ref.
cross	$20\ \mu m \times 20\ \mu m$†	113	2‡	[21]
cross	$W = 1.5\ \mu m;\ L = 35\ \mu m$	65	0.8	[24]
octagon	$100\ \mu m$ (diameter)	68	1.4	[15]
modified octagon	$200\ \mu m$ hex diam + $70\ \mu m$ legs length	89	2–4	[18]
square	$W = 35\ \mu m;\ L = 35\ \mu m$	103	2	this work
cross	$W = 15\ \mu m;\ L = 35\ \mu m$	89	4–6	this work

†width of the cross branch not reported.
‡maximum value at 1 mA bias.

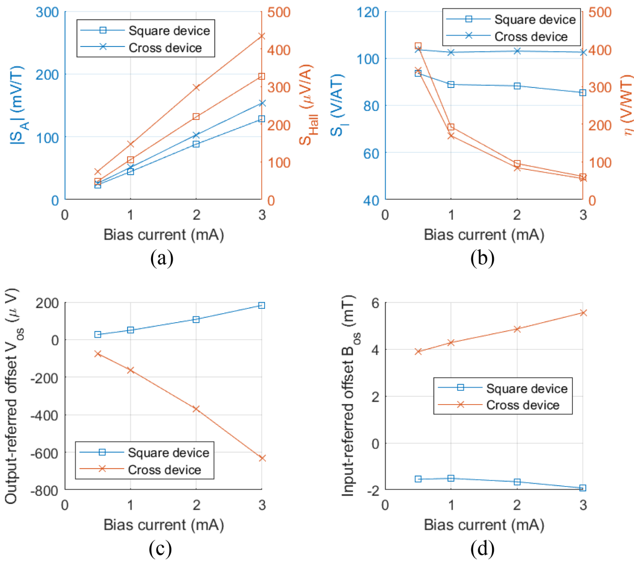


Fig. 4. (a) Estimated absolute sensitivity (blue lines) and estimated current-sensor gain expressed in $\mu V/A$ (orange line) of the square device (squares) and the cross device (crosses) as a function of the bias current. (b) Current-related sensitivity S_I in V/AT (blue line) and power-related sensitivity in V/WT (orange line) of the square device (squares) and the cross device (crosses) as a function of the bias current. (c) Output-referred offset V_{OS} and (d) input-referred magnetic offset B_{OS} for square and cross devices estimated from the coil-based tests.

metal strip is placed only a few micrometers away from the sensor, and it features a resistance on the order of tens of milliohms. This nonlinearity effect is a typical problem for Hall-effect sensors, which could yet be acceptable in the final sensor system [21]. Nevertheless, further analysis is required to quantify the temperature coefficient of the sensitivity and to consider the implementation of an active compensation technique.

The values for the sensitivity and offset are extracted from the static characteristics and then reported in Fig. 4 . In particular, the absolute sensitivity, defined as $S_A = V_H/B_z$, is extracted for the coil-based configuration. For the strip-based tests, the global sensitivity, defined as $S_{\mathrm{Hall}} = V_H/I_{\mathrm{in}}$, is instead extracted, where I_{in} is the current applied on the on-chip strip. Both the sensitivities display a linear dependency on the bias current I_{bias}, as expected from theory [22]. The global sensitivity S_{Hall} can be related to the absolute sensitivity S_A using the current-to-magnetic field transduction factor G_{IB} by means of the expression $S_{\mathrm{Hall}} = S_A G_{\mathrm{IB}}$ in [6]. A $G_{\mathrm{IB}} = 2.7$ mT/A for both the topologies can be estimated by comparing the values of S_A and S_{Hall}, which is coherent with values reported in the literature for Hall plates with on-chip metal strips [20], [23].

Since the absolute sensitivity depends on the value of I_{bias} [see Fig. 4(a)], the Hall plates are usually evaluated using the current-related

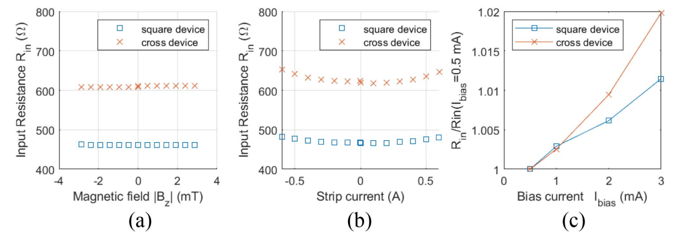


Fig. 5. Dependence of R_{in} on the magnetic field generated by (a) external magnetic source or (b) on-chip trace, at I_{bias}=2 mA. (c) Dependence of R_{in} on I_{bias} at zero-magnetic field. (a) $\mathrm{I_{bias}} = 2$ mA. (b) $\mathrm{I_{bias}} = 2$ mA. (c) $\mathrm{B_z} = 0$ T.

sensitivity $S_I = S_A/I_{\mathrm{bias}}$, which specifically pertains only to the Hall plate. The results reported in Fig. 4(b) refer to a single Hall plate, clearly showing that the cross-shaped device provides higher sensitivity with respect to the square-shaped one. This result is in agreement with both the general theory of Hall plates [22] as well as with studies on silicon Hall plates [17]. Indeed, the cross shape features higher L/W ratio and geometrical correction factor G_H, making it inherently more sensitive to the magnetic field. Another interesting figure-of-merit is the power-related sensitivity η, which express the energy efficiency of the device, namely, how much power is needed to create the same Hall voltage. In this respect, the two topologies are practically equivalent, given that the square device shows a lower input resistance.

The analysis of the additive offset V_{OS}, reported in Fig. 4(c), demonstrates that the square device performs better than the cross device, featuring a $\times 3$ to $\times 4$ reduction of the output offset. The sensitivity and the offset can be considered in a global way by evaluating the input-referred magnetic offset $B_{\mathrm{OS}} = V_{\mathrm{OS}}/S_A$, which can be seen as a general figure of merit. In general, B_{OS} is influenced by various technological and geometrical aspects, such as the shape and dimensions of the contacts and junction field effects [22]. Concerning the specific effect of the device's shape on the offset, the following relationship holds:

$$B_{\mathrm{OS}} \propto \frac{1}{W G_H}. \tag{1}$$

The cross device features a smaller width ($W = 15\,\mu\mathrm{m}$) with respect to the square device ($W = 35\,\mu\mathrm{m}$). At the same time, as per the literature [17], [22], the geometrical correction factor is approximately $G_H \simeq 0.9$ for the cross device and $G_H \simeq 0.7$ for the square device. Hence, the experimental results reporting a higher offset for the cross device are in agreement with the theoretical predictions.

The input resistance of the DUT $R_{\mathrm{in}} = V_{\mathrm{bias}}/I_{\mathrm{bias}}$ defines the required power to allow a certain bias current to flow through the device. Fig. 5 reports R_{in} as a function of the magnetic field and of the bias current. The square device shows a lower R_{in}, implying a better power efficiency. The analysis also shows that R_{in} is independent from the applied magnetic field when it is uniform and created from an external source [see Fig. 5(a)], while it displays a degree of dependence on

the field when the magnetic field is generated on-chip [see Fig. 5(b)]. This effect can be again due to thermal effects, or to parasitic magnetic effects related to the presence of a non-negligible in-plane magnetic field, yet further investigations are required to better understand this phenomenon. Finally, Fig. 5(c) shows a slight nonlinear behavior for R_{in} with respect to the bias current.

IV. CONCLUSION

A solution based on an Hall-effect GaN device for isolated dc–ac current sensing in GaN power systems has been presented. The devices were fabricated using the standard p-GaN enhancement-mode fabrication process by STMicroelectronics, ensuring low cost, and seamless integration.

Two different device topologies have been implemented and characterized, demonstrating performance in alignment with the literature, as reported in Table 1. The reported sensitivity values are comparable to silicon-based Hall plates; however, high-gain electronics will be required to amplify the signal. Although the cross-device shows higher sensitivity, the square device offers lower input resistance and lower additive offset, making it the device with the best energy efficiency and the lower input-referred magnetic offset. Concerning the offset, it should be highlighted that this characterization has been carried out on the bare Hall plates, whereas accurate offset compensation enabled by the SCT might allow for a substantial improvement for both topologies. The characterization also outlined the presence of nonideal phenomena when the Hall plate is used to detect the magnetic field generated by the current flowing through the on-chip metal trace. In this case, the nonlinear response of the current sensor, as well as the dependence of the input resistance on the applied field, have been reported.

The devices presented in this work can sense field amplitudes within the range required by the applications, although further developments are necessary to enhance the accuracy by increasing sensitivity and reducing offset. Additionally, a more comprehensive investigation of parasitic effects is required to enable their compensation.

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