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This is the final peer-reviewed author's accepted manuscript (postprint) of the following publication:

Published Version:
Baldisserri, S., Mandrioli, R., Neretti, G., Ricco, M., Cristofolini, A. (2025). Square-Wave-Fed Cockcroft-Walton Voltage Multipliers for Ionic Propulsion in Atmosphere. New York : IEEE [10.1109/ITEC63604.2025.11097961].

Availability:
This version is available at: https://hdl.handle.net/11585/1029391 since: 2025-11-20

Published:

DOI: http://doi.org/10.1109/ITEC63604.2025.11097961

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15 November 2026

Square-Wave-Fed Cockcroft-Walton Voltage Multipliers for Ionic Propulsion in Atmosphere

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***Abstract*—The development of high-power-density and efficient high-voltage DC/DC power electronic circuits plays a crucial role in ionic propulsion's potential employment. Traditional voltage multipliers (VMs) are typically fed by sinusoidal voltages delivered by a resonant converter coupled with a high-voltage step-up transformer. This paper explores a transformerless solution, achieved by feeding the VM directly with the inverter's square wave output voltage. Although requiring additional multiplier stages to get the same output voltage level, this configuration simplifies the implementation and could be suitable for size- and weight-sensitive applications. The performance and feasibility of the square-wave-fed VMs are evaluated, and it is demonstrated that lower output voltage ripple and drop and better system dynamic response are achieved with this approach.**

***Index Terms*—DC high voltage, high power density, ionic propulsion, output voltage regulation, square wave, voltage multiplier**

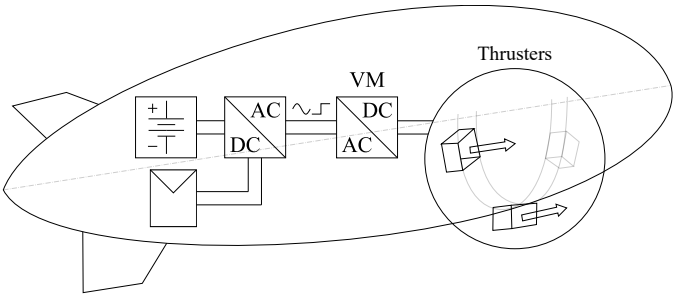


Fig. 1: Main power converters for an airship-based ionic propulsion in atmosphere.

I. Introduction

Advances in ionic propulsion technology are leading to developments in several fields, including aviation, climate monitoring, telecommunications, and other stratospheric missions [1], [2]. The development of high-power-density and efficient high-voltage power electronic circuits plays a crucial role in the ion thrusters' potential employment [3], [4]. As visible in Fig. 1, DC/DC power converters used in this type of application usually consist of three stages: a resonant and/or multilevel inverter (i.e., DC/AC), an isolation step-up high-voltage high-frequency transformer, and a rectification stage (i.e., AC/DC) [5]. Typical applications require for output voltages and powers in the order of about 10-30 kV and 0.1-1 kW respectively.

IPROP project has received funding from the European Union's Horizon Europe Research and Innovation Programme under grant agreement No 101098900. Views and opinions expressed are however those of the authors only and do not necessarily reflect those of the European Union or EISMEA. Neither the European Union nor the granting authority can be held responsible for them.

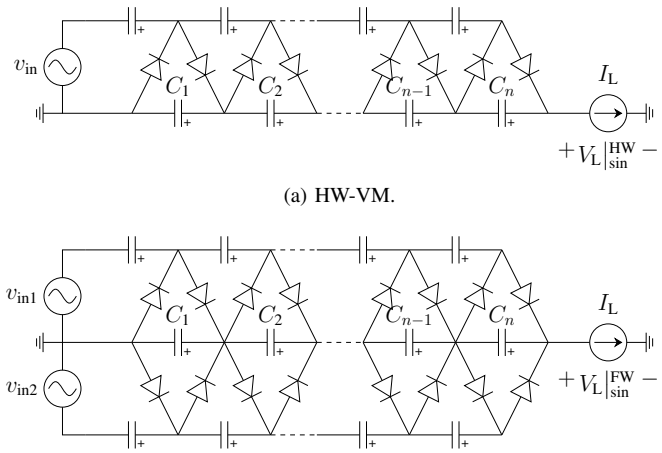
The rectification stage is commonly realized by means of a voltage multiplier (VM). VMs consisting of a cascaded configuration of diodes and capacitors are widely used because capable to provide a significantly high voltage step-up ratio without employing active devices and thus floating supplies [6]–[8]. First introduced by Villard in 1901 and Greinacher in 1921, the VM circuit gained significant recognition in 1932 when Cockcroft and Walton employed it to achieve the first artificial nuclear disintegration [9]–[11]. The original VM, a half-wave (HW) configuration, suffered from several drawbacks, including high output voltage ripple and drop. To mitigate these limitations, Heilpern proposed the full-wave (FW) topology in 1954, also called symmetrical VM, adding an oscillating column of capacitors and a stack of diodes [12]–[16]. While the FW-VM design significantly reduced ripple and voltage drop, it introduced new challenges, such as the need for a high-voltage transformer with center-tapped secondary windings, increasing the system complexity and bill of material [17].

Till now, VMs have been analyzed by considering a sine wave input voltage, typically supplied by a high-voltage transformer [18]. This approach, however, introduces significant weight and complexity into the overall system, due to the transformer and the related resonant tank [19]. This paper explores a transformerless solution, achieved by feeding the VM directly with the inverter's square wave output voltage. The behaviour of the HW- and FW-VMs is investigated, analyzing performance and feasibility in high-voltage systems. The square-wave-fed configuration requires a higher number of multiplier stages to achieve the same output voltage level, but potentially avoids the transformer. The results demonstrate that lower output voltage ripple and drop are achieved with this approach, and could pave the way for a weight trade-off and a simplified system design in fields where size and weight are critical constraints. The use of a square wave input voltage introduces challenges, such as current spikes due to faster capacitive transients. Although these spikes can have an impact on component stress, they are manageable given the typical low currents of these applications.

The rest of the manuscript is organized as follows: a background on sine-wave-fed HW- and FW-VMs is provided in Section II, while the proposed square-wave-fed VMs are introduced in Section III. Section IV presents the numerical validation, and Section V draws conclusions.

II. Background on Sine-Wave-Fed HW- and FW-VMs

Fig. 2a represents the HW-VM introduced in [11] while Fig. 2b represents the FW-VM introduced in [12] and [13]. The n-stage HW-VM is driven by an input AC voltage source $v_{\text{in}} = V_{\text{in}} \sin(\omega t)$ and consists of one oscillating column of capacitors, one smoothing column of capacitors $(C_1, C_2, ..., C_n)$, and a stack of diodes. The n-stage FW-VM is driven by a pair of phase-shifted AC voltage sources $v_{\text{in1}} = V_{\text{in}} \sin(\omega t)$ and $v_{\text{in2}} = V_{\text{in}} \sin(\omega t - \pi)$, commonly obtained by using a transformer with center-tapped secondary windings. It includes an additional oscillating column of capacitors and a stack of diodes.



(a) HW-VM.

(b) FW-VM.

Fig. 2: Sine-wave-fed VMs with n stages.

In steady-state operations, the capacitors of the smoothing column are charged in parallel by the oscillating columns and discharged in series through the load. The latter, for ease, is considered as a constant current I_{L}. The total output voltage V_{L} is the sum of the smoothing column capacitors' voltages. For the sake of simplicity, it is assumed that the capacitance of each capacitor is equal to C [13]–[18], [20]–[22].

From now on, the notation $|^{\text{HW/FW}}_{\text{sin/sq}}$ will be used; the subscript refers to the input voltage waveform (i.e., "sin" and "sq" in case of sine or square waves respectively) type while the superscript refers to the voltage multiplier topology (i.e., "HW" or "FW" in case of HW-VM or FW-VM respectively). The key steady-state waveforms of the VMs are depicted in Fig. 3. At no load, with $I_{\text{L}} = 0$, each capacitor of the smoothing column charges up to $2V_{\text{in}}$, where V_{in} is the maximum value of the input voltage v_{in}. Thus, the total output voltage at no load is $V_{\text{L}}|^{\text{HW}}_{\text{sin}} = V_{\text{L}}|^{\text{FW}}_{\text{sin}} = 2nV_{\text{in}}$, where n is the number of stages. If a load current $I_{\text{L}} > 0$ is drawn through the output terminal of the multiplier circuits, a voltage ripple $\hat{V}_{\text{L}}$ and drop ΔV_{L} will occur across the capacitors of the oscillating columns and, consequently, across the capacitors of the smoothing column. The voltage drop across diodes is considered negligible in this analysis, as frequently done in literature [13]–[18], [20]–[22].

From Fig. 3 it can be noted that thanks to the additional oscillating column, the output voltage of the FW-VM presents an half-wave symmetry, therefore its analysis can be limited to the half period $T/2$; $f = 1/T = \omega/2\pi$. The latter statement does not apply to the HW-VM, which requires to be studied considering the whole period $T = 1/f$ because lacking half-wave symmetry.

A. Analysis of the Sine-Wave-Fed HW-VM

The output voltage ripple and drop of the sine-wave-fed HW-VM is the sum of the voltage ripples and drops of the smoothing column capacitors, respectively, resulting in:

$$\begin{aligned} \hat{V}_{\text{L}}|^{\text{HW}}_{\text{sin}} &= \frac{q}{C}\frac{n(n+1)}{2} \\ \Delta V_{\text{L}}|^{\text{HW}}_{\text{sin}} &= \frac{q}{C}\left(\frac{2}{3}n^3 + \frac{n^2}{2} - \frac{n}{6}\right) \end{aligned}, \tag{1}$$

where $q = I_{\text{L}}/f$ is the load charge within the time T [20]–[22].

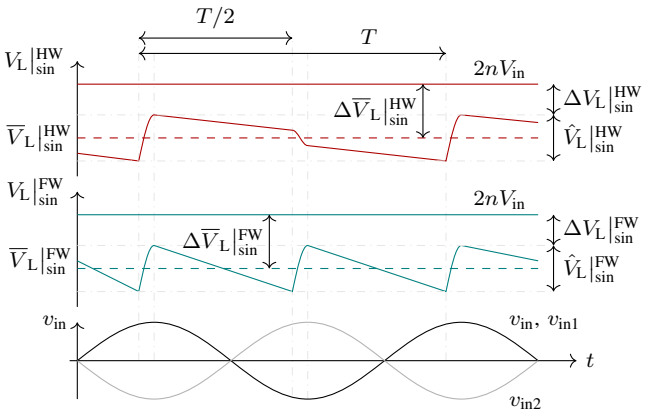


Fig. 3: Key steady-state waveforms of the sine-wave-fed VMs.

As visible in Fig. 3, the average output voltage of the VM circuits can be determined, after calculating the output voltage ripple and drop, as $\overline{V}_{\rm L} = V_{\rm L} - \Delta\overline{V}_{\rm L} = V_{\rm L} - (\Delta V_{\rm L} + \hat{V}_{\rm L}/2)$, where $\Delta\overline{V}_{\rm L}$ indicates the average output voltage drop.

Regarding the sine-wave-fed HW-VM, the average output voltage can be computed from (1) as:

$$\overline{V}_{\rm L}\big|_{\rm sin}^{\rm HW} = 2nV_{\rm in} - \frac{q}{C}\left(\frac{2}{3}n^3 + \frac{3}{4}n^2 + \frac{n}{12}\right) . \tag{2}$$

B. Analysis of the Sine-Wave-Fed FW-VM

The output voltage ripple and drop of the sine-wave-fed FW-VM is the sum of the voltage ripples and drops of the smoothing column capacitors:

$$\begin{aligned} \hat{V}_{\rm L}\big|_{\rm sin}^{\rm FW} &= \frac{q}{C}n \\ \Delta V_{\rm L}\big|_{\rm sin}^{\rm FW} &= \frac{q}{C}\left(\frac{n^3}{3} + \frac{n^2}{2} + \frac{n}{6}\right) , \end{aligned} \tag{3}$$

where $q = I_{\rm L}/(2f)$ is the charge transferred to the load within half a period $T/2$ [12]–[18].

Following the same principle as the HW-VM, the average output voltage drop of the sine-wave-fed FW-VM can be computed from (3) as:

$$\overline{V}_{\rm L}\big|_{\rm sin}^{\rm FW} = 2nV_{\rm in} - \frac{q}{C}\left(\frac{n^3}{3} + \frac{n^2}{2} + \frac{2}{3}n\right) . \tag{4}$$

Clearly, FW-VMs present lower voltage drops compared to HW-VMs. This can be verified comparing (4) and (2).

III. Proposed Square-Wave-Fed HW- and FW-VMs

Fig. 4 displays the key steady-state waveforms of the square-wave-fed HW- and FW-VMs, while Fig. 5 and Fig. 6 represent the main operating principle. Thanks to the half-wave symmetry of the FW-VM output voltage, Fig. 6 represents the working principle of the FW-VM only during the first half of the period, as in the second one the operation is symmetrical. At no load, with $I_{\rm L} = 0$, the operating principle is the same as in the sine-wave-fed VMs. Consequently, the total output voltage at no load is $V_{\rm L}\big|_{\rm sq}^{\rm HW} = V_{\rm L}\big|_{\rm sq}^{\rm FW} = 2nV_{\rm in}$. If a load current $I_{\rm L} > 0$ is drawn through the output terminal of the multiplier circuits, the square-wave-fed VMs behave differently from the sinusoidal case.

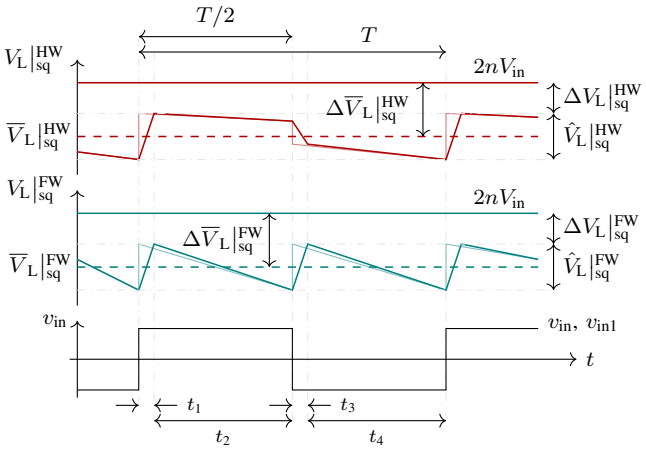
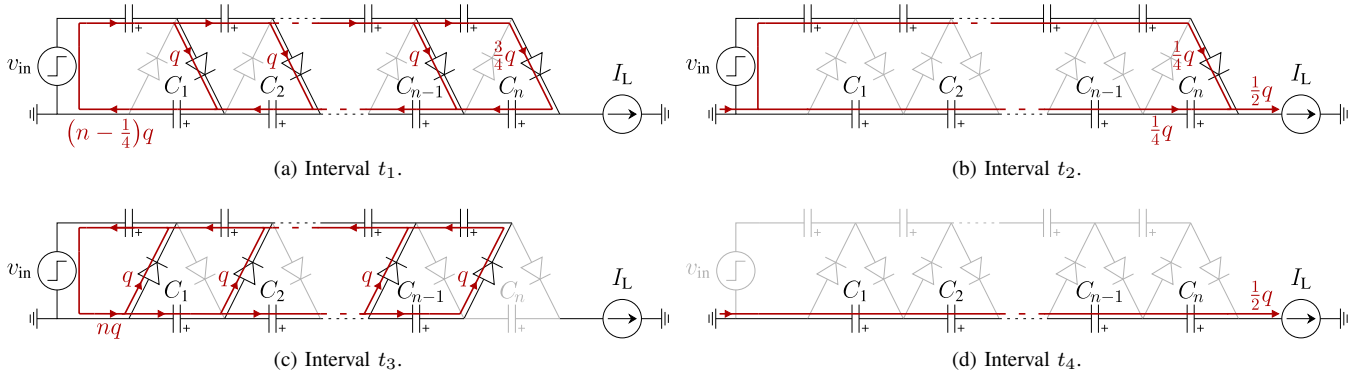


Fig. 4: Key steady-state waveforms of the square-wave-fed VMs.



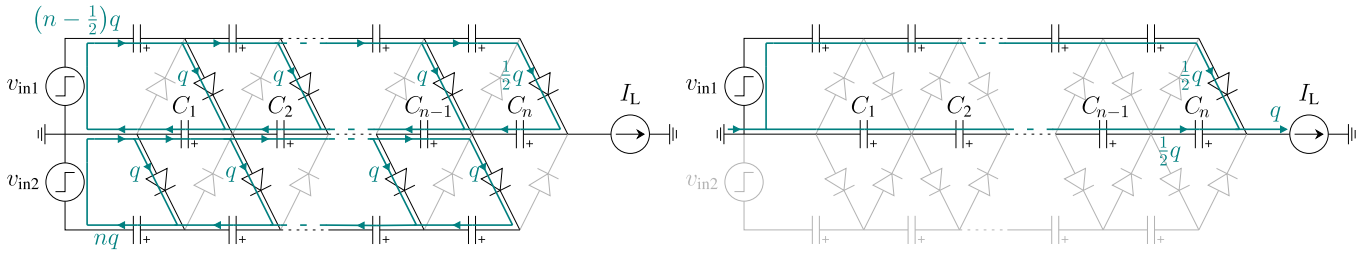
(a) Interval t_1.

(b) Interval t_2.

(c) Interval t_3.

(d) Interval t_4.

Fig. 5: Operating principle of the square-wave-fed HW-VM during time intervals t_1, t_2, t_3, and t_4.



(a) Interval t_1.

(b) Interval t_2.

Fig. 6: Operating principle of the square-wave-fed FW-VM during time intervals t_1 and t_2.

Generally, four time intervals within a period T can be distinguished:

- t_1 – the smoothing column capacitors are charged by the upper oscillating column;
- t_2 – the smoothing and oscillating column capacitors are discharged through the load;
- t_3 – in the HW-VM the oscillating column is charged by the smoothing column, while in the FW-VM the smoothing column is charged by the lower oscillating column;
- t_4 – the smoothing and, only for the FW-VM, the oscillating column capacitors are discharged through the load.

As frequently done in literature, to analyze the VM circuits it can be assumed that the time intervals $t_1 \ll T$ and $t_3 \ll T$ [13]–[18], [20]–[22]. Therefore, the charging processes (i.e., t_1 and t_3) are considered instantaneous and the discharging processes last $t_2 = t_4 = T/2$. This allows the portion of charge supplied to the load during the charging intervals t_1 and t_3 to be neglected, and consider the load supplied only during intervals t_2 and t_4. Furthermore, this allows to obtaining of generic formulations that can give good approximation results regardless of the actual charging transients. The key steady-state waveforms modified according to this approach are shown in mild colors in Fig. 4.

Considering the periodicity of the HW- and FW-VM discussed in Section II, and assuming that $q = I_{\mathrm{L}}/f$ is the charge transferred to the load by each capacitor of the smoothing column of the HW-VM in a period T, with a simple power balance equation it can be obtained that the charge supplied by the source in time T is $q_{\mathrm{in}} = 2nq$, as can also be deduced from Fig. 5. The same applies to the FW-VM considering half a period $T/2$, then $q = I_{\mathrm{L}}/(2f)$, and can be verified from Fig. 6.

The main difference from the sine wave case is that during t_2 the input voltage is constant. This causes the conduction of the diode in the last stage of the multiplier chain, as shown in Fig. 5b and Fig. 6b. It is easy to demonstrate that the charge supplied to the load during t_2 is equally shared between the smoothing and oscillating column capacitors. It should first be noted that the first capacitors of the oscillating columns are charged up to V_{in}, while all the other oscillating and smoothing capacitors are charged up to $2V_{\mathrm{in}}$. This can be deduced from the Kirchhoff's voltage law during diode conduction intervals displayed in Fig. 5 and Fig. 6. As a result, the circuits are capacitive current dividers where the impedances of the two branches are equal.

During t_4, the diode in the last stage of the HW-VM is reverse-biased. Consequently, the charge is supplied to the load only by the smoothing column capacitors. This is visible in Fig. 4, where the output voltage slope, which depends only on the smoothing column capacitors, during t_4 is twice the one during t_2. On the other hand, in the FW-VM, during t_4 the lower oscillating column capacitors supply the load together with the smoothing column capacitors.

In-depth analysis of square-wave-fed HV- and FW-VMs is reported in Subsections III-A and III-B.

A. Analysis of the Square-Wave-Fed HW-VM

The output voltage ripple is produced due to the periodic charging and discharging of the smoothing column capacitors. During t_2, t_3, and t_4 the smoothing column capacitors of the HW-VM discharge, while during t_1 these capacitors are charged back of the full amount of the charge lost in the previous intervals. Consequently, the output voltage ripple and drop of the HW-VM can be evaluated just by considering the interval t_1. This aspect is displayed in Fig. 4. The output voltage ripple of the square-wave-fed HW-VM is obtained by summing the individual voltage ripples of each smoothing column capacitor, which can be deduced from Fig. 5a, as:

$$\hat{V}_{\mathrm{L}}\big|_{\mathrm{sq}}^{\mathrm{HW}} = \frac{q}{C}\sum_{i=1}^{n}\left(i-\frac{1}{4}\right) = \frac{q}{C}\left(\frac{n^2}{2}+\frac{n}{4}\right) . \tag{5}$$

The output voltage drop can be determined by summing the individual voltage drops of each smoothing column capacitor. Although the first oscillating capacitor C_1' is charged up to $V_{C_1'} = V_{\mathrm{in}}$ during t_3, if ideal diodes and no voltage drop within the source are assumed, it cannot charge C_1 during t_1 above:

$$V_{C_1} = 2V_{\mathrm{in}} - \frac{q}{C}\left(n-\frac{1}{4}\right) , \tag{6}$$

as C_1 has lost a total charge of $[1/4+(n-1)+1/2]q = (n-1/4)q$ during the previous full cycle, and must be charged back of the same amount. Then C_1, that is discharged of $[1/4+(n-1)]q$ during t_2 and t_3, respectively, cannot charge during t_3 the second oscillating capacitor C_2' to a voltage greater than:

$$\begin{aligned} V_{C_2'} &= 2V_{\mathrm{in}} - \frac{q}{C}\left[\left(n-\frac{1}{4}\right)+\frac{1}{4}+(n-1)\right] \\ &= 2V_{\mathrm{in}} - \frac{q}{C}[n+(n-1)] . \end{aligned} \tag{7}$$

Moreover, during the previous full cycle, C_2 has lost a total charge of $[1/4+(n-2)+1/2]q = [(n-1)-1/4]q$. Capacitor C_2' charges it back of the same amount during t_1. Consequently, C_2 cannot be charged to a voltage greater than:

$$V_{C_2} = 2V_{\mathrm{in}} - \frac{q}{C}\left[\left(n-\frac{1}{4}\right)+2(n-1)\right] . \tag{8}$$

This applies to all the following capacitors till C_n, which cannot be charged to a voltage greater than:

$$V_{C_n} = 2V_{\mathrm{in}} - \frac{q}{C}\left[\left(n-\frac{1}{4}\right)+2(n-1)+\ldots+2(1)\right] . \tag{9}$$

By summing all the obtained contributions it is possible to derive the general formula for the output voltage drop of the square-wave-fed HW-VM:

$$\Delta V_{\mathrm{L}}\big|_{\mathrm{sq}}^{\mathrm{HW}} = \frac{q}{C}\left[\left(n-\frac{1}{4}\right)n+\sum_{i=1}^{n-1}2i^2\right] = \frac{q}{C}\left(\frac{2}{3}n^3+\frac{n}{12}\right) . \tag{10}$$

The average output voltage of the square-wave-fed HW-VM can be calculated from (5) and (10), as:

$$\overline{V}_{\mathrm{L}}\big|_{\mathrm{sq}}^{\mathrm{HW}} = 2nV_{\mathrm{in}} - \frac{q}{C}\left(\frac{2}{3}n^3+\frac{n^2}{4}+\frac{5}{24}n\right) . \tag{11}$$

B. Analysis of the Square-Wave-Fed FW-VM

Considering the previously stated assumptions regarding the half-wave symmetry of the FW-VM, in the following analysis only half a period including time intervals t_1 and t_2 will be analyzed in the following.

Each smoothing column capacitor of the FW-VM transfers to the load a charge $q/2$ in time t_2. During t_1 they are charged back of the same amount. Therefore, the peak-to-peak ripple produced across each smoothing column capacitor is $q/(2C)$. The output voltage ripple of the FW-VM is obtained by summing the voltage ripples of each smoothing column capacitor as:

$$\hat{V}_{\mathrm{L}}|_{\mathrm{sq}}^{\mathrm{FW}} = \frac{q}{2C} n \ . \tag{12}$$

The output voltage drop can be determined by summing the individual voltage drops of each smoothing column capacitor. Following the same procedure as for HW-VM, during t_1, the first upper oscillating capacitor C_1' charges the smoothing capacitor C_1, which consequently can not have a voltage greater than:

$$V_{C_1} = 2V_{\mathrm{in}} - \frac{q}{C}\left(n - \frac{1}{2}\right) \ . \tag{13}$$

This applies to all the capacitors in the smoothing column. Given that capacitor C_n is charged by the whole upper oscillating column, his maximum voltage results to be:

$$V_{C_n} = 2V_{\mathrm{in}} - \frac{q}{C}\left[\left(n - \frac{1}{2}\right) + \left(n - \frac{3}{2}\right) + ... + \frac{1}{2}\right] \ , \tag{14}$$

and by summing all the obtained contributions it is possible to compute the general formula for the output voltage drop of the square-wave-fed FW-VM:

$$\Delta V_{\mathrm{L}}|_{\mathrm{sq}}^{\mathrm{FW}} = \frac{q}{C}\left(-\frac{1}{2}\sum_{i=1}^{n} i + \sum_{i=1}^{n} i^2\right) = \frac{q}{C}\left(\frac{n^3}{3} + \frac{n^2}{4} - \frac{n}{12}\right) . \tag{15}$$

The average output voltage of the square-wave-fed FW-VM can be calculated from (12) and (15), as:

$$\overline{V}_{\mathrm{L}}|_{\mathrm{sq}}^{\mathrm{FW}} = 2nV_{\mathrm{in}} - \frac{q}{C}\left(\frac{n^3}{3} + \frac{n^2}{4} + \frac{n}{6}\right) \ . \tag{16}$$

IV. Numerical Validation

The sine- and square-wave-fed HW- and FW-VMs are simulated on PLECS (Plexim GmbH) environment considering an input voltage of 1 kV, a switching frequency of 50 kHz, a load current of 0.1 A, and capacitances of 1 μF. Diodes with an on-resistance of 10 mΩ are considered in the simulations.

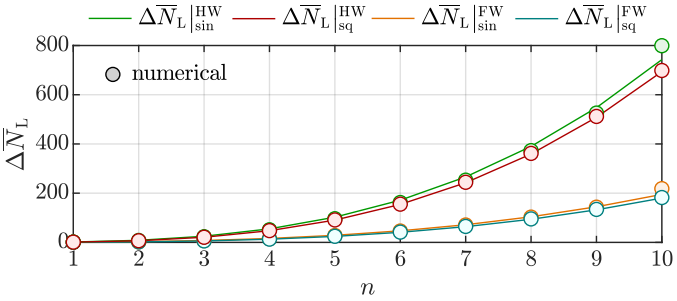


Fig. 7: Numerical validation of the normalized average output voltage drop $\Delta\overline{N}_{\mathrm{L}}$ as a function of the total number of stages n for sine- and square-wave-fed HW- and FW-VMs.

Fig. 7 shows the normalized average output voltage drop $\Delta\overline{N}_{\mathrm{L}} = -(\overline{V}_{\mathrm{L}} - 2nV_{\mathrm{in}})/(q/C) = \Delta\overline{V}_{\mathrm{L}}/(q/C)$ of the described VMs as a function of the total number of stages n. Considering the same charge transferred to the load q and capacitance value C, the normalized average output voltage drop $\Delta\overline{N}_{\mathrm{L}}$ is representative of the whole average output voltage drop $\Delta\overline{V}_{\mathrm{L}}$. It can be noticed that the square-wave-fed VMs turn out to have lower average output voltage drop, thus better output voltage regulation. Overall, the FW-VM has better performance than the HW-VM, as well known in literature [18]. As visible, numerical results (circles) fairly match the analytical predictions (solid traces).

Moreover, the absolute error ε_{A} and relative error ε_{R} between numerical results and analytical prediction of the normalized average output voltage drop $\Delta\overline{N}_{\mathrm{L}}$ of both square-wave-fed VMs is computed and listed in Table I. As the number of stages n increases, ε_{A} increases. This is because the number of diodes in the VM increases, as well as the total voltage drop across them. A constant current is assumed, thus a constant voltage drop across diodes. Therefore, it can be observed as a general trend that ε_{R} decreases as the output voltage increases. In fact, by increasing the number of stages, the assumption of neglecting the diode voltage drop acquires validity. Although the voltage drop across diodes is not taken into account in the analysis, ε_{R} is anyway lower than 5%, especially for high n values, therefore validating (11) and (16).

Fig. 8 shows the dynamic response in time of the sine- and square-wave-fed HW- and FW-VMs for different numbers of stages n. It can be noted that the square-wave-fed VMs present a faster transient response with respect to the sine-wave-fed ones. Furthermore, as the number of stages, and thus the output voltage, changes, the transient slope does not change. Eventually, it can be verified from Fig. 8 that the FW-VM has a lower output voltage drop and a faster dynamic response than the HW-VM.

TABLE I: Absolute error ε_{A} and relative error ε_{R} in % between numerical results and analytical prediction of the normalized average output voltage drop $\Delta\overline{N}$ of the square-wave-fed HW- and FW-VMs with n from 1 to 10.

	n	1	2	3	4	5	6	7	8	9	10
HW-VM	ε_{A}	0.0621	0.0686	0.0468	0.287	0.584	1.18	1.91	2.67	3.69	4.75
	ε_{R}	5.52%	1.02%	0.224%	0.604%	0.644%	0.762%	0.789%	0.745%	0.726%	0.685%
FW-VM	ε_{A}	0.0167	0.0858	0.186	0.328	0.517	0.782	1.03	1.40	1.69	2.29
	ε_{R}	4.46%	4.29%	3.17%	2.52%	2.12%	1.91%	1.62%	1.48%	1.28%	1.27%

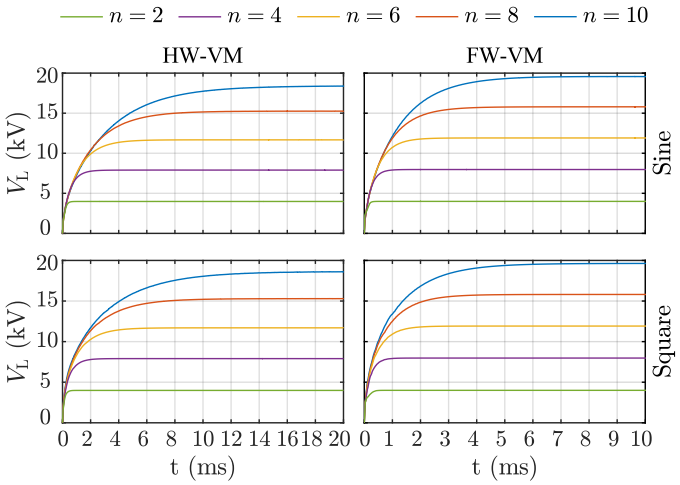


Fig. 8: Dynamic response of the sine- and square-wave-fed HW- and FW-VM for different number of stages n.

V. Conclusion

The analysis of the square-wave-fed HW- and FW-VM has been proposed in this paper. The different operating principles with respect to the traditional sine wave approach have been highlighted, and the results show that lower output voltage ripple and drop and faster system's dynamic response are achieved. The feasibility of this solution has been numerically validated by simulations. Although the voltage drop across diodes is not taken into account in the analytical analysis, the relative error between numerical results and analytical prediction is lower than 5%, especially for a high number of stages, therefore validating the analysis. This approach could pave the way for high-power-density and efficient designs for size- and weight-sensitive applications.

Future works can include the voltage drop across diodes in the analytical developments and the experimental validation of the proposed approach. Furthermore, the power density of the sine- vs square-wave-fed systems is still an open point to be studied.

References

[1] D. Lev, R. M. Myers, K. M. Lemmer, J. Kolbeck, H. Koizumi, and K. Polzin, "The technological and commercial expansion of electric propulsion," *Acta Astronautica*, vol. 159, pp. 213–227, 2019.

[2] H. Xu, Y. He, K. L. Strobel, C. K. Gilmore, S. P. Kelley, C. C. Hennick, T. Sebastian, M. R. Woolston, D. J. Perreault, and S. R. H. Barrett, "Flight of an aeroplane with solid-state propulsion," *Nature*, vol. 563, no. 7732, pp. 532–535, Nov 2018.

[3] C. E. D. Riboldi, M. Belan, S. Cacciola, R. Terenzi, S. Trovato, D. Usuelli, G. Familiari *et al.*, "Preliminary sizing of high-altitude airships featuring atmospheric ionic thrusters: An initial feasibility assessment," *Aerospace*, vol. 11, no. 7, pp. 1–26, 2024.

[4] L. Zhang, W. Zhu, H. Du, and M. Lv, "Multidisciplinary design of high altitude airship based on solar energy optimization," *Aerospace Science and Technology*, vol. 110, p. 106440, 2021.

[5] Y. He and D. J. Perreault, "Lightweight high-voltage power converters for electroaerodynamic propulsion," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 2, no. 4, pp. 453–463, 2021.

[6] M. M. Weiner, "Analysis of cockcroft-walton voltage multipliers with an arbitrary number of stages," *Review of Scientific Instruments*, vol. 40, no. 2, pp. 330–333, 1969.

[7] P. Lin and L. Chua, "Topological generation and analysis of voltage multiplier circuits," *IEEE Transactions on circuits and systems*, vol. 24, no. 10, pp. 517–530, 1977.

[8] M. D. Bellar, E. Watanabe, and A. Mesquita, "Analysis of the dynamic and steady-state performance of cockcroft-walton cascade rectifiers," *IEEE transactions on power electronics*, vol. 7, no. 3, pp. 526–534, 1992.

[9] P. Villard, "Transformateur à haut voltage. a survolteur cathodique," *Journal de Physique Théorique et Appliquée*, vol. 10, no. 1, pp. 28–32, 1901.

[10] H. Greinacher, "Über eine methode, wechselstrom mittels elektrischer ventile und kondensatoren in hochgespannten gleichstrom umzuwandeln," *Zeitschrift für Physik*, vol. 4, no. 2, pp. 195–205, 1921.

[11] J. D. Cockcroft and E. T. Walton, "Experiments with high velocity positive ions," *Proceedings of the royal society of London. Series A, containing papers of a mathematical and physical character*, vol. 129, no. 811, pp. 477–489, 1930.

[12] W. Heilpern, "Kaskadengeneratoren zur partikelbeschleunigung auf 4 mev," *Helv. phys. acta*, vol. 28, no. 5, pp. 485–491, 1955.

[13] G. Reinhold, K. Truempy, and J. Bill, "The symmetrical cascade rectifier an accelerator power supply in the megavolt and milliampere range," *IEEE Transactions on Nuclear Science*, vol. 12, no. 3, pp. 288–292, 1965.

[14] S. Iqbal, "A three-phase symmetrical multistage voltage multiplier," *IEEE Power Electronics Letters*, vol. 3, no. 1, pp. 30–33, 2005.

[15] S. Iqbal, G. Singh, R. Besar, and G. Muhammad, "A cascaded three-phase symmetrical multistage voltage multiplier," *Journal of Instrumentation*, vol. 1, no. 10, p. T10001, 2006.

[16] H. Zhang and A. Takaoka, "Efficient compensation method for reducing ripple of cockcroft–walton generator in an ultrahigh-voltage electron microscope," *Review of scientific instruments*, vol. 65, no. 10, pp. 3194–3198, 1994.

[17] ——, "Fundamental harmonic of ripples in symmetrical cockcroft-walton cascade rectifying circuit," *Review of scientific instruments*, vol. 67, no. 9, pp. 3336–3337, 1996.

[18] M. Ruzbehani, "A comparative study of symmetrical cockcroft-walton voltage multipliers," *Journal of Electrical and Computer Engineering*, vol. 2017, no. 1, p. 4805268, 2017.

[19] Y. He and D. J. Perreault, "Lightweight high-voltage power converters for electroaerodynamic propulsion," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 2, no. 4, pp. 453–463, 2021.

[20] J. Kuffel and P. Kuffel, *High voltage engineering fundamentals*. Elsevier, 2000.

[21] M. Abdel-Salam, *High-voltage engineering: theory and practice, revised and expanded*. CRC Press, 2000.

[22] C. Wadhwa, *High voltage engineering*. New Age International, 2007.