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Synchronous Switching Scheme - Bringing Modular Fault Tolerance to Power Converters

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ABSTRACT Various critical applications in domains such as electric vehicles, space technology, defence, data-centers and microgrids require high power, uninterruptible and high reliability power electronic converters. This paper focusses on developing a highly modular and topology independent fault tolerant approach, making it an attractive solution for industrial applications. The paper validates the proposed approach through PLECS simulation of a 400 V and 5 kW full-bridge forward converter, and performs hardware validation at 400 V DC bus voltage as well. Further, the paper thoroughly analyses the losses, efficiency, reliability and mean time to failure of the proposed fault tolerance solution, and proves its effectiveness across various key factors in comparison to existing approaches in literature.

INDEX TERMS DC-DC converters, fault tolerance, reliability, isolated power converters, modularity.

I. INTRODUCTION

Power electronics in current times has proven to be an integral part of multiple domains involving energy generation, storage, transfer, and consumption. At larger scales, solar PV generation [1] and wind energy generation [2] have proven to be the biggest contributors to distributed energy generation. This has led to a demand for high-power converters for energy conversion applications [3], [4]. Similarly, battery energy storage systems and their power converter technologies have seen tremendous growth in grid-connected applications [5]. The increasing popularity of microgrids has further popularised distributed energy generation and storage technologies [6]. These microgrids tend to be interfaced through various topologies of power converters to high voltage DC (HVDC) [7] and medium voltage DC [8] transmission networks. Further, rapid adoption of technologies such as electric vehicles [9], green hydrogen generation [10], and more electric aircrafts [11], all highlight the irreplaceable role of power electronics in our lives.

Thus, to ensure uninterrupted flow and conversion of power, the reliable operation of power converters becomes paramount. This highlights the importance of research and development in the domains of fault detection, fault-tolerant converter topologies, as well as reliability analysis. A recent study showed, with the example of a resonant converter, that the most vulnerable component of the power converter is the primary side semiconductors, followed by resonant capacitors, the control system, and finally the secondary side semiconductors [12]; vulnerability distribution is depicted in Fig. 1. Due to the rise of wide-band-gap semiconductors, SiC MOSFETs have become a popular choice for primary side devices [13]. MOSFET failure can occur due to various factors, such as long-term thermal cycling, high di/dt and dv/dt stresses, high ambient operating temperatures, and high heat dissipation, which become more and more common as power converters reach higher power transfer capacities and high power densities. Thermal cycling plays a significant role in the long-term ageing of power semiconductor devices, due to

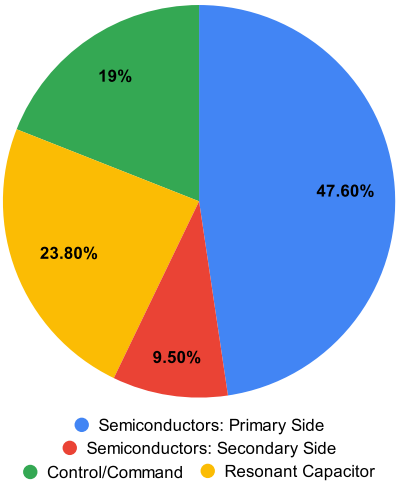


FIGURE 1. Device vulnerability to failure for an SRC/LLC converter [12].

the differences in the thermal expansion coefficients of various materials used in the fabrication of these devices [14].

Fault detection and identification are crucial steps in developing fault-tolerant approaches for power converters. Common fault detection methods may be grouped into hardware-based, model-based, and historic data-based fault detection [15]. Hardware-based detection methods employ additional sensors for measuring relevant parameters of the power converter, whose data is then used to determine whether a fault has occurred or not. The model-based method focuses on developing a mathematical model of the power converter under observation. Any deviations in the behaviour of the power converter from the mathematical model are then used to identify the fault condition. A historical data-based approach relies on previously recorded data of the power converter's input and output parameters. These are combined with a multitude of soft computing techniques for the identification of faults within the converter.

Fault tolerance can be described as the ability of a power converter to deliver uninterrupted power from its input to its output, even during the occurrence of a fault in any component of the converter, and popular fault-tolerant approaches in literature are depicted in Fig. 2 [16], [20], [22], and some of their examples are briefly discussed in Table 1. Traditionally, redundancy-based fault tolerance has proven to be the most widely adopted approach. It involves the replication of vulnerable components of the power converter, which remain in standby mode during normal operation of the converter and only operate when a faulty component is detected and isolated [23], [24], [25]. Redundancy based fault tolerance, despite its ease of incorporation, suffers from low component utilisation of the power converter, and no reduction in the electrical and thermal stresses faced by various critical components of the power converter due to the inactivity of the redundant components in normal operation of the converter. A more recent fault tolerance approach is topology morphing. This approach involves online reconfiguration of the power converter from one topology to another upon fault detection, which either isolates the faulty component or utilises it as a short circuit path and ensures that power transfer is uninterrupted [19]. Despite its rising popularity, topology morphing based approaches suffer from their own set of disadvantages, such as inability to provide fault tolerant operation to all critical devices in the power converter, and its reliance on complex control techniques to ensure uninterrupted post-fault operation. The fault tolerance solution proposed in this paper draws upon the concept of active redundancy, where vulnerable components of the power converter are replicated just as in a redundancy-based approach, but they contribute to the normal operation of the power converter as well as in post-fault operation to ensure uninterrupted transfer of power. In previous literature, active redundancy in power converters has been proposed at the converter level and submodule level in multilevel inverters, as well as in interleaved inverters [20], [21], [26], but not at the individual switch level. This opens up the possibility to propose an active redundancy based fault tolerant solution at the individual MOSFET level, making it a highly modular solution for convenient incorporation of fault tolerance in any power converter. Thus, the proposed ARM-based approach solves these issues by:

- Ensuring that the additional MOSFETs also contribute during normal operation of the power converter, thus reducing current and thermal stress on individual devices.
- Ensuring high component utilisation factor by involving all additional MOSFETs in normal operation of the converter.
- Providing fault tolerance to every MOSFET in the power converter as it is implemented at the switch-level.
- Providing a highly modular fault tolerance solution which can be incorporated into any power converter topology.

While MOSFETs operating in parallel is a well established practice in industry, its incorporation as a modular fault tolerant approach along with the proposed fault detection logic and implementation contributes to the novelty of the paper [27], [28], [29]. The contributions of this paper may be summarised as:

- Proposal and hardware implementation of an Active Redundancy Module (ARM) and Synchronous Switching scheme as a highly modular fault-tolerant solution.
- Proposal and hardware implementation of a fault detection algorithm and its implementation for the ARM.
- Power loss analysis of fault-tolerant full-bridge forward converter with detailed steps, providing a systematic procedure for loss calculations.
- Reliability analysis of fault-tolerant full-bridge forward converter with detailed steps, providing a systematic procedure for reliability calculations.

The paper is organised as follows: Section II discusses the proposed ARM and Synchronous Switching scheme in detail, and explains its working through incorporation in a full-bridge forward converter. Section III shows the simulated results for this converter, while Section IV discusses the hardware

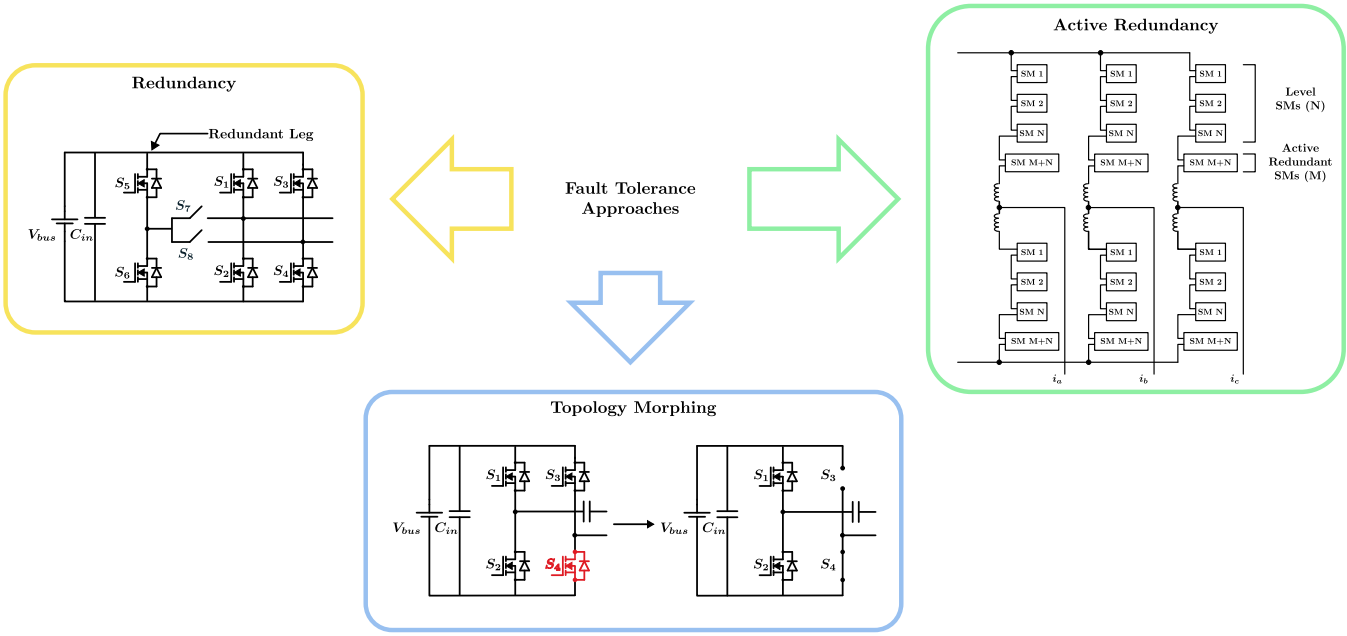


FIGURE 2. Popular fault tolerance approaches.

TABLE 1. Existing Fault Tolerance Approaches Applied in Literature

Source	Topology	Approach	Remarks
[16]	Fault Tolerant Series Resonant Converter with a redundant active leg	Redundancy	• Active leg non-operational during normal operation of the power converter. • Power converter has component utilisation. • Post-fault power delivery capability is unchanged.
[17]	Bidirectional fault-tolerant Series Resonant Converter	Redundancy	• Active leg non-operational during normal operation of the power converter. • Power converter has component utilisation. • Reduced post-fault power delivery capability.
[18]	Fault Tolerant Series Resonant Converter	Topology Morphing	• Functional only if S4 experiences short circuit fault. • Short circuited MOSFET is not a reliable conduction path, as $R_{DS(on)}$ of the faulty MOSFET cannot be accurately predicted. • Does not provide fault tolerance to all MOSFETs in the power converter. • Reduced post-fault power delivery capability.
[19]	Fault Tolerant Dual Active Bridge (DAB)	Topology Morphing	• Upon short circuit fault occurrence in S4, the DAB morphs into a half bridge on primary side and voltage doubler on secondary side. • Does not provide fault tolerance to remaining switches in the converter. • Post-fault power derating may be necessary to reduce stresses on healthy switching devices.
[20]	Three phase modular multilevel converter (MMC)	Active Redundancy	• Active redundant Sub-Modules (SM) in MMC. • Faulty SMs are bypassed and converter operation is unaffected. • Dynamic performance of MMC is unchanged.
[21]	Modular multilevel converter (MMC)	Active Redundancy	• Active redundant Sub-Modules (SM) in MMC. • Introduction of a participation factor k. • Number of active redundant submodules participating in operation of MMC is flexible. • Redundant SMs can either engage in fault tolerance or meeting the P-Q requirements of the MMC.

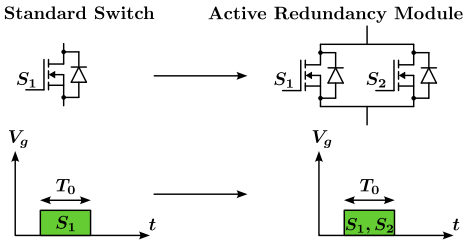


FIGURE 3. Proposed ARM with synchronous switching scheme.

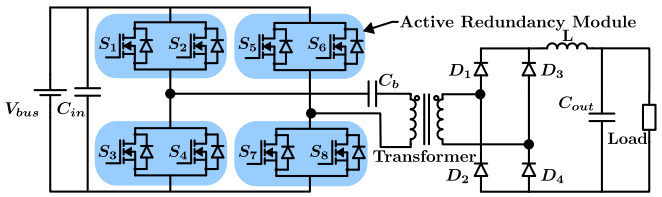


FIGURE 4. ARM incorporated full-bridge forward converter.

implementation of the fault detection algorithm as well as ARM. Section V elaborates in detail on the loss and reliability analysis of the proposed fault tolerance solution. Section VI discusses the various advantages as well as disadvantages of the proposed fault tolerance solution, and compares its effectiveness with existing fault tolerance approaches as well. Finally, Section VII concludes the paper.

II. PROPOSED FAULT-TOLERANT APPROACH

The proposed fault-tolerant solution may be described as an ARM, consisting of two identical MOSFETs connected in parallel. These MOSFETs switch synchronously; thus, the switching scheme is referred to as synchronous switching scheme. Each MOSFET in an ARM is rated to carry the full current conducted by the ARM. The proposal is visually summarised in Fig. 3. As fault tolerance is being implemented at the switch level, this makes the ARM highly modular and may be incorporated in any power converter topology with minimal modifications. To demonstrate its operation, the ARM is implemented in a full-bridge forward converter, as is shown in Fig. 4.

As the proposed ARM is implemented at the switch level, it can be incorporated in complex topologies such as resonant converters as well. The various switching pulses for an ARM-based full-bridge forward converter with synchronous switching scheme are shown in Fig. 5, along with relevant switch currents and full-bridge front-end output voltage. One may notice that in the event of fault occurrence, the complete load current flows through the healthy MOSFET in the affected ARM. Thus, the overall operation of the power converter remains unaffected in the pre- to post-fault transition. Each stage of operation in Fig. 5 has been depicted individually in Fig. 6. Fig. 6(a) and 6(b) show the normal operation of the ARM-based full-bridge forward converter. The shared current between two healthy MOSFETs of an ARM results in decreased conduction losses and improved

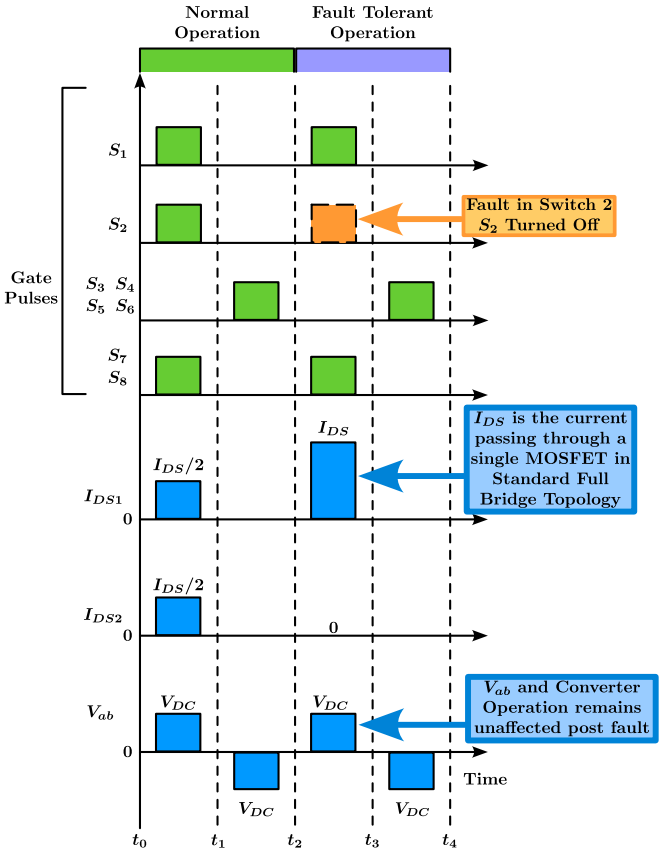


FIGURE 5. Full-bridge forward converter with active redundancy module implementation and synchronous switching scheme.

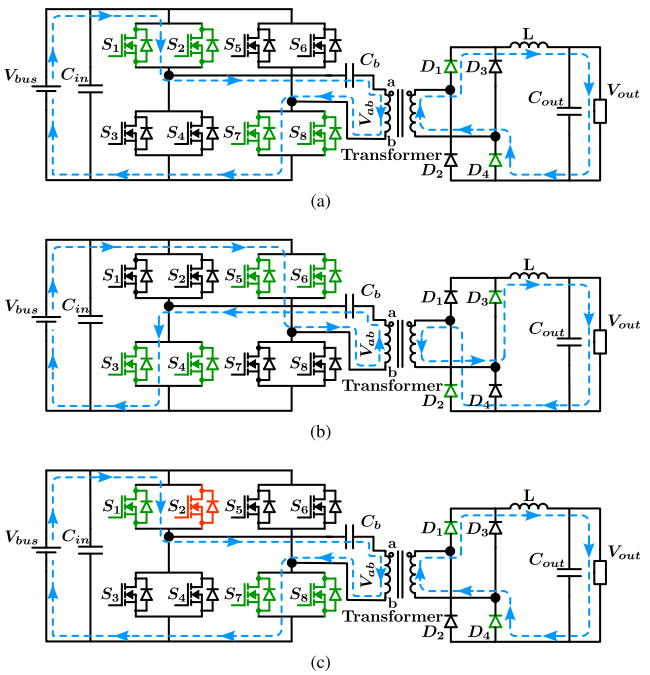


FIGURE 6. Operation of ARM-based full-bridge forward converter with synchronous switching scheme. Green indicates healthy MOSFETs, red indicates faulty and inactive MOSFETs, and blue paths indicate current flow paths.

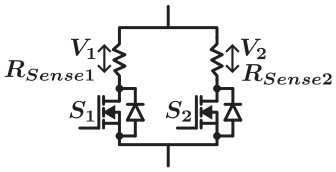


FIGURE 7. MOSFET current sensing in ARM.

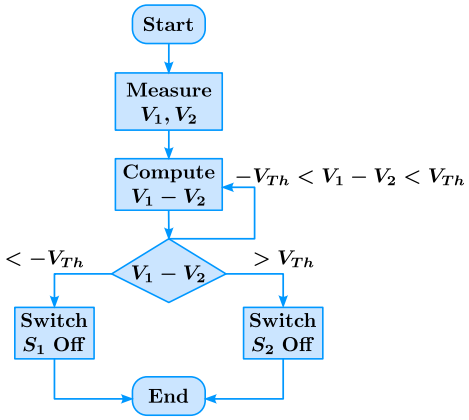


FIGURE 8. Algorithm for MOSFET deterioration detection in an ARM.

reliability, though at the cost of increased switching losses. Fig. 6(c) shows MOSFET S_2 being detected to undergo failure and subsequently switched off. Here, the entire current in the ARM flows through healthy MOSFET S_1. This brings the losses of the ARM to levels similar to a standard MOSFET. The overall reliability of the ARM, and of the entire power converter, is discussed in the following.

Failure detection in MOSFETs of an ARM is done through R_{sense} resistors connected in series with each switch, as shown in Fig. 7. During normal operation, each MOSFET carries the same amount of current, and the difference in voltages across each R_{sense} is ideally zero. If a MOSFET starts failing, its $R_{DS(on)}$ increases, reducing the current passing through it. This causes an increase in the magnitude of the voltage difference between the shunt resistors. If the voltage difference crosses a pre-defined threshold, either positive or negative, then based on the sign of the voltage difference, the faulty MOSFET is identified, and its gate pulses are disabled. This fault detection method is devised into an algorithm, and is shown in Fig. 8. Here, voltages V_1 and V_2 are the voltages across each R_{sense} in an ARM. V_{Th} is the magnitude of the threshold value set for the magnitude of $V_1 - V_2$, and accounts for minor differences in voltage across R_{sense} resistors due to non-idealities in the MOSFETs and sense resistors.

III. SIMULATION

The proposed fault-tolerant approach based on the ARM and synchronous switching scheme is simulated through a full-bridge forward converter as shown in Fig. 4 using PLECS. The power converter is simulated at 5 kW, with an input of 600 V and an output of 400 V, and operates at a switching frequency of 100 kHz. MOSFET S_2 undergoes deterioration

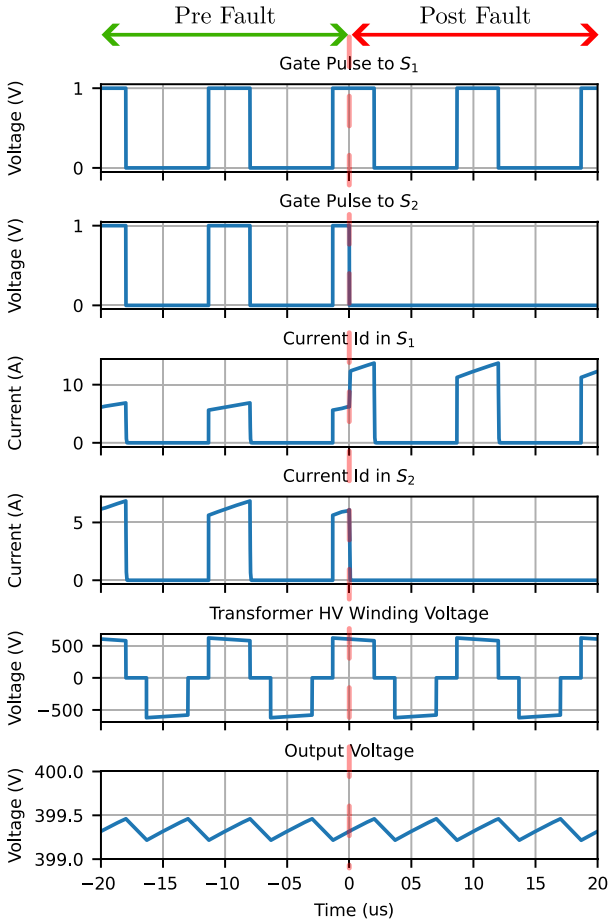


FIGURE 9. Simulation of an ARM-based full-bridge forward converter with synchronous switching scheme.

due to wearout and experiences an increase in $R_{DS(on)}$. This leads to a decrease in the current passing through S_2, and, subsequently, an increase in current through S_1. When the current difference between S_1 and S_2 exceeds a defined threshold with the appropriate sign, S_2 is turned off. S_1 then carries double the amount of current from its pre-fault operation, thus transitioning to the post-fault operation of the power converter. The pre-fault and post-fault operation of the power converter is captured by Fig. 9. One can observe that the transition from pre-fault to post-fault operation is nearly seamless, and the output voltage and power delivered by the converter remain the same in post-fault operation of the converter.

IV. HARDWARE VALIDATION

A. FAULT DETECTION

A fully analog circuit is designed to implement the algorithm shown in Fig. 8 using op-amps, to ensure fast operation and minimal resource consumption for the microcontroller being used. The circuit diagram of the fault detection circuit for two MOSFETs in an ARM, arranged as shown in Fig. 7, is depicted in Fig. 10. The proposed fault detection method

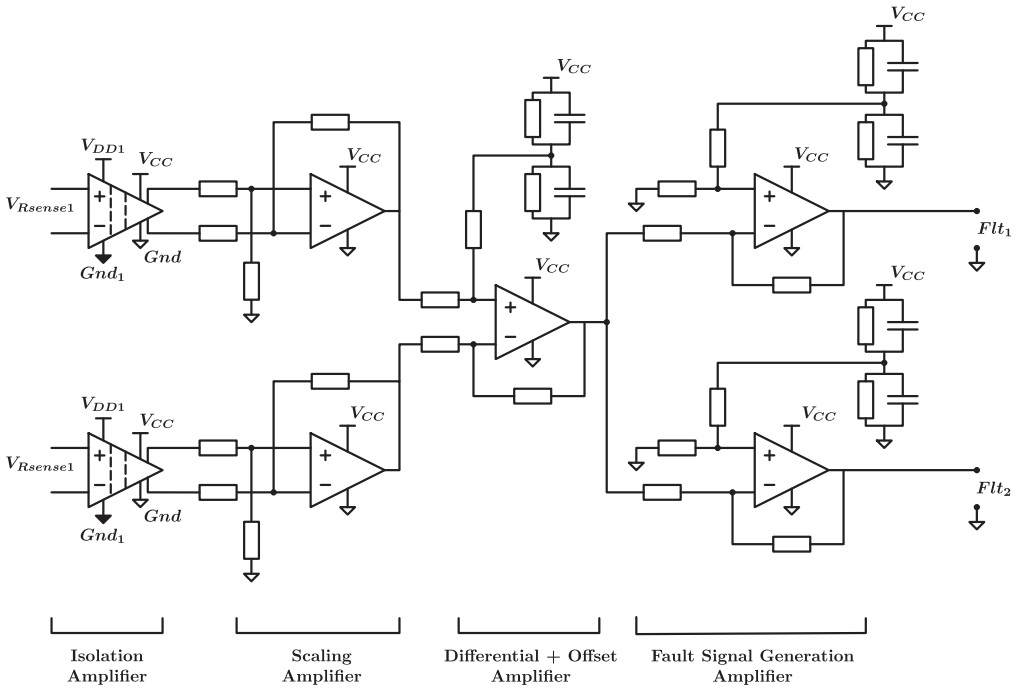


FIGURE 10. Block circuit schematic of the fault detection circuit.

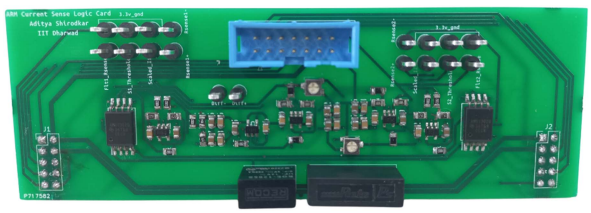
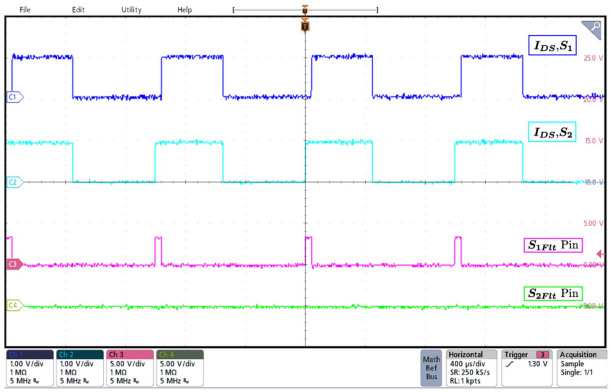


FIGURE 11. Hardware implementation of the fault detection circuit.

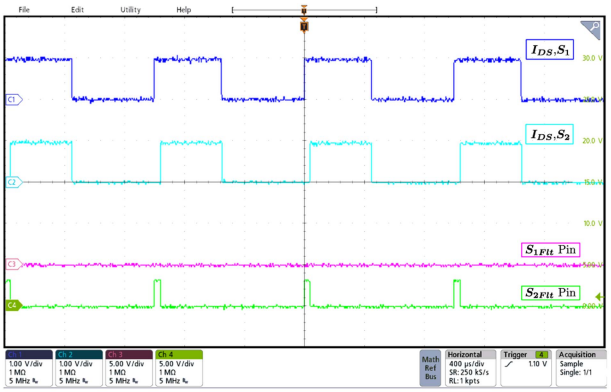
attempts to monitor MOSFET degradation at each switching, and identify and switch off degrading MOSFETs before they get fully damaged and become uncontrolled. Thus, the MOSFET undergoing degradation is taken out of operation before it enters open-circuit or short-circuit failure. The R_{sense} resistor value, gains of Op-Amps as well as the failure detection threshold values are chosen to be able to detect current differences which occur in parallel MOSFETs due to degradation of any of the MOSFET in the ARM module. The fully implemented fault detection circuit is shown in Fig. 11. To observe its behaviour, the fault detection circuit is connected to a signal generator with two independently controllable channels, to emulate the signals generated across the R_{sense} of each MOSFET present in the ARM.

The various scenarios tested are shown in Fig. 12. When switching two parallel MOSFETs synchronously, a common problem that may occur is the delay in the turn-on of one device with respect to another. This can cause the entire current of the ARM to flow through a single MOSFET momentarily, thus increasing its losses and reducing ARM reliability. The proposed fault detection circuit is able to spot such anomalies and trigger a fault signal for the relevant MOSFET based on the algorithm in Fig. 8, and this operation is shown in Fig. 12(a) and 12(b) for the turn-on delay in either MOSFET of an ARM. MOSFET degradation over time also proves to be yet another scenario of failure in an ARM. In such cases, the $R_{DS(on)}$ of the affected MOSFET rises, leading to a reduction in current flowing through it and an increase in the current flowing through the healthy MOSFET of the ARM. This difference in currents leads to a difference in voltages across sense resistors connected in series with each MOSFET. The fault detection circuit then acts in accordance with the algorithm in Fig. 8 to identify the faulty MOSFET. This is seen in action in Fig. 12(c) and 12(d). Finally, to gain insight into the algorithm's working, a synchronisation mismatch is introduced between the emulated voltages across the sense resistors of each MOSFET, and the voltage difference $V_1 - V_2$ is shown in Fig. 12(e). Here, $V_1 - V_2$ by 1.65 V to confine the difference between 0 V and 3.3 V, so that it can directly be read by the microcontroller if necessary. When this threshold crosses over a set threshold V_{Th} in either direction, the fault pin corresponding to the MOSFET undergoing degradation generates a fault signal, which is then detected by the microcontroller. The microcontroller proceeds to cut off gate pulses to the affected MOSFET and the power converter transitions to post-fault operation.

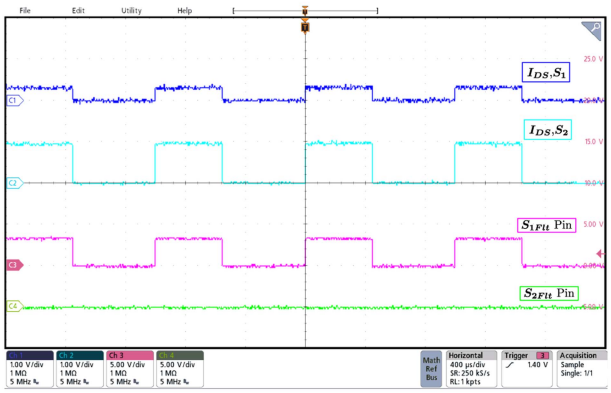
Further, the fault detection circuit is then tested with a more realistic scenario to analyse its behaviour. An ARM-based full-bridge forward converter operating at 5 kW and $V_{DC} = 400\,V$, with 12.5 A current flowing through each ARM module is considered. MOSFET S2 in the ARM is considered to be undergoing degradation, and it sees a 10% rise in its



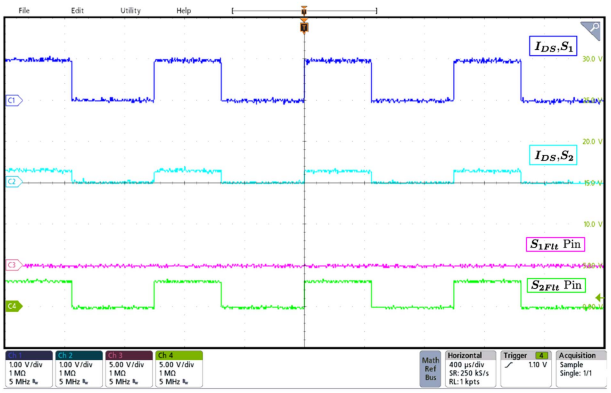
(a) Delayed turn-on of MOSFET S_1.



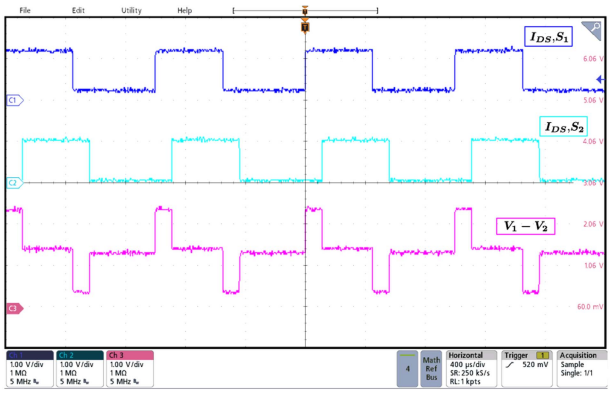
(b) Delayed turn-on of MOSFET S_2.



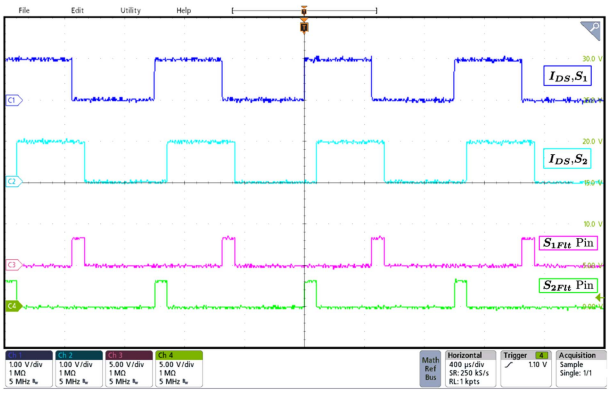
(c) Deterioration of MOSFET S_1 leading to reduced current.



(d) Deterioration of MOSFET S_2 leading to reduced current.



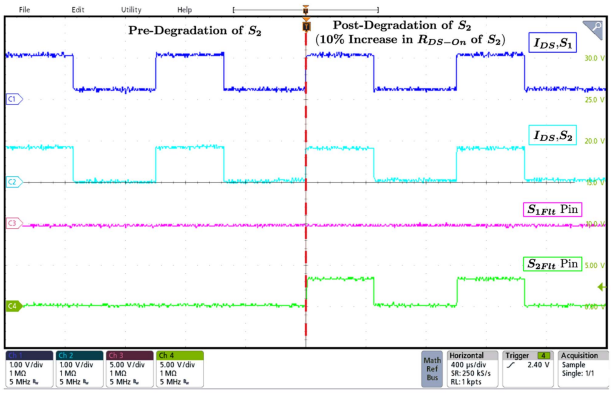
(e) Output of differential amplifier shown by mismatching synchronisation in S_1 and S_2



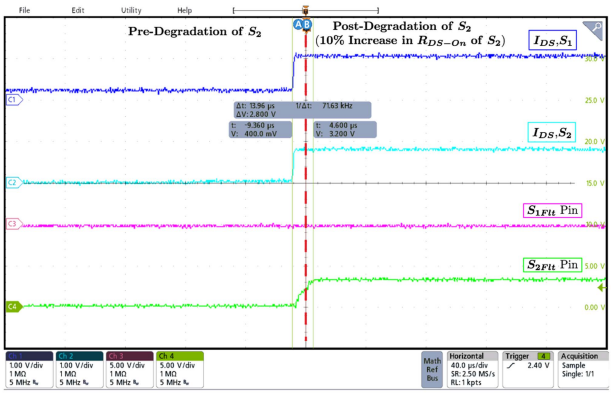
(f) Output of fault pins shown by mismatching synchronisation in S_1 and S_2

FIGURE 12. Operation of ARM fault detection circuit in various scenarios. (a) Delayed turn-on of MOSFET S_1. (b) Delayed turn-on of MOSFET S_2. (c) Deterioration of MOSFET S_1 leading to reduced current. (d) Deterioration of MOSFET S_2 leading to reduced current. (e) Output of differential amplifier shown by mismatching synchronisation in S_1 and S_2 (f) Output of fault pins shown by mismatching synchronisation in S_1 and S_2

$R_{DS(on)}$. To emulate this accurately, a 2-channel signal generator is used to emulate the voltages at each current-sense resistors, and appropriate signals are given to the isolated op-amps which measure the difference across each current-sense resistor. The imbalance in the currents flowing through both parallel MOSFETs is detected by the current sensing based fault detection circuit, and the appropriate MOSFET fault indication is signalled, as is depicted in Fig. 13(a). The captured waveforms are used to understand the delay between occurrence of current imbalance and generation of reliable fault signal. This delay, through experimental testing, is found to be 13.96 μS, shown in Fig. 13(b). Therefore, the proposed fault detection circuit is found to reliably detect MOSFET degradation, and generate fault signals with minimal delay due to its composition of purely analog op-amp based circuits. As seen from Fig. 10 depicting the fault detection logic, the current sensing signals pass through multiple op-amps with limited gain-bandwidth products, leading to propagation



(a) Detection of degradation of a MOSFET in an ARM.



(b) Delay between degradation occurrence and detection.

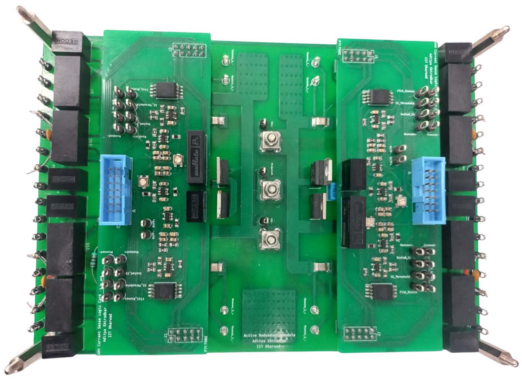
FIGURE 13. Fault detection speed of Current-sensing based fault detection circuit. (a) Detection of degradation of a MOSFET in an ARM. (b) Delay between degradation occurrence and detection.

delay. This in turn results in a delay between fault occurrence and fault detection, thus limiting the operating frequency of the power converter. This is one of the limitations of the currently proposed method. Hence, it is necessary to explore other fault detection methods which are not dependent on op-amps to decrease this delay in fault detection.

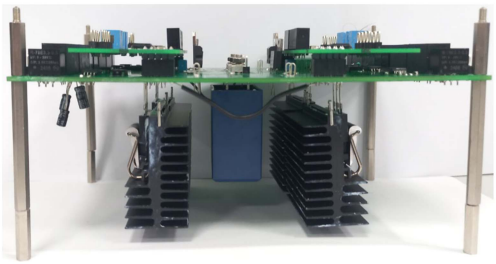
B. ACTIVE REDUNDANCY MODULE

For experimental validation, ARM-based half-bridge modules are designed and developed as shown in Fig. 14, and then are connected in a full-bridge front-end configuration. For reliable creation of a fault condition, an additional fault-creation circuit is added to the gate of each power MOSFET, as is shown in Fig. 15. The resistor, R_{flt}, is selected such that when S_{flt} is turned on, the effective gate voltage available (at S_1) is forced to a lower voltage value, thus forcing the MOSFET (S_1) to operate in its linear zone instead of saturation zone. This increases the $R_{DS(on)}$ of the MOSFET, emulating its behaviour when undergoing deterioration.

As the ARM is incorporated at the switch level, developing an ARM and synchronous switching scheme based full-bridge front-end and demonstrating its operation proves to be sufficient to experimentally validate the proposed fault-tolerant approach.



(a) Top View



(b) Side View

FIGURE 14. Hardware prototype of proposed ARM in Half Bridge configuration. (a) Top View (b) Side View

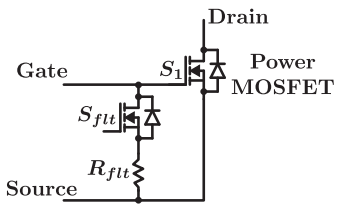


FIGURE 15. Circuit for the artificial fault creation (forcing the S_1 in linear operation).

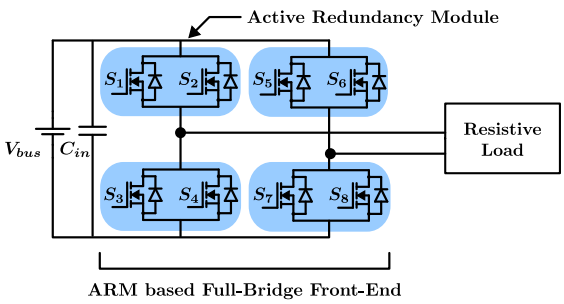


FIGURE 16. Experimental setup schematic for the ARM-based full-bridge front-end.

This is because the output of the ARM incorporated full-bridge front-end is exactly the same as a standard full-bridge front-end, and there are no modifications necessary to the rectifier side of the converter. Hence, the hardware setup is developed in accordance with Fig. 16.

A hardware setup is designed to test and validate the ARM-based full-bridge front-end, as shown in Fig. 17. Hardware testing is done in two phases. First, to validate the operation

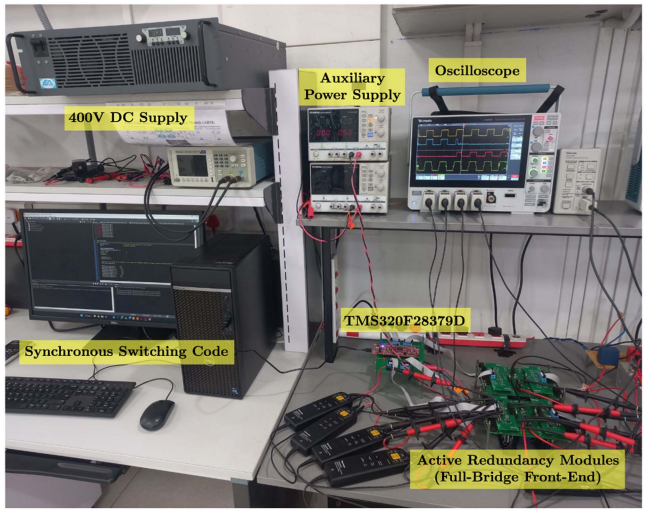


FIGURE 17. Experimental setup of the ARM-based full-bridge front-end.

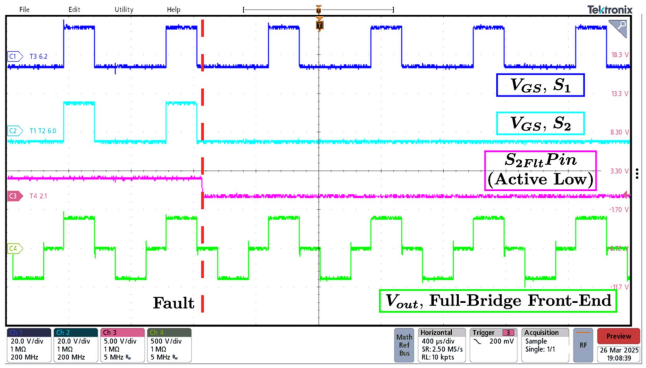


FIGURE 18. Waveforms captured for the ARM-based full-bridge front-end experimental setup at $V_{DC} = 400\,V$ with software-triggered fault [29].

of the ARM-based full-bridge front-end, it is operated at a DC voltage of 400 V and 1 kHz. Fault is then induced through software at the microcontroller itself, and the output of the full-bridge front-end is observed. It is seen that in pre-fault as well as post-fault operation, the ARM-based full-bridge front-end provides an output similar to the standard full-bridge, as is shown in Fig. 18 [29]. Further, to validate the operation of the entire fault-tolerant solution, the fault creation as well as the fault detection circuit is also incorporated into the hardware testing setup. A fault is then induced in MOSFET S_2 through the fault-creation circuit. To understand the behaviour of an individual ARM, the gate pulses given to MOSFETs S_1 and S_2, the fault pin of S_2 in the fault detection circuit, and the output of the full-bridge front-end are observed through an oscilloscope. As the voltage produced across sense resistors is in the order of millivolts, reading these voltages by the differential amplifiers of the fault detection circuit while maintaining signal integrity proved to be highly challenging due to electromagnetic interference. Further, the AMC1302QDWVRQ1 isolation op-amps used in the fault detection circuit are limited by a bandwidth of $280kHz$. The test setup is operated at 150 V,

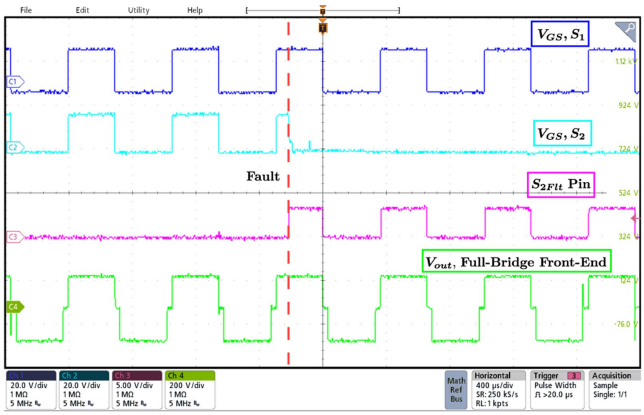


FIGURE 19. Waveforms captured for the ARM-based full-bridge front-end experimental setup at $V_{DC} = 150\,V$ with fault detection circuit.

TABLE 2. Full-Bridge Forward Converter Analysis Specifications

Sr. No.	Parameter	Value	Unit
1	Power Rating	5	kW
2	Switching Frequency	50	kHz
3	Duty Ratio	0.45	-
3	Input DC Voltage	400	V
4	Input DC Current	12.5	A
5	Transformer Turns Ratio	1:1	-

2.5 A, and 1 kHz, taking into consideration the EMI issues and low bandwidth of the isolation op-amps. Regardless of this limitation, the operation of the ARM, the fault detection circuit, and the full-bridge front end, and their behaviour are captured on the oscilloscope as shown in Fig. 19, and validate its operation sufficiently well.

As can be observed from the oscilloscope waveforms, the transition from pre-fault to post-fault conditions is nearly seamless, and the output of the ARM-based full-bridge front-end is unchanged in post-fault operating conditions. Further, as each MOSFET is rated to carry the entire current of the ARM, there is no reduction in power delivered in post-fault operation of the converter.

V. ANALYSIS

The contribution of this section is to provide simple guidelines to readers for calculating losses, efficiency, and reliability of the case-study power. Specifically, a full-bridge forward converter incorporating an ARM and synchronous switching scheme, operating with specifications shown in Table 2, is analysed by considering the components listed in Table 3.

A. LOSS ANALYSIS

This section aims to provide readers with a simple and streamlined approach for analytically calculating losses incurred by each component of the full bridge forward converter. The various steps for calculating losses of each component are explained thoroughly in a step-by-step manner.

TABLE 3. Full-Bridge Forward Converter Component Specifications

Sr. No.	Component	Specification
1	MOSFETs	IMW120R060M1H
2	Diodes	MSC015SDA120B
3	Output Capacitor	KPP-UPS-6 $1\mu F/1000V_{dc}$
4	Magnetics Cores	EE 80/38/20
5	Magnetic Core Material	N-97 Ferrite
6	Conductor for Magnetics	Copper Litz wire, $4mm^2$
7	Heatsinks	Ohmite CR101-50AE

TABLE 4. Analytically Calculated and Simulated Device Losses

Device	Calculated Loss	Simulated Loss	Unit
MOSFET	9.65	9.34	W
Diode	8.76	7.61	W

1) MOSFETs

$$\begin{aligned} P_{Loss} &= P_{Switching} + P_{Conduction} \\ &= \frac{E_{Turn-On} + E_{Turn-Off} + E_{Conduction}}{T_{period}} \\ &= \frac{E_{OSS} + E_{OSS} + I_{DS}^2 R_{DS(on)} T_{on}}{T_{period}} \\ &= \frac{2E_{OSS}}{T_{period}} + I_{DS}^2 R_{DS(on)} D \end{aligned} \tag{1}$$

where E_{OSS} is the energy stored by the output capacitance C_{OSS}, T_{period} is the time period for a switch, switching at a frequency f_{sw}, and D is the duty cycle, given by

$$D = \frac{T_{on}}{T_{period}}, \qquad T_{period} = \frac{1}{f_{sw}} \tag{2}$$

2) DIODES

$$\begin{aligned} P_{Loss} &= P_{Switching} + P_{Conduction} \\ &= \frac{E_{Switching} + E_{Conduction}}{T_{period}} \\ &= \frac{\frac{1}{2} C_J V_{DC}^2 + V_F I_F T_{on}}{T_{period}} \\ &= \frac{1}{2} C_J V_{DC}^2 f_{sw} + V_F I_F D \end{aligned} \tag{3}$$

To ensure that the analytically calculated losses are accurate, a double pulse test is simulated using the SPICE models of the MOSFET and diode in question at 400 V, 12.5 A, 0.45 duty cycle, and 50 kHz. The calculated losses were found to satisfactorily match the simulation results, as shown in Table 4. It is to be noted that the SPICE model of the diode showed a forward voltage of $V_F = 1.35$ V, which is below the value of 1.5 V mentioned in the datasheet. Using $V_F = 1.35$ V in (3), the diode losses become 7.9 W, which is closer to the simulated results.

3) OUTPUT CAPACITOR

$$P_{Loss} = I_{ripple}^2 ESR \tag{4}$$

where ESR is the effective series resistance of the capacitor.

4) TRANSFORMER

The transformer is designed such that the number of turns on the primary as well as secondary winding is 58, and the overall length of wire used in each winding is 5.2 m.

Transformer losses are calculated as:

$$P_{Loss} = P_{CopperLoss} + P_{CoreLoss} \tag{5}$$

Considering overall 4 mm^2 thickness litz wire, the DC resistance of transformer windings can be calculated using (6).

$$R_{DCwinding} = \frac{\rho l}{A} \tag{6}$$

Here, ρ is the resistivity of copper, l is the length of winding and A is the area of cross section of the conductor. AC resistance of the litz wire used can be calculated using the formula and Table 1 from [30].

$$F_R = \frac{R_{AC}}{R_{DC}} \tag{7}$$

Finally, the copper losses for each winding of the transformer can be calculated using (8).

$$P_{CopperLoss} = I_{RMS}^2 R_{ACwinding} \tag{8}$$

Here I_{RMS} is the RMS current flowing through the transformer winding. The calculated copper losses are 7.221 W.

The datasheet of the ferrite material used for the magnetic core describes a "Relative core losses versus frequency" graph, which can be used to calculate core losses as:

$$P_{CoreLoss} = P_{CoreLoss}(kW/m^3) \times Volume_{core} \tag{9}$$

Assuming a magnetic flux density of 300 mT, the core losses become 86.16 W at 25 °C for a ferrite core with specifications described in Table 3. Using these values of copper and core losses in (5), the total power losses in the transformer are calculated to be 93.381 W.

5) INDUCTOR

Inductor losses, just like the transformer, consist of copper and core losses. Core losses of an inductor cannot be calculated analytically using only datasheet values. This is because the DC bias is applied, and the unique operating conditions of inductors differ with their application, making it mandatory to experimentally determine the core losses. Therefore, for our analytical calculations, the core losses are neglected, and only the copper losses are considered. As these core losses are neglected in calculating the losses for all fault-tolerant approaches, their comparative analysis cancels out the effect

TABLE 5. Losses Due to Various Components of the Proposed Fault-Tolerant Full-Bridge Forward Converter

Component	Calculated Losses (W)	
	Pre-Fault	Post-Fault
MOSFETs	32.504	37.271
Diodes	35.028	35.028
Transformer	93.381	93.381
Inductor	2.937	2.937
Output Capacitor	4.687×10^{-3}	4.687×10^{-3}
Sense Resistors	281.25×10^{-3}	351.56×10^{-3}
Total Losses	164.17	169.01

of inductor core losses. The inductor was calculated to have 50 turns, with an overall conductor length of 4.5 m. Therefore, its copper losses can be calculated using (6).

6) SENSE RESISTORS

$$P_{Loss} = I_{DS}^2 R_{sense} \tag{10}$$

where R_{sense} is the resistance value of sense resistors used for fault detection. The losses incurred due to sense resistors used for all MOSFETs in the power converter need to be taken into consideration.

The overall power converter efficiency is calculated as:

$$\eta = \frac{P_{in} - P_{Losses}}{P_{in}} \tag{11}$$

The losses for various components of the full-bridge forward converter incorporating ARM and synchronous switching scheme and operating under the conditions described in Table 3 can be calculated by referring to the datasheets of components specified in Table 2 and using the (1)-(9). These losses are compiled in Table 5 for pre-fault as well as post-fault conditions, and the loss distributions are visually depicted in Fig. 20. When transitioning from pre-fault to post-fault operation, the converter losses experience an increase. This is due to the increased conduction losses in the healthy MOSFET of the affected ARM in the power converter, as this MOSFET now has to carry the entirety of the current flowing through the ARM. Thus, using the data in Table 5 and (11), the pre-fault efficiency of the full-bridge forward converter incorporating ARM and synchronous switching scheme is calculated to be 96.716%, and the post-fault efficiency is 96.619%. One can observe that the overall efficiency of the power converter remains majorly unchanged.

This analysis is also carried out for a standard full-bridge forward converter, fault tolerance implemented through topology morphing [22], as well as fault tolerance through redundancy [16], and the results are shown in Table 6. The proposed fault tolerance approach provides marginally better efficiency in comparison with existing solutions, while also allowing for high component utilisation, no reduction in power transfer capabilities in post-fault operation, high modularity as well as low complexities.

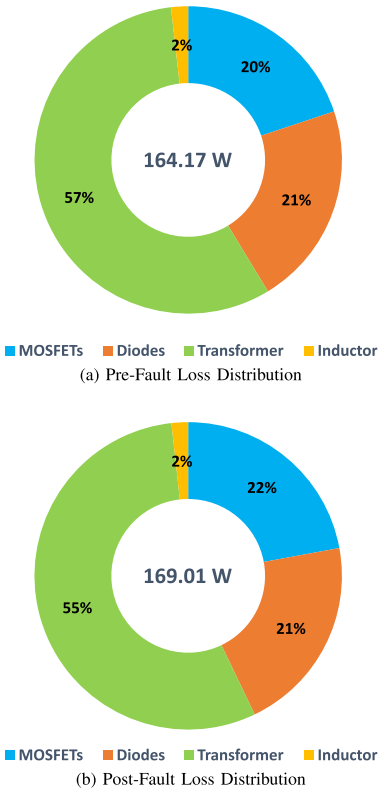


FIGURE 20. Loss distribution across various components of the proposed fault-tolerant full-bridge forward converter. (a) Pre-Fault Loss Distribution (b) Post-Fault Loss Distribution

TABLE 6. Efficiencies of Various Fault Tolerance Approaches When Implemented on a Full-Bridge Forward Converter

Fault Tolerance Approach	Efficiency (%)	
	Pre-Fault	Post Fault
Standard Full-Bridge	96.600	0
Topology Morphing	96.600	96.390
Redundancy	96.600	96.004
ARM + Synchronous Switching	96.716	96.619

B. RELIABILITY ANALYSIS

This section provides insight into how the reliability of various fault tolerance approaches, when applied to a power converter, may deteriorate over time. Reliability analysis involves calculating the failure rate (λ) for various components of the power converter topology and developing an expression for the overall reliability of the power converter as a function of time. For the convenience in understanding by the readers, the various steps taken for reliability calculations are presented and thoroughly elaborated. It is to be noted that only the data available in device datasheets is used in this section as well, to allow for accessible calculation of reliability by readers for their own applications. Thus, the contribution of this section is to provide convenient guidelines for readers to perform reliability analysis and calculate the mean time to failure of power converters.

To begin, each component of the power converter has its own failure rate, which depends on the stresses it experiences, its operating temperature, the quality of the material used in manufacturing, and other factors. The guidelines for failure rate calculations are outlined in MIL-HDBK-217 [31]. The reliability expression for a full-bridge forward converter incorporating ARM and synchronous switching scheme is elaborated upon in this section, for the benefit of readers looking to understand reliability and how to apply it for their applications. The various factors that affect the failure rate (λ) of power electronic devices are described as follows:

$$\begin{aligned}\lambda_b &= \text{Base Failure Rate}\\ \pi_T &= \text{Temperature Factor}\\ \pi_Q &= \text{Quality Factor}\\ \pi_S &= \text{Electrical Stress Factor}\\ \pi_E &= \text{Environment Factor}\\ \pi_A &= \text{Application Factor}\\ \pi_C &= \text{Contact Construction Factor}\\ \pi_{CV} &= \text{Capacitance Factor}\end{aligned} \tag{12}$$

Further, the general expression for reliability $R(t)$ for any component is given by:

$$R(t) = e^{-\lambda t} \tag{13}$$

1) DIODES

The reliability of diodes is calculated as:

$$\lambda_{Diode} = \lambda_b \pi_T \pi_S \pi_C \pi_Q \pi_E \text{Failures}/10^6\text{Hours} \tag{14}$$

Calculation of π_T depends on device junction temperature according to:

$$R_{\theta CA} = \frac{T_J - T_A}{P_{loss}} + R_{\theta JC} \tag{15}$$

where

$$\begin{aligned}R_{\theta CA} &= \text{Thermal Resistance, Heatsink}\\ R_{\theta JC} &= \text{Thermal Resistance, Junction to Case}\\ P_{loss} &= \text{Device Losses}\\ T_J &= \text{Junction Temperature}\\ T_A &= \text{Ambient Temperature}\end{aligned}$$

2) MOSFET

The failure rate of MOSFETs is calculated from:

$$\lambda_{MOSFET} = \lambda_b \pi_T \pi_A \pi_Q \pi_E \text{Failures}/10^6\text{Hours} \tag{16}$$

π_T here again depends on device junction temperature, which is obtained using (15).

TABLE 7. Failure Rates of Various Components of a Full-Bridge Forward Converter Incorporating ARM and Synchronous Switching Scheme

Description	Notation	Failures/10^6 (hours)
MOSFETs operating at 12.5 A	$\lambda_{SW,12.5A}$	2.178
MOSFETs operating at 6.25 A	$\lambda_{SW,6.25A}$	1.496
Diodes	λ_{Diode}	7.29696×10^{-3}
Input Capacitor	λ_{Cin}	0.04871
Output Capacitor	λ_{Cout}	0.0322

3) CAPACITOR

For capacitors, failure rate is given by (17).

$$\lambda_{Capacitor} = \lambda_b \pi_{CV} \pi_Q \pi_E \text{Failures}/10^6\text{Hours} \tag{17}$$

4) INDUCTOR AND TRANSFORMER

Multiple studies have shown that the magnetic components show the highest reliability in a power converter, and thus, are the least likely to fail [32], [33]. Therefore, they are omitted in the reliability analysis of the converter.

When equations (14) to (17) are applied to an ARM and Synchronous Switching Scheme based Full-Bridge Forward Converter operating as described in Table 2 and consisting of components listed in Table 3, the failure rates calculated and shown in Table 7 are obtained.

Following the procedure detailed in [34], the reliability of a single ARM can be expressed as per:

$$\begin{aligned}R_{M(t)} = {} & e^{-2\lambda_{SW,6.25A}t}\\ & + \frac{2\lambda_{SW,6.25A}}{\lambda_{SW,12.5A} - 2\lambda_{SW,6.25A}}\\ & \times [e^{-2\lambda_{SW,6.25A}t} - e^{-\lambda_{SW,12.5A}t}]\end{aligned} \tag{18}$$

Therefore, the reliability of the complete ARM and Synchronous Switching Scheme-based Full-Bridge Forward Converter can be written as:

$$R_{converter} = R_{Cin} R_M^4 R_D^4 R_{Cout} \tag{19}$$

Utilising (13), (18) and Table 7 in (19), we get:

$$R_{converter} = e^{-0.109t}(3.675e^{-2.178t} - 2.675e^{-2.99t})^4 \tag{20}$$

Similar analysis is done for the standard full-bridge forward converter with no fault tolerance, topology morphing, and redundancy-based approaches, and the results are compiled in Table 8, and visually represented in Fig. 21. From Table 8, it is evident that the reliability of each fault-tolerant approach decreases exponentially with time. Compared to a standard full-bridge forward converter, topology morphing does provide marginally higher operating life, but is limited by the number of MOSFETs it covers for fault tolerance. Redundancy-based approach provides fault tolerance to all MOSFETs in the converter, but remains inactive during normal operation. Therefore, each MOSFET carries higher currents and therefore has higher losses, leading to reduced reliability. The unique nature of active redundancy, involvement

TABLE 8. Reliability Expressions of Various Fault Tolerance Approaches When Implemented in a Full-Bridge Forward Converter

Approach	Reliability Expression
Standard Topology	$e^{-8.821t}$
Topology Morphing	$e^{-8.886t} + 1.1e^{-10.866t}(e^{1.98t} - 1)$
Redundancy	$e^{-0.109t}[e^{-8.712t} + 0.814(e^{-8.712t} - e^{-19.404t})]$
ARM + Synchronous Switching	$e^{-0.109t}(3.675e^{-2.178t} - 2.675e^{-2.99t})^4$

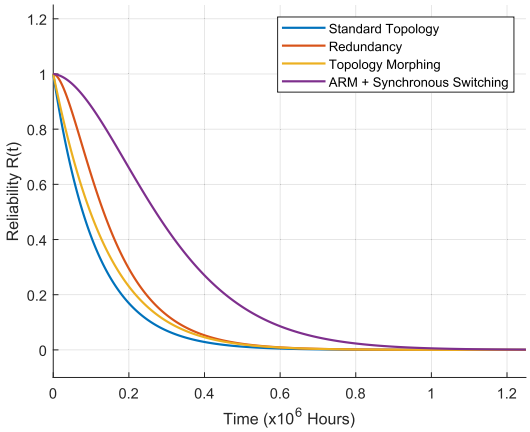


FIGURE 21. Reliability of a full-bridge forward converter for various fault-tolerant approaches over time.

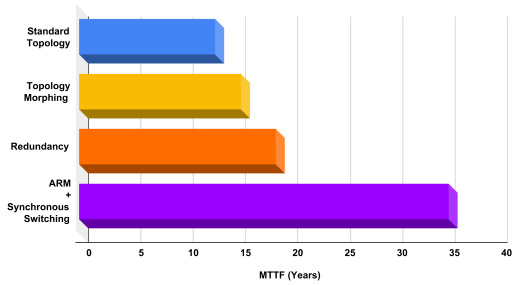


FIGURE 22. MTTF of various fault tolerance approaches when implemented on a full-bridge forward converter.

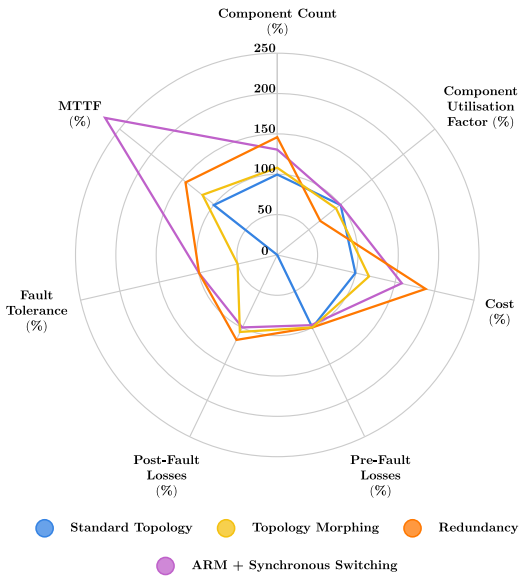


FIGURE 23. Comparison of proposed fault-tolerant solution over various approaches.

of additional components during normal operation of the converter, and the highly modular switch level implementation of the ARM and synchronous switching scheme ensure much higher reliability over existing fault tolerance approaches, as is seen in Fig. 21.

Mean Time To Failure (MTTF) is the expected time for which a system can operate before occurrence of failure. MTTF can be calculated from a system's reliability expression R(t) as shown in (21) [35].

$$MTTF = \int_{t=0}^{\infty} R(t)dtrm(\times 10^6 Hours) \qquad (21)$$

Where R(t) correspond to the reliability expressions for a full-bridge forward converter with various incorporated fault tolerance approaches as shown in Table 8. MTTF calculation for the various discussed fault tolerant approaches assumes that the full-bridge forward converter is fully operational with no degradation or defects at the start of its operating life, and that the reliability of the power converter decreases with time as dictated by Table 8.

As is shown Fig. 22, in the higher reliability of the proposed fault-tolerant approach translates to a much higher mean time to failure of the power converter, thus significantly extending the operating life of the converter compared to existing fault-tolerant approaches.

VI. DISCUSSION

From the previous sections, it is evident that the proposed fault-tolerant solution provides a multitude of benefits. The converter power delivered, as well as the efficiency, remains almost unchanged in pre-fault and post-fault operation. Further, it causes no modifications to the power converter transfer function, leading to easy implementation of closed-loop control. In comparison to existing fault-tolerant approaches, the proposed ARM and synchronous switching scheme exhibits high modularity, high component utilisation factor, higher reliability over time, and better mean time to failure as well. This makes the proposed approach highly attractive to industrial applications regardless of the converter topology employed, complex or otherwise. The only major drawback of the proposed ARM and Synchronous Switching scheme is its reliance on sense resistors. The accuracy of sense resistors, as

TABLE 9. Analysis of Full-Bridge Forward Converter Incorporating ARM and Synchronous Switching Scheme

Operation	Advantages	Disadvantages
Pre-Fault	• Minimal modifications to power converter topology • Reduced MOSFET conduction losses • Power converter transfer function is unaffected • No alterations necessary to closed loop control	• Additional MOSFETs and gate drivers required • Additional fault sensing circuit required • Additional cost • Increased switching losses • Reliance on sense resistors
Post-Fault	• No change in output voltage, current, or frequency of the full-bridge front end; therefore, magnetic elements of the converter are unaffected. • No reduction in delivered output power. • Minimal effect on the efficiency of the power converter • No modification in converter transfer function and closed loop control.	• Increased conduction losses in the healthy MOSFET of the affected ARM.

TABLE 10. Comparison With Existing Fault Tolerance Approaches

Fault-Tolerant Approach	Drawback of Existing Approach	Advantage of Active Redundancy Module
Redundancy	• Reduced component utilisation during normal operation. • Higher component count, leading to higher costs. • Lower reliability and mean time to failure. • Difficult to predict the performance of redundant components due to their dormant state in harsh operating conditions under pre-fault operation of the converter.	• Active redundancy ensures that all switches are utilised, and the distribution of power stress over both switches in a module promotes the longer lifespan of each switch. • Higher reliability and much longer mean time to failure.
Topology Morphing	• Post-fault operation may demand complicated control schemes. • This approach proves to be very converter topology specific. • The value of $R_{DS(on)}$ of short circuited MOSFET proves to be inconsistent [36]. This can prove detrimental to topology morphing solutions utilising a short-circuited MOSFET. • Topology morphing approaches may lead to reduced power delivered by the converter in post-fault conditions. • Minimal increase in reliability and mean time to failure of the power converter.	• Minimal changes to the control scheme. • High modularity allows for easy incorporation in any power converter topology. • Much higher reliability and mean time to failure of the power converter.

well as the electromagnetic interference encountered in measuring the small voltages that occur across these resistors, may reduce the accuracy of the fault detection approach. Therefore, care must be taken to ensure the integrity of signals reaching the isolation amplifiers used for current measurement. The various advantages and disadvantages of the proposed fault-tolerant solution are further discussed in Table 9, and its comparison with existing approaches has been elaborated upon in Table 10.

To understand the performance of the proposed fault-tolerant solution with respect to existing approaches at a glance, various parameters crucial for power converter performance and operation are considered. These include pre-fault and post-fault converter losses, mean time to failure, cost of development, component utilisation factor, and ability to provide fault-tolerant operation to all the MOSFETs in the converter. For uniform comparison, all values are expressed in percentages, with the standard full-bridge forward converter with no incorporated fault tolerance as the reference. The various fault-tolerant solutions are then applied to a full-bridge forward converter, and the converter performance across the decided parameters is observed. The results are shown in Fig. 23. It is to be noted that in the standard redundancy approach, the redundant leg is connected to operational legs through bidirectional switches composed of two MOSFETs each. This is done to allow for fast switching between the faulty leg and redundant leg. These additional devices and their corresponding gate drivers result in a comparatively higher component count and cost in comparison to the proposed ARM based approach. Further, both MOSFETs in an ARM are designed to carry full-load current and are equipped with heatsinks which can safely dissipate heat at full-load operation as well (Heatsink selection is done based on single switch full load operation, as it is the worst-case operating condition). The inclusion of additional MOSFETs and heatsinks leads to reduced power density, larger volume and higher cost in comparison to a standard full-bridge forward converter. Yet, these drawbacks are offset by the improved pre-fault efficiency, comparable post-fault efficiency and full-proof fault-tolerant capabilities of the ARM and synchronous switching scheme incorporated full-bridge forward converter. The proposed fault-tolerant solution requires moderate component count and cost, while providing pre-fault and post-fault operating efficiency comparable to existing approaches as is evident from the comparable converter losses, and providing fault-tolerant operating capabilities to all MOSFETs in the

power converter, a high component utilisation factor, and a high mean time to failure. All of these characteristics make the proposed ARM and synchronous switching scheme an attractive fault-tolerant solution.

VII. CONCLUSION

The paper proposes an Active Redundancy Module and Synchronous Switching Scheme as a novel and highly modular fault-tolerant approach. The proposed approach is validated through PLECS simulation of a 400 V, 5 kW full-bridge forward converter. Further, hardware prototypes of ARM incorporated half-bridge modules are developed, and their pre-fault as well as post-fault operation is demonstrated through a full-bridge front-end configuration at 400 V DC. It is observed that the proposed fault tolerance solution can switch from pre-fault to post-fault operation nearly seamlessly, from the perspective of converter operation. For fault detection, a current-sensing-based logic is proposed, implemented in hardware, and its operation in various scenarios is demonstrated as well. The paper then performs an in-depth loss, efficiency and reliability analysis for the proposed fault-tolerant solution when applied to a full-bridge forward converter. It is observed that the efficiency of the converter when incorporated with the proposed fault-tolerant approach is very similar to the standard full-bridge forward converter. Further, the reliability analysis showed that the proposed fault tolerant solution greatly increases the reliability and significantly extends the life of the power converter. The various advantages and disadvantages of the proposed solution are discussed, and it is compared with existing approaches across various key factors, proving its effectiveness as a practical and attractive approach for incorporating fault tolerance in power converters.

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