A Wideband and Low-Noise CMOS-Integrated X-Hall Current Sensor Operating in Current Mode

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***Abstract*— Power electronic circuits are moving toward higher switching frequencies, exploiting the capabilities of novel devices, so as to shrink the dimension of the passive components. This trend demands sensors able to operate at such high frequencies. This article aims to demonstrate the broadband capability of a fully integrated CMOS current sensor based on the X-Hall approach and configured in current mode, by alleviating the impact of stray capacitive loading at the probe–readout interface. Current-mode operation enables the usage of a transimpedance amplifier (TIA) as a readout circuit, offering better bandwidth, noise, and power performance than conventional instrumentation amplifiers (IAs). The system exploits a common-mode (CM) control system to operate the submodules at different supply voltages, respectively, 5 V for the X-Hall probe to achieve high sensitivity, and 1.2 V for the readout to exploit the high transition frequency of transistors with reduced oxide thickness. A chip-on-board mounting limits the parasitic inductive effects on the host printed circuit board (PCB). The developed prototype achieves a maximum acquisition bandwidth of 12 MHz. With a power consumption of 11.46 mW and a resolution of 39 mA_{rms}, it presents a sensitivity of 8% T^{-1} and achieves an FoM of 569 MHz/A^2mW, which is significantly higher than the current state-of-the-art hybrid Hall/coil solutions. The prototype is implemented in a 90-nm microelectronic process from STMicroelectronics and occupies a silicon area of 2.4 mm^2.**

***Index Terms*— Broadband sensing, current mode, current sensing, Hall sensor, self-biased transimpedance amplifier (TIA), voltage mode, X-Hall.**

I. Introduction

INNOVATIVE current-sensing solutions allowing for high signal bandwidths must be sought to respond to the demand for fast switching power electronics [1], [2]. An ideal approach would be the deployment of a noninvasive current sensor, compact in size, which fulfills the criteria of the broadband operation of power electronics, supports ac and dc sensing with galvanic isolation, and consumes low power. The Rogowski coil (RC) [3] and the current transformers (CTs) [4], [5] are competent in terms of realizable bandwidth (up to GHz) [6], but the resulting sensor is bulky, difficult to integrate, and loses the dc signal component. Differently, compactness and integrability in microelectronic substrates are achieved by Hall-effect current sensors, which offer the advantages of sensitivity to dc signals and galvanic isolation [2], [7], but can barely reach the MHz range in bandwidth [8], [9], [10] and may require additional back-end processes or exotic materials for improved performance [11], [12]. To overcome these drawbacks, the state-of-the-art broadband current sensing techniques have adopted hybrid solutions by combining RC or CT with compact Hall-effect current sensors [13], [14]. This approach is, however, challenged by nonlinearity issues mainly arising from the matching of different frequency responses. When following a hybrid approach, reduction of the nonlinear deviation is of primary concern [15], while the bandwidth requirements are usually assured by the CT or RC. Another category of highly reliable, miniature, and low-power sensors are the tunneling magnetoresistance (TMR) sensors, which demonstrate a bandwidth of 5 MHz [16] although commercial sensors such as the TLE5501 and the TMR2301 could reach a few hundreds of kHz [17], [18]. Moving apart from the hybrid solutions and focusing on the purely Hall-effect sensor, although it was mainly considered for low-frequency applications, it can become a valuable solution in broadband applications, by boosting its bandwidth limit in the MHz range [19], [20] and beyond [21].

In microelectronic implementations, a Hall probe is usually fabricated as an n-well device surrounded by a p-type layer with two sense contacts and two bias contacts placed orthogonal to each other. Due to the Hall effect, the incident magnetic field B_z, which is generated by the current to be sensed, causes a potential difference V_H to develop across the sense terminals following the static formulation:

$$V_H = S_I \cdot I_{\text{bias}} \cdot B_z \tag{1}$$

where I_{bias} is the applied bias current, and S_I is the current-related sensitivity [20]. Crescentini et al. [22] identified four bandwidth limits for purely Hall sensors as shown in Fig. 1: 1) physical limit set by the carrier relaxation time; 2) fundamental limit set by the n-well intrinsic capacitance; 3) practical limit due to the capacitive load of the analog front-end (AFE); and 4) methodological limit set by the

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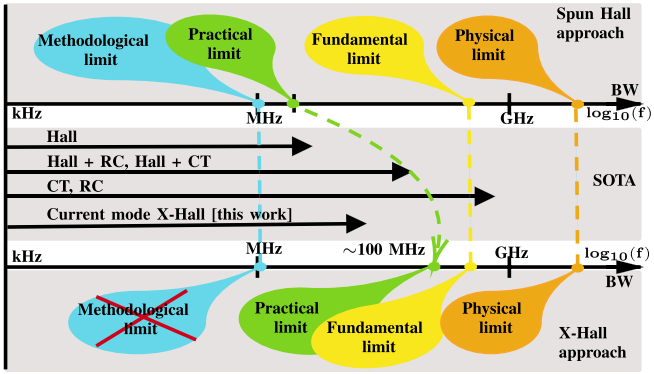

Fig. 1. Bandwidth limits enhancement provided by the X-Hall architecture compared with spun Hall sensors.

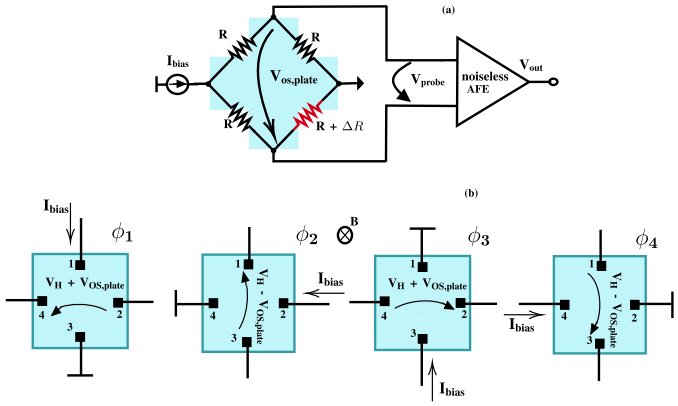

Fig. 2. (a) Wheatstone bridge model of the offset of a Hall sensor illustrating the bridge unbalance due to probe asymmetries. (b) Representation of the SCT.

read-out techniques, e.g., by the widely adopted spinning current technique (SCT) [23]. In addition, thermal noise generated by the probe and bandwidth limits of the AFE are further hindrances to the broadband exploitation of the Hall-effect current sensor.

Fig. 2(a) illustrates the general offset model of the Hall sensor, represented as a Wheatstone bridge with branch resistances of value R. Practically, the device comes with its own set of imperfections in terms of device geometry, doping concentration, and other fabrication issues, which may alter the balance of the Wheatstone bridge, resulting in an undesirable offset of tens of mV that completely dominates the detected signal, which usually is in the order of a few μV. Multiple solutions were proposed to overcome this major drawback [20], [24]. The most used offset-reduction method is the SCT [25], [see Fig. 2(b)] which uses a single Hall plate but spins the bias current around the probe and uses all the contact pairs sequentially, while sensing the Hall voltage at contacts perpendicular to the respective bias direction. The measurement is made at every $T_{\text{spin}} = 1/f_{\text{spin}}$ implying a rotation time of n-T_{spin} for an n-phase SCT. Summing all the measurements over a complete rotation leads to a reduction of the offset by almost a factor of 100 [20], [26]. Besides this, the practical implementation of this technique increases the capacitive load seen by the Hall plate, which sets a significant limit to the bandwidth. The methodological bandwidth limit was overcome by the design of the X-Hall probe [22] by providing inherent static offset reduction, hence eliminating the need for the SCT and speculating an improved practical limit of 200-MHz bandwidth achievable by the X-Hall probe itself, subject to AFE's design. This would place the X-Hall sensor on par with the state-of-the-art hybrid solutions. Practically, the X-Hall sensing system operated in voltage mode [27] achieved a 4-MHz bandwidth when implemented in the 0.16-μm technology with a differential-difference current feedback amplifier (DDCFA) as AFE. The limitations in bandwidth were mainly due to the amplifier itself and the parasitic inductive effects at package level.

Changing the configuration of the probe from traditional voltage mode to the current mode [28] opens the choice of AFE to transimpedance amplifiers (TIAs) which are proven to be much faster [29] than conventional instrumentation amplifiers (IAs) [30] and differential-difference amplifiers (DDAs) [31] used in the voltage mode. The two configurations would differ in the aspect of whether the AFE reads a Hall voltage or a Hall current, respectively. Moreover, the current mode configuration would require the AFE to have a low input impedance in contrast to that in voltage mode, making the effect of probe intrinsic output capacitance negligible, thus hastening its response.

This article presents a novel Hall-effect current sensor that extends the sensing bandwidth by a factor of roughly 10 with respect to the recent literature [14], [32] and of 3 with respect to our previous work [27]. The sensor is based on the X-Hall architecture; it overcomes the limitations in [27] by proposing to operate the X-Hall probe in current mode and by bonding the die to the test board to reduce parasitics. The current-mode readout enables the usage of a fast and low-noise TIA. A common-mode control (CMC) circuit is proposed at the probe–AFE interface to enable the coupling between the Hall probe, connected to the 5-V supply domain for better sensitivity, and the AFE, which is realized using faster low-voltage transistors. Finally, an S-shaped metal path is proposed to better focus the magnetic field generated by the current onto the X-Hall sensor, providing a better current sensitivity.

This article is organized as follows. Section II presents the main technical solutions that allow to extend the acquisition bandwidth beyond the MHz limit, while Section III describes the proposed architecture of the current sensor. Section IV presents the results of the experimental measurements on the fabricated prototypes, Section V discusses the broadband application scope of the state-of-the-art devices followed by a conclusive discussion.

II. Bandwidth Enhancement in Hall Sensors

The proposed solution widens the bandwidth of the Hall-effect current sensor by tackling the methodological and the practical bandwidth limit. The X-Hall architecture replaces the SCT with a static offset reduction technique that makes it possible to operate the Hall probe at higher frequencies, even though a higher residual offset is expected with respect to the SCT. Second, current-mode readout operation allows neglecting the capacitive load of the AFE, moving the

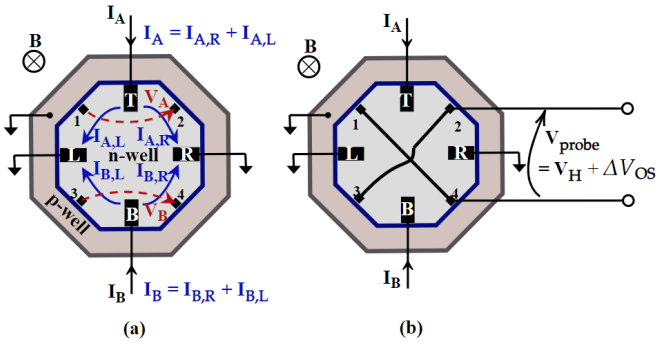

Fig. 3. X-Hall probe configured in voltage mode. (a) Distribution of bias currents. (b) X-like shorting of the four smaller contacts.

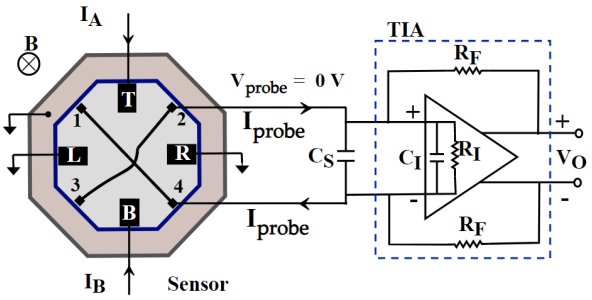

Fig. 4. X-Hall probe configured in current mode. The Hall voltage is nulled and the current out from the probe is measured using a TIA. C_S is the output capacitance of the Hall plate, and C_I is the intrinsic capacitance of the shunt-feedback TIA with feedback resistors R_F.

practical bandwidth limit closer to the fundamental limit of hundreds of MHz. Furthermore, the AFE is designed using the faster low-voltage transistors available in the versatile bipolar-CMOS-DMOS (BCD) technology, which is a microelectronic process that embeds on the same silicon structure all the above types of transistors, i.e., bipolar junction, complementary metal-oxide and double-diffused metal-oxide transistors.

A. X-Hall

The X-Hall probe was proposed initially in [22] and was described in [27]. It is an octagon-shaped n-well with four large bias contacts at the top (T), bottom (B), left (L), and right (R) and four small sense contacts (1–4), as shown in Fig. 3(a). The bias current is fed to the plate by two opposite bias contacts, while the other two are shorted to a low-impedance node, like the ground. Lightly doped n-wells with doping concentration n used for high-voltage devices in BCD technology are appropriate for the active layer of the Hall probe due to their higher mobility, thus yielding a higher sensitivity to the magnetic field.

The active n-well must be isolated from the substrate, and this is usually achieved by surrounding it with a p-well. However, the p–n junction causes nonlinearity and anisotropy problems for the sensor, as well as a parasitic capacitive effect at the probe output, due to the difference in the potentials between the active n-well and the grounded p-well [20], [28].

When configured in the voltage mode and in the presence of an external magnetic field normal to the probe surface, the current density over the entire device will no more be uniform and will concentrate on one side. This can be represented by the corresponding unbalance of bias currents on the right or left sides, $I_{A,R}$ and $I_{A,L}$ in the top half of the probe, in response to the tilting of the equipotential lines. Considering that the structure can be viewed as a composition of two Hall probes, there is a similar unbalance between $I_{B,R}$ and $I_{B,L}$, and hence, the differential Hall voltage potentials V_A and V_B, respectively, appear across the sense contacts (1, 2) and (3, 4) as depicted in Fig. 3(a)

$$\begin{aligned} V_A &= V_2 - V_1 = V_H + V_{\text{OS,plate}}^{(A)} \\ V_B &= V_4 - V_3 = -V_H + V_{\text{OS,plate}}^{(B)} \end{aligned} \tag{2}$$

where the Hall voltage, V_H, acts in opposition on V_A and V_B because the bias currents I_A and I_B flow in opposite directions

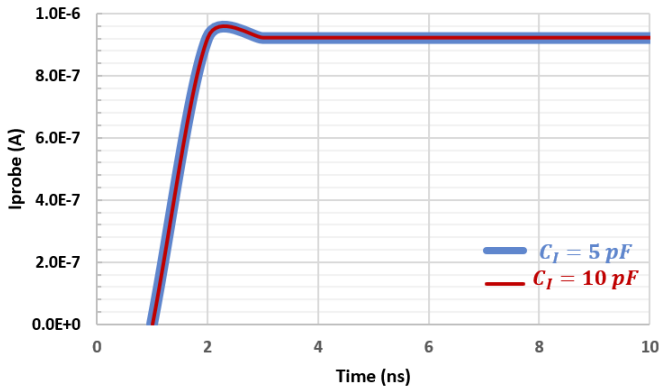

Fig. 5. Simulated time response of X-Hall probe in current mode to a magnetic field step stimulus of 50 mT at $t = 0$ s and biased at 500 μA.

within the active region and are ideally equal in magnitude. At first sight, the offset voltages associated with the Hall plate, $V_{\text{OS,plate}}^{(A)}$ and $V_{\text{OS,plate}}^{(B)}$, can be treated as fully correlated since there is a unique active region. A diagonal shorting of the sense contacts to form an "X" would now promote a new boundary condition on the charge distribution, such that $V_A = -V_B = V_{\text{probe}}$ and results in an X-Hall output voltage $V_{\text{probe}} = V_H + \Delta V_{\text{OS}}$, where ΔV_{OS} is the residual uncompensated offset originated by all those sources of local defects, such as geometrical and microelectronic imperfections [33], [34].

In conclusion, the X-Hall probe realizes a static offset reduction without requiring SCT and allows to achieve a wider bandwidth than standard spun Hall sensors. Device simulation using technology computer aided design (TCAD) has proven the potential to achieve a bandwidth greater than 200 MHz under ideal conditions. However, it must be stated that the residual offset in the X-Hall sensor is noticeably higher than that in spun Hall sensors. This tradeoff between accuracy and speed may be accepted in applications requiring the detection of very short spikes.

B. Current-Mode Readout

An alternative way to operate the Hall probe is the current mode, wherein the independent sense contacts 2 and 4 are virtually shorted through the input impedance of the TIA, which should be as low as possible to sink maximum current from the probe and force the potential difference between the contacts to be zero, as illustrated in Fig. 4; hence behaving

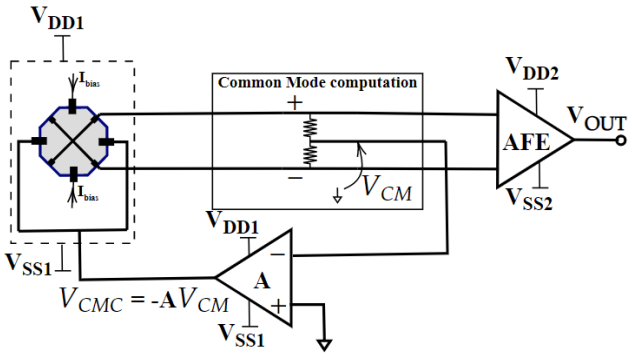

Fig. 6. Scheme of the CMC loop.

as a dual of the voltage mode. This short circuit avoids the accumulation of charges on the edges of the probe and the creation of the Hall voltage by constantly sinking/sourcing current at the sense nodes. The imbalance of the bias currents in the presence of magnetic field results in a current through the sense terminals, $I_{\text{probe}} = I_H + \Delta I_{\text{OS}}$, where I_H is the Hall current and ΔI_{OS} is the residual current offset. This modality allows to overcome the bandwidth limit set by the capacitive load of the AFE by lowering the impedance value associated with the node and the relative time constant. TCAD simulation of the probe, considering equivalent resistance of the probe $R = 3$ kΩ and $C_S = 0.7$ pF, working in the current mode interfaced with an ideal TIA model with input capacitance of 5 and 10 pF demonstrates the possibility to achieve a bandwidth greater than 200 MHz (see Fig. 5). This gives a time constant of about $\tau = 2$ ns in both the cases, highlighting the negligible impact of the self-loading capacitance of the probe in the current mode. A picture of the shunt-feedback TIA interfaced with the Hall plate is shown in Fig. 4. The inherent output capacitance of the plate C_S sums up with the input capacitance of the TIA C_I and the stray capacitances of the interconnects, which makes up the total capacitance at the input node C_T that could be several pF. The equivalent resistance at that node is mainly defined by the low input resistance R_I of the TIA, which is given by

$$R_I = \frac{2R_F}{A_{\text{OL}}} \tag{3}$$

where R_F is the feedback resistance, and A_{OL} is the open-loop gain of the operational amplifier. Assuming realistic reference values, the associated time constant easily lies in the order of a few nanoseconds and the capacitive load of the AFE is no more a key limitation to the bandwidth of the Hall-effect current sensor.

It is important to highlight that the current-related sensitivity, S_I, of the Hall sensor operated in current mode is different from that of one operated in voltage mode and they are not comparable. The two sensitivities can be, respectively, expressed as [35]

$$S_{I_I} = \frac{I_H}{I_{\text{bias}} B_z} \quad [T^{-1}] \tag{4}$$

$$S_{I_V} = \frac{V_H}{I_{\text{bias}} B_z} \quad [\text{V/AT}]. \tag{5}$$

C. Common Mode Control

Regardless of the operation of the X-Hall in either voltage or current mode, the transduction gain, also known as the absolute sensitivity of the Hall plate, $S_H = I_{\text{bias}} S_I$, is proportional to I_{bias}. Then, higher bias currents and voltages are beneficial to improve S_H, implying the connection of the Hall plate to a rather high-voltage supply (e.g., 5-V supply). On the contrary, the TIA would benefit from the exploitation of low-threshold transistors at low voltage supply (e.g., 1.2-V supply) to achieve wider bandwidth, leveraging the higher transition frequency. This creates an interfacing problem at the AFE input side since it should work with input common-mode (CM) voltage levels higher than its supply voltage. Moreover, the X-Hall probe is dc biased by two currents that may be different from the nominal value or can drift apart in response to temperature variations, altering the output CM voltage of the probe during operation.

To cope with these problems, the sensor system has two different dual supplies with a common ground, and a CM feedback is implemented to force the CM output voltage of the Hall plate to ground. The principle of the feedback system is reported in Fig. 6. The error between the X-Hall CM output voltage and ground is nulled by the feedback amplifier, which drives the two opposite bias contacts that should be connected to a low-impedance node. In this way, the voltage bias across the Hall plate, with equivalent resistance R, is adjusted so that the CM output voltage is ideally nulled for an amplifier with infinite open loop gain A, following the equation:

$$V_{\text{CM}} = \frac{R I_{\text{bias}}}{1 + A}. \tag{6}$$

III. Architecture

The architecture of the complete broadband current sensor is illustrated in Fig. 7. A detailed description of the main subsystems will follow. The overall transduction gain of the system, G, is based on the model, $G = G_{\text{IB}} S_H G_{\text{ELE}}$ where the multiplication terms are the current-to-magnetic field transduction factor, the gain of the Hall probe, and the gain of the electronic front end, respectively.

A. I–B Transducer

The transduction of the current into a magnetic field incident on the Hall probe is realized by the flow of the input current I_{IN} through an on-chip 174-μm-wide metal path shaped as an "S" and realized using the top copper layer. The copper track can conduct dc, ac, or transient power currents up to 3 A according to the electromigration prevention rules. The shape of the track was chosen to focus the transduced magnetic field on the Hall probes, thus supporting a higher current-to-magnetic field transduction factor G_{IB}. The magnetic field over the Hall probe is inhomogeneous and the Hall voltage will be proportional to the weighted average of field distribution on the surface of the probe, affecting G_{IB}. However, finite-element method (FEM) simulations of a simplified model of the copper trace reported an estimated G_{IB} of 7.5 mT/A, which is an improvement over our previous design of a straight metal strip, having $G_{\text{IB}} = 2$ mT/A. Two X-Hall probes are placed

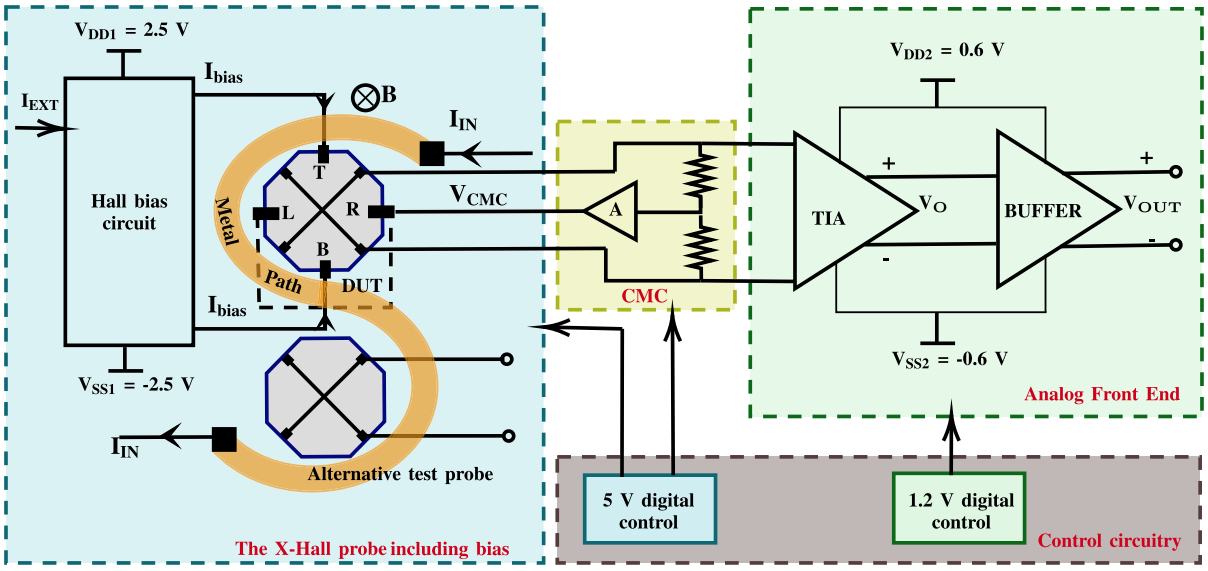

Fig. 7. Block scheme of the proposed X-Hall sensing system in current mode.

in between the curvatures of the metal trace. One probe is connected to the TIA, while the second one is used for testing. Alternatively, the second Hall probe could also be used to realize a differential configuration to null the interferences due to external magnetic fields.

B. X-Hall Probe

The probe is realized in BCD technology as an octagon shape. The active layer is made using a low-doped n-well typically used for high-voltage devices. Sense contacts with a resistance of a few Ohms are smaller than the bias contacts to minimize parasitic capacitances and increase sensitivity. The active area of the Hall probe is inscribed in a circle with a radius of about 40 μm, and the total physical area occupied by each Hall probe is 7845 μm^2. The area of each bias and sense contact is 8.9 and 3.6 μm^2, respectively. To ensure reverse biasing of the p-n-junction, the p-well and the chip substrate are connected to V_{SS1}. When biased, the probe is contemporarily excited in four orthogonal directions, keeping a uniform current density distribution within the active region. The sensor is biased by two 1-mA currents applied at two opposite bias contacts (see Fig. 7). TCAD simulation of the X-Hall probe in current mode resulted in a maximum current I_{probe} of 3 μA for a bias current of 1 mA and applied magnetic field of 50 mT. The current I_{probe} (in any case lower than a few μA) flowing through the "X" is approximately 1 million times lower than the measurand current I_{IN} and generates a negligible magnetic field distribution over the probe.

C. Common Mode Control

The common-mode voltage control (CMC) block computes the CM voltage using a resistive divider network placed at the interface of the X-Hall probe with the AFE. The series equivalent of the divider, parallel to the TIA input resistance, is about 200 kΩ, affecting the signal magnitude by about 0.3%. The computed CM voltage is then negatively fed back to the

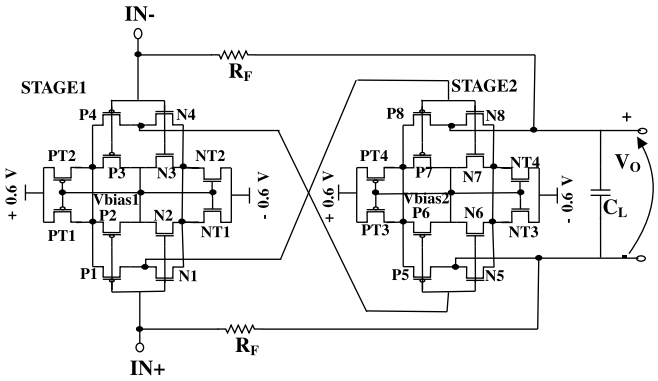

Fig. 8. Circuit schematic of the TIA.

L and R bias terminals of the X-Hall probe, so that its output stays compliant with the CM input voltage range criteria of the TIA. The CMC circuit also improves the stability performance since the X-Hall is forced to work with a mid-voltage fixed to the ground. The feedback amplifier operates at an open-loop gain of 37 dB and with bandwidth limited to a few kHz.

D. Analog Front End

The readout circuit is powered at 1.2 V benefiting from the high transition frequency of low-voltage transistors to widen the acquisition bandwidth of the front-end. It is based on a selectable-gain, resistive-feedback TIA designed as a two-stage, fully complementary, and fully differential amplifier, as shown in Fig. 8. Each single stage incorporates within it a negative feedback loop formed through the bias transistors PTx and NTx and the node voltages, Vbias1 and Vbias2, control the bias against any variations. The open-loop gain of a single stage is 35 dB. For simplicity, the control transistors with their respective control signals are not shown. The TIA architecture is symmetric in terms of schematic and layout and implements a self-biasing scheme for an opamp [36], thus reducing the need for an additional biasing circuit. The amplifier gain is

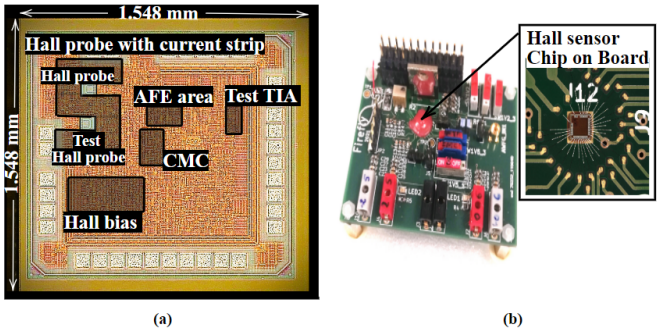

Fig. 9. (a) Chip microphotograph of the X-Hall sensor IC. (b) Picture of the test board developed for characterizing the X-Hall sensor IC with a magnification of the chip-on-board bonding solution.

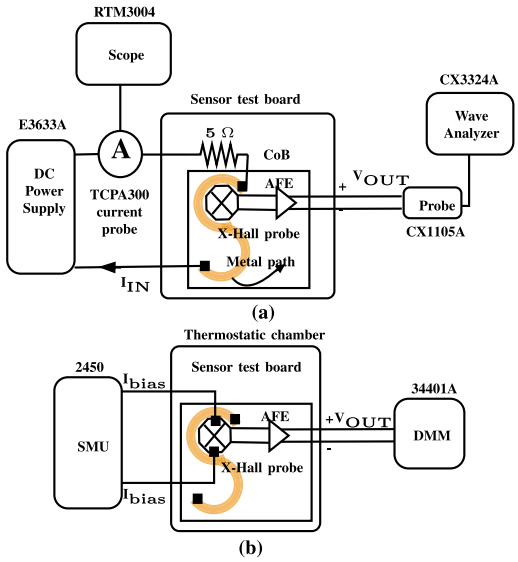

Fig. 10. Measurement setups: (a) Static characterization and (b) offset drift.

set by feedback resistor, $R_F = 90$ kΩ or 200 kΩ, and has a quiescent current consumption of 120 μA. The transistors are sized so that the amplifier is capable of achieving a maximum acquisition bandwidth of 45 MHz when the feedback resistor $R_F = 90$ kΩ and the load capacitance $C_L = 100$ fF. The main drawback of this architecture is its reduced input CM range; however, this issue is solved by the CMC block that sets the input CM voltage of the TIA to ground and limits its variations. Due to the high open-loop gain of nominally 69.7 dB, the input impedance is as low as 65 Ω, thus enabling maximum current sinking from the Hall plate into the AFE and reducing the effect of the parasitic capacitances. In addition, the AFE as a whole consumes a power of only 0.4 mW and an area of less than 0.4 mm^2, while achieving a very high gain bandwidth product (GBW) of 30 GHz. The TIA is followed by another self-biased single-stage buffer to support the system in handling a load up to 5 pF. However, this last stage limits the overall bandwidth of the AFE to about 12 MHz, depending on the highest capacitive load connected to the output.

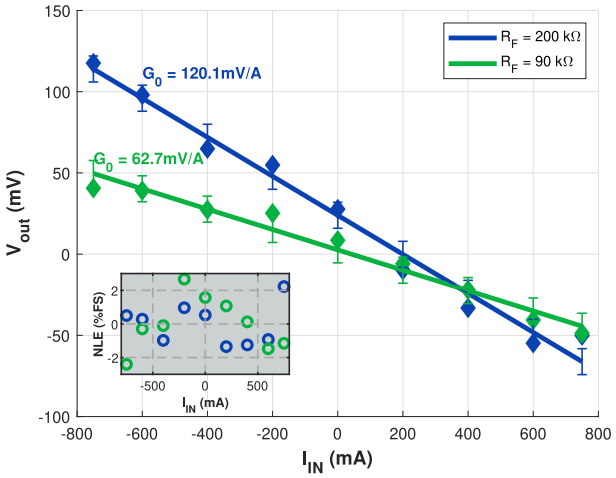

Fig. 11. Static characteristics: output voltage versus input current. The measured NLE as a percentage of full scale of 3 A corresponding to the data points of the main plot is also reported in the inset.

IV. Experimental Results

A. Implementation

The X-Hall sensing system was implemented using a 90-nm BCD technology provided by STMicroelectronics on a total chip area of 2.39 mm^2 with the active area being only 0.511 mm^2 (see Fig. 9). The measured power consumption of the X-Hall probe is 10.98 mW and that of the AFE is only 0.4 mW. The bare die is bonded on the printed circuit board (PCB) with staggered leads and using a conductive glue to provide a better ground connection to the back contact to the substrate (see Fig. 9). A special consideration was taken to minimize the length of the bond wires used to convey the input current and, at the same time, maximize the distance from all the other bond wires. This was done in an effort to minimize the parasitic inductance between the wires that limits the dynamic performance of the sensors [27]. However, due to issues during the assembly process related to the properties of bonding wires, the prototype is limited to a maximum current of 800 mA, although the metal path inside the chip can handle up to 3 A. This limitation can be easily handled in the future using thicker bond wires or moving to other packaging techniques such as solder bumps.

B. Static Characterization

The characterization of the static response was carried out with the setup indicated in Fig. 10. A Keysight E3633A dc power supply connected through a 5-Ω, 35-W power resistor was used to generate the input current through the metal path inside the chip. The applied input current is accurately measured using a Tektronix TCPA300 current probe together with a Rohde and Schwartz RTM3004 scope. The sensor output voltage is measured using a Keysight CX1105A differential probe and a CX3324A waveform analyzer. The prototype does not incorporate a temperature compensation mechanism, which is quite standard [9], and thus, the input current was applied in bursts of 7 s while simultaneously monitoring the temperature over the chip surface to avoid overheating of the

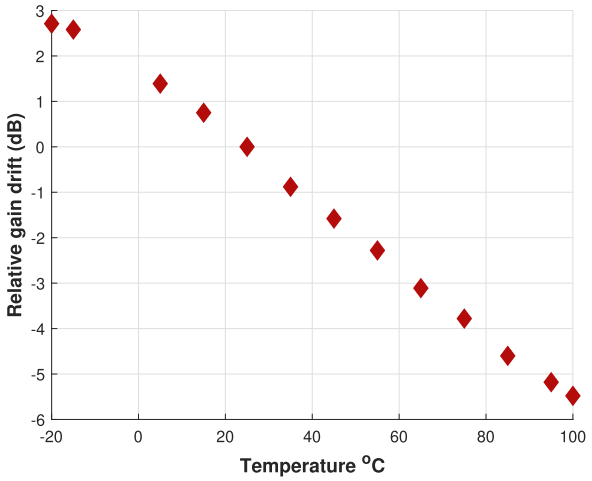

Fig. 12. Transduction gain drift with respect to temperature. The frequency of I_{IN} is at 500 kHz and $R_F = 200$ kΩ.

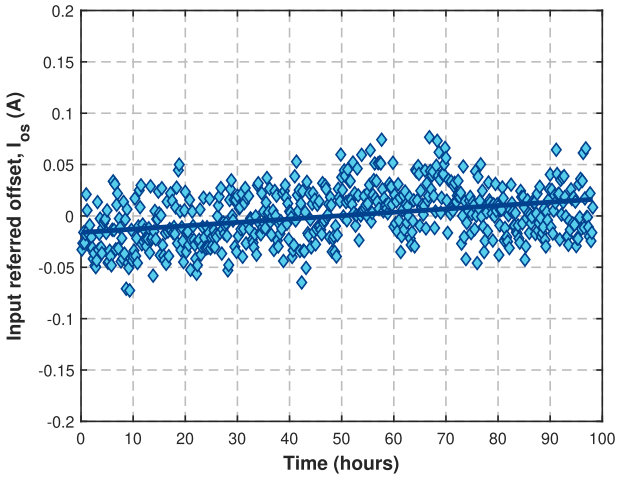

Fig. 13. Input-referred offset drift in time, normalized to the mean of the measurement points. The measurement was carried out at a stable temperature of 27 °C ± 0.5 °C for 98 h. The measurement reports a mean standard deviation of the offset as ±26 mA and a total offset drift of 0.33 mA/h.

sensor with sufficient cool-down time between each measurement. The output voltage was acquired at 16-bit resolution and low sampling rate, and the dc value was estimated by averaging all the samples over a single 7-s-long acquisition. The results of the static characterization are reported in Fig. 11 for the X-Hall probe internally biased at $I_{\text{bias}} = 1.05$ mA and R_F values of 90 and 200 kΩ, yielding a dc sensitivity of the entire system $G_0 = 62.7$ mV/A and 120.1 mV/A, respectively. The nonlinearity error (NLE) is computed for a full-scale range of ±3 A and is about 2.6%FS and 2.2%FS for R_F of 90 and 200 kΩ, respectively, over the measured range (see Fig. 11). The NLE is an optimistic underestimate of the real value as the sensor could not be excited to its full scale. Furthermore, if we assume that G_{IB} is aligned to the simulation value of 7.5 mT/A, the practical values achieved of G_0 corresponds to a mean current-related sensitivity, S_{I_I} of 8.6% T^{-1} with the variability accounting to an exact value of R_F of 90 or 200 kΩ. The achieved S_{I_I} is greater than the stated sensitivity of 6.86% T^{-1} for a cross-shaped Hall sensing system in current mode [37]. Finally, the gain spread of the system across the temperature range was experimentally evaluated as in Fig. 12, and it is found to be around ±4 dB over the entire temperature range. Note that a temperature compensation circuit is usually implemented in the state-of-the-art Hall sensors while this prototype has no analog temperature compensation.

C. Offset

The nominal input-referred offset of the tested prototype is 224 mA (defined as the input required to null the output) at 25 °C, as shown in Fig. 11, and it is found to be long-term stable, facilitating one-point compensation. To evaluate the stability of the offset under temperature and time variations, the setup indicated in Fig. 10(b) was used. The prototype, with R_F set to 200 kΩ, was placed inside an ACS DY110(T) climatic chamber with controlled temperature.

The variability of the offset with respect to time was evaluated at zero input over 100 hours with an Agilent 34401A digital multimeter (DMM) recording the offset voltage at an interval of 10 min and the internal temperature of the thermostatic chamber set to 27 °C ± 0.5 °C. The Hall probe was externally biased using the Keithley 2450 Source Meter Unit. The result of this experiment, shown in Fig. 13, reports a dispersion of the input-referred offset at a stable temperature of ±26 mA with a drift of 0.33 mA/h, which correspond to a dispersion of ±197 μT and a drift of 2.5 μT/h.

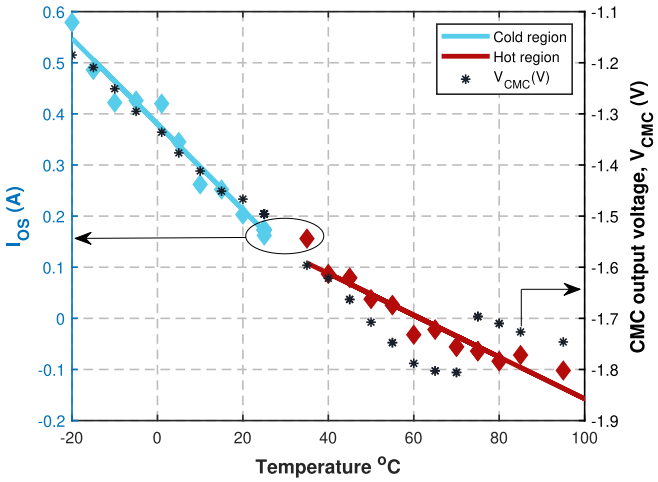

Fig. 14. Input-referred offset drift with respect to temperature, TC (cold region) = −8.4 mA/°C, TC (hot region) = −4.1 mA/°C.

Fig. 14 reports the dispersion of the input-referred offset current of the prototype in the ambient temperature range of −20 °C to +100 °C. The temperature was swept in both the directions of heating and cooling using the climatic chamber to check for possible hysteretic behavior. The mean of 20 sample values of the output offset voltage V_{OS} was recorded by the DMM at each temperature point and then referred to the input of the system mathematically to obtain the input-referred offset, $I_{\text{OS}} = V_{\text{OS}}/G_0(T)$, where $G_0(T)$ is the dc gain of the system expressed as a function of temperature T. Least-squares linear interpolation of the measured data separately in the cold region (−20 °C to +30 °C) and the hot region (+31 °C to +100 °C) resulted in two different temperature coefficients of −8.4 mA/°C and −4.1 mA/°C,

TABLE I
STATE-OF-THE-ART COMPARISON

Parameter	this work	[27]	[37]	[14]	[38]
Supply voltage (V)	5/1.2	5	3.3	1.8/3.3	1.8
Sensor type	X-Hall	X-Hall	Hall	Hall +coil	Hall +coil
Spin/chop	No	No	Yes	Yes	Yes
Mode	Current	Voltage	Current	Voltage	Voltage
Tech node (μm)	0.09	0.16	0.18	0.18	0.18
Area (mm^2)	2.4	4	1.54	4.6	3.17
Sensor BW(MHz)	12/10	4	0.03	1.8	75
Power(mW)	11.46	27.5	15.4	19.5	33.7
Resolution (mA_{rms})	39.16 (293 μT)	75	(52 μT)	64	150
I_{OS} (mA)	224* (1.38 mT)	280	(100 μT)	268.5	N.A
FoM [14] (MHz/A^{2}mW)	569**	25.8	N.A	22.5	99

* The I_{OS} is indicated for one tested chip sample, while the values indicated in SOTA are computed for a mean over samples.
**The lower limit of BW is used for the computation of FOM

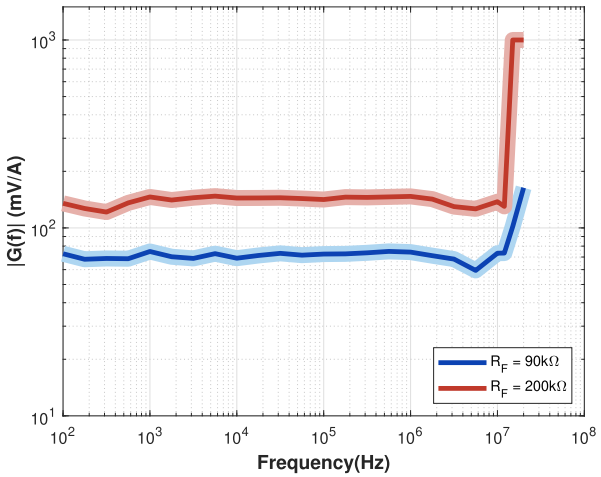

Fig. 15. Transduction gain as a function of frequency.

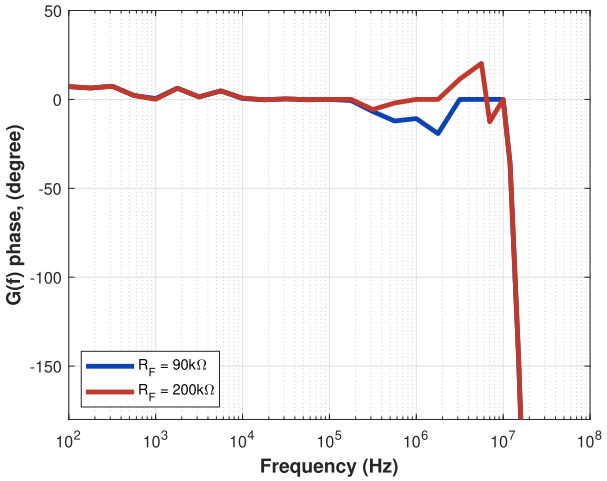

Fig. 16. Phase response as a function of frequency.

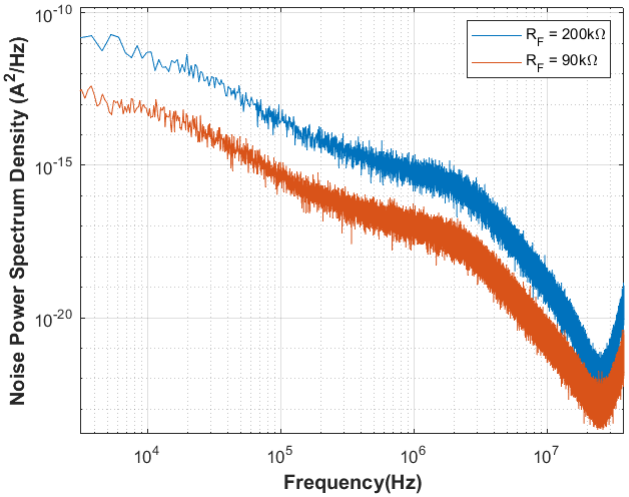

Fig. 17. Noise power spectral density.

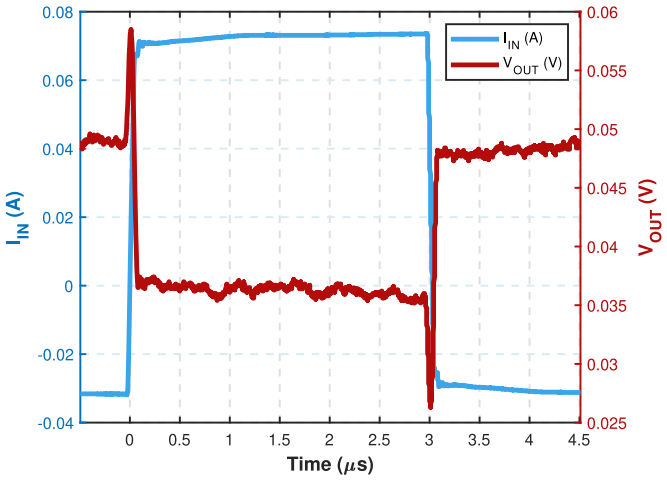

Fig. 18. Transient response of the system to a 100-kHz pulsed input current of 50 mA_{rms}. The observed delay in response is 25 ns.

respectively. Considering the sensor would most likely operate in the warmer region in practical application, then the proposed sensor is more stable than the voltage-mode X-Hall sensor described in [27], which reported TC = 5.5 mA/°C, and slightly higher to TC = 2.4 mA/°C of standard spun Hall sensors [32]. In addition, the variation in the voltage V_{CMC} generated by the CMC block is simultaneously measured. The resistance of the Hall probe changes with temperature, and with a constant I_{bias} would alter the output CM voltage of the probe, risking the exposure of AFE to a higher voltage. V_{CMC} counteracts this variation due to temperature, always attempting to force the output CM voltage to ground, hence demonstrating the functionality of the CMC block.

D. Dynamic Characterization

The measurement setup was modified, and the transfer function of the prototype is estimated by applying a sinusoidal input current of 37 mA_{rms} using the RTM3004. The input current flows through the 5-Ω power resistor soldered on the test board before flowing through the metal trace within the chip. The input current is measured and controlled using the Tektronix TCPA300 current probe. The differential voltage at the output of the sensing system is acquired using the 45-MHz differential probe CX1105A and observed on the CX3324A

scope. The amplitude of the applied current is limited by the available instrumentation and it is below the minimum detectable signal (MDS) of the sensor, and therefore, the scope is used in averaging mode over an adequate number of waveform capturing to enhance the experimental resolution on the output voltage. Acquiring both the stimulus current and the output voltage on the CX3324A scope allows accurate synchronization and minimum time skew. Ten frequency points per decade were acquired in the 100 Hz - 20 MHz frequency range. The plot of the transfer function obtained with the Hall sensing system internally biased at 1.05 mA and its corresponding phase response are shown in Figs. 15 and 16. Fig. 15 clearly demonstrates achieved bandwidths of 10 and 12 MHz for the case of $R_F = 200$ kΩ and $R_F = 90$ kΩ, respectively. Above these frequency values, perturbative inductive effects due to the bondwires come into play, as also observed and discussed in [27]. The shaded region corresponds to the standard uncertainty of measurement and is in the order of tens of μV/A. To the best of our knowledge, this prototype implemented using a standard CMOS process demonstrates the highest acquisition bandwidth compared with the state-of-the-art purely Hall-effect sensors.

The input-referred noise power spectrum density of the sensor is shown in Fig. 17. The total in-band noise (dc-20 MHz) referred to the output of the system is 4.7 mV_{rms}. Referring the rms noise to the main input of the current sensor leads to $i_{in,tot} = 39$ mA_{rms}. To compare with the state-of-the-art Hall sensors, we use the conventional figure of merit also used in [14]

$$\text{FoM} = \frac{\text{Bandwidth(MHz)}}{\text{In-band noise power}(A_{\text{rms}})^2 \cdot \text{Power(mW)}}. \quad (7)$$

Table I summarizes at a glance the performance of state-of-the-art Hall sensor designs. The purely Hall sensor proposed in this work achieves the highest bandwidth with a low power consumption and the highest FoM without using the SCT. It can also be observed that as a necessary tradeoff, the performance in terms of offset is not the best reported, but is still comparable to the values in some similar works.

E. Validation

The capability of the proposed system to sense very fast current events is validated in the acquisition of a pulsed current stimulus of 100 mA_{pk-pk} with a frequency of 100 kHz, 30% duty cycle, and trail edges of 50 ns, as shown in Fig. 18. The figure compares the applied current, acquired using the commercial TCPA300 current probe, with the output of the system. The 100-mA_{pk-pk} pulse is transduced into a 12-mV_{pk-pk} pulse at the output with peaks added on the trailing edges due to the high-frequency inductive parasitic element. Despite this stray effect, the prototype demonstrates a delay in the response as short as 25 ns.

V. Discussion

In view of the above results, it is comprehensible that by replacing the SCT, the realization of a broadband current sensor with a rather low offset is possible owing to the self-compensating architecture of the X-Hall probe. With suitable microelectronic signal conditioning, such a broadband capability could also be achieved by other devices found in the literature. The symmetrical attribute of the X-Hall causes the bias contacts to source and sink the same amount of current improving offset reduction. Another innovative device with such a self-compensation was proposed in [39] wherein two Hall devices were integrated to share an active region and each had contacts placed in a single row mirrored to each other. The geometrical symmetry is such that the offset generated by the two devices cancels each other resulting in a residual offset hundreds of times lower than single standard devices. In fact, electrical symmetry could improve the single-mode and residual offset by a factor of almost 10 as demonstrated in [40], by orthogonally coupling four identical three-contact vertical Hall devices. The resulting offset was of the order of a few microvolts tested at the wafer level. When it comes to architectures without self-offset compensation, Banjevic et al. [41] also benefitted from symmetry by realizing a CMOS quasi-differential magnetic angle sensor with eight contacts embedded in a circular vertical Hall device with a hole. The sensor operated in voltage mode and achieved a high bandwidth of 1 MHz limited by SCT and at the cost of the lowered measurement range. The sensitivity of the vertical Hall devices is also more than ten times lower compared with the planar Hall devices such as the X-Hall in which case one might have to make a choice subject to the context of the application. Another potential candidate that exploits symmetry could be the enhanced version of silicon MAGFET [42], the chopper-stabilized magnetic field effect transistor (CHOPFET). Unlike MAGFET, it is a square device deploying four split contacts at each angle allowing the use of SCT and hence dynamic offset and noise reduction. Alternatively, a technology shift could be beneficial, such as to the GaN Hall devices with a thermally stable offset which is almost comparable to the residual offset of the self-compensation architectures [43].

Furthermore, temperature compensation is also an essential design challenge for any sensor. The work proposed in this article primarily focused on achieving bandwidth enhancement without a specialized technique to cope with the thermal stability of the gain and reliability under variant temperature conditions which are prerequisite for several industrial and real-time power electronic applications. Interestingly, it will be one of the main challenging objectives for future research activity to address this setback, while preserving the broadband capability to achieve even higher industry-level standards.

VI. Conclusion

In this work, we demonstrated a broadband dual-supply integrated current sensor for measuring currents in the ampere range. The broadband capability of the sensor is granted by the X-Hall architecture operated in current mode, which removes the methodological bandwidth limit of the SCT and reduces the effects of parasitic capacitances at the probe–AFE interface. The AFE is realized by a resistive feedback TIA supplied at the lower power domain of 1.2 V to exploit the fastest transistors. A CM control circuit is used to align the CM voltage of the X-Hall probe and the TIA, which

are connected to different power domains. The sensor features a remarkable performance with a maximum acquisition bandwidth of 12 MHz, a resolution of 39.16 mA_{rms}, and a power consumption of 11.46 mW, leading to a figure of merit 25 times better than the state of the art.

However, the bandwidth of the prototype is still limited by the inductive parasitic effect, which has been minimized but unsolved. Lead-free packages with flip-chip assembly should completely resolve the problem. This will be investigated in the future. Despite the presence of the parasitic effect, the sensor has been validated in the acquisition of fast current pulses, reporting a delay of the sensor response of only 25 ns, comparable to the trail edge of the current pulse. The prototype shows also good input-referred offset, which is granted by the high value of G_{IB} provided by the S-shaped copper trace realized on the top metal layer. Due to the limitations in the wire-bonding procedure of the prototype, the measured current range for now was restricted to 800 mA and this will be addressed in future designs by opting for a stud-bump mount. Moreover, as previously discussed, the architecture would benefit from a temperature compensation scheme to cope with the temperature drift of the Hall sensitivity and offset.

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