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Experimental evaluation of Hall-effect current sensors in BCD10 technology

Gian Piero Gibiino [a,c,*], Marco Marchesi [b], Marco Cogliati [b], Sana F. Syeda [a], Aldo Romani [a,c], Pier Andrea Traverso [a], Marco Crescentini [a,c]

[a] Department of Electrical, Electronic, and Information Engineering (DEI), University of Bologna, Italy
[b] STMicroelectronics, Analog and Smart Power Technology R&D, Italy
[c] Advanced Research Center on Electronic Systems (ARCES), University of Bologna, Italy

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ABSTRACT

A new version of the X-Hall broadband current sensor implemented in the BCD10 process by STMicrolectronics is experimentally characterized by means of static, magnetic, and thermal measurements. The results are comparatively assessed against the same topology implemented in a previous BCD generation as well as against a reference square-Hall sensor in the same BCD10 process and operated under the spinning current technique. The sensors realized in BCD10 technology are here presented for the first time. This experimental study demonstrates that the BCD10 technology generally improves sensor sensitivity for all the topologies under analysis. In particular, it offers a 10% increase of the current-to-magnetic field transduction factor, and almost a two-fold improvement of the current-related sensitivity for the X-Hall sensor.

1. Introduction

Current sensors are essential components in modern power electronics, with a range of applications including control feedback loops in power converters [1,2], monitoring and diagnostic functions in power systems [3,4], and power metering in smart grids and smart homes [5,6]. These applications require current sensors with characteristics that are becoming increasingly demanding in terms of size, power consumption, accuracy, bandwidth, etc.

Among the possible solutions, Hall-effect current sensors (HECSs) are widely used for accurately measuring electrical currents in a variety of applications, including power converters, motor drives, and renewable energy systems. HECSs operate by sensing the magnetic field generated by the current flowing through the conductor. They typically consist of a Hall probe and an output analog front-end, which includes signal conditioning and amplification [7]. When optimized to operate with minimal power loss, they are suitable for integration into more complex systems to enable compact and efficient designs.

In recent years, there has been a significant increase in the research on the characterization and optimization of HECSs [8–13]. For example, advanced silicon-based process platforms such as BCD (Bipolar, CMOS, and DMOS) offer the potential for improved performance, enabling the development of new magnetic approaches for lossless current sensing that can be implemented in silicon chips and can provide both accuracy and broadband capabilities.

One of the most promising current sensing topology is based on the X-Hall probe [13,14], which boasts a wide bandwidth and small size, making it suitable for use in space-constrained applications. However, the X-Hall technique might display suboptimal behavior concerning sensitivity and offset. Provided that the broadband capability of the X-Hall sensor does not depend on the technology platform, instead of addressing these issues by further complicating the sensor topology, they can be mitigated at the technology level through specific process steps for optimizing the active region, increasing the isolation, and miniaturizing the metal stack.

This work presents the experimental evaluation of the static behavior of an X-Hall sensor implemented in Silicon 90-nm BCD technology version 10 (BCD10) by STMicroelectronics. The potentiality and improvements offered by BCD10 are analyzed by comparing experimental results with those from similar X-Hall devices realized in the previous version of the process (sensor technology comparison) as well as those from a square-Hall sensor operated using the well-known spinning-current technique (sensor topology comparison).

The article, which is an extended version of [15], is structured as follows. Section 2 provides the description of the BCD10 process, highlighting the main differences with respect to the previous generation featuring Hall-effect devices (BCD8). Also in Section 2, the working principles and features of both square-Hall and X-Hall topologies are briefly described. In Section 3, after introducing the on-wafer measurement set-up employed to perform the static characterization, the statistical analysis of the current-related sensitivity and residual offset are reported across process spread. The sensitivity related to magnetic field is also investigated. Section 4 is dedicated to the evaluation of

* Corresponding author.
E-mail address: gianpiero.gibiino@unibo.it (G.P. Gibiino).

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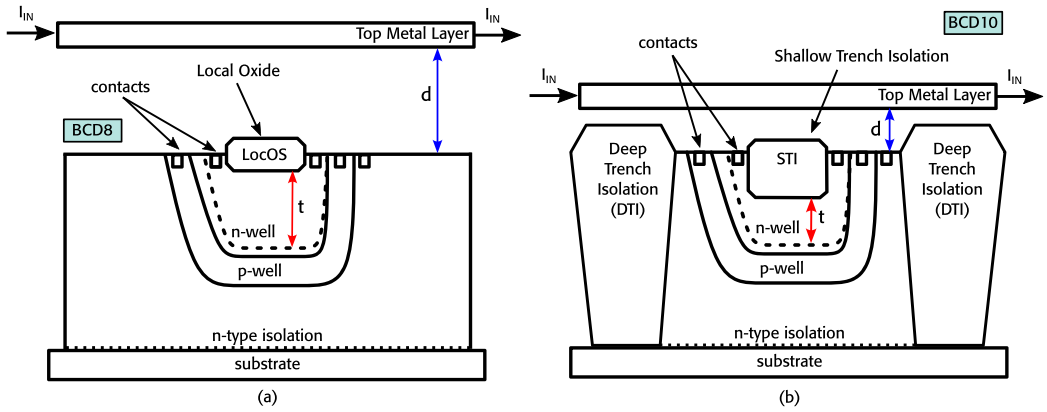

Fig. 1. Cross-section of the device stack for the silicon BCD8 (a) and BCD10 (b) technology by STMicroelectronics.

quantities influencing the static performance of the X-Hall sensor, in particular addressing the junction field effect and the dependency on temperature. A summary discussion related to the trade-offs across the various sensor implementations is provided in Section 5, while conclusions are drawn in Section 6.

2. Description of the sensors

2.1. BCD10 process technology

BCD is a family of process technologies that combines Complementary Metal-Oxide-Semiconductor (CMOS) for digital processing, bipolar transistors for analog functions, and double-diffused MOS (DMOS) for power applications ranging from low-voltage (<40 V) to high-voltage (>600 V) classes. It also includes passive components such as resistors, capacitors, transformers, and non-volatile memories. BCD was introduced by STMicroelectronics in 1984 and has since undergone continuous improvement, including the scaling down of CMOS from 4 μm of the first generation (BCD1) to 90 nm of the latest BCD10.

The increasing number of applications and corresponding performance specifications have also led to an expansion in the number of available voltage classes and device types to be integrated. Specifically, three development lines for integration have been pursued for high-voltage, high-density, and high-power features, respectively. High-voltage BCD often employs a Silicon-on-Insulator (SOI) substrate instead of a bulk substrate in order to address critical requirements in terms of current leakage and parasitic capacitance. High-power BCD features relaxed specifications in terms of area occupation, in order to make it compatible with high current density. Finally, high-density BCD targets Very Large Scale Integration (VLSI) and it is compatible with advanced CMOS.

The high-power BCD process line is mainly intended for smart power applications, which exploits the presence of high-power devices together with short-channel devices for on-chip control features. In this context, the BCD technology would benefit by the addition of on-chip isolated current sensors to extend the range of available control features that can be realized directly on-chip.

The HECSs considered in this work are designed in BCD10 technology, which employs an n-type diffusion layer as the active region within a p-type encapsulation well. The realization of the HECS does not require additional mask sets because it makes use of the 60-V tolerant n-type diffusion layer already available in the BCD10 process line. In comparison to previous implementations based on the BCD8 [10,13], the active well features a different doping level and it is covered with shallow trench isolation (STI) instead of field oxide (see Fig. 1). This change reduces the effective thickness of the active region, which should increase the sensitivity. Additionally, the Hall probes are isolated laterally using deep-trench isolation (DTI) regions, allowing them to be placed closer to high-voltage devices. Furthermore, the metal stack in these sensors has smaller dimensions, reducing the distance between the top metal layer and the active region. This configuration is intended to enhance the incident magnetic field on the Hall probe originating from the input current flowing through the copper trace on the top metal layer [7], further increasing the overall sensitivity of the sensors.

2.2. Square-Hall topology

The first HECS under consideration, here used as a reference sensor, is realized as a square-shaped n-well with one contact at each corner (four in total), as shown in Fig. 2a. More in detail, the whole sensor is composed by one Hall plate connected in parallel to another 90°-rotated plate, so to minimize the piezo-Hall effect [16].

Such a composite device is operated using the spinning current technique (SCT) [17], which is the state-of-the-art methodology employed to compensate for the generally high intrinsic offset of the Hall probe. It consists in exploiting the symmetry of the device by continuously interchanging the bias and sense contacts in order to rotate the biasing current and the readout voltage in a phased manner for a given number of phases (four phases in the typical configuration).

Due to the reciprocity of the Hall plate, a 90° spatial rotation of the bias current reverses the sign of the additive offset voltage $V_{OS,plate}$ on the sensed voltage. In this way, the readout voltage at the output is $V^i_{probe} = V_H \pm V^i_{OS,plate}$ during the ith phase. After one complete rotation, the measured voltages are averaged out to obtain a final estimate of the Hall voltage:

$$V_{OUT} = \frac{1}{4}\sum_i V^i_{probe} = V_H + \Delta V_{OS}; \tag{1}$$

where ΔV_{OS} is a residual offset due to the anisotropy property of the Hall plate, while the Hall voltage V_H is related to the bias current I_{bias} and the incident magnetic field B_z by the current-related sensitivity S_I:

$$V_H = S_I I_{bias} B_z. \tag{2}$$

The general expression for the current-related sensitivity is

$$S_I = G_H \frac{r_H}{nqt}; \tag{3}$$

where G_H is the geometrical correction factor, r_H is the Hall factor, t is the effective thickness of the active region, n is the volumetric carrier concentration on the active region, and q is the electron charge [7,16]. In the solution under test, an optimum trade-off between the sensitivity and the maximum bias voltage (chosen to be compatible with the available silicon CMOS logic) has been found using a couple of 34 × 34 μm^2 Hall cells connected in parallel.

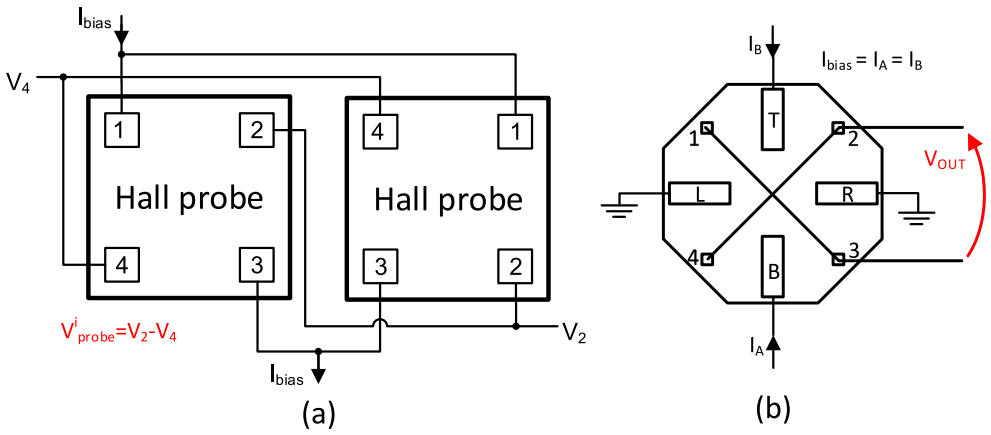

Fig. 2. (a) Top-view of the square-Hall probe during a single phase of the SCT. (b) Top-view of the X-Hall probe.

2.3. X-Hall topology

The second type of HECS here considered is based on the X-Hall topology, which was introduced in [13]. As shown in Fig. 2b, the active region is shaped like an octagon and it features eight contacts: four large ones (T, B, L, R) for applying the bias, and four small ones (1, 2, 3, 4) for measuring the Hall voltage. In this topology, sensing and biasing contacts cannot be interchanged and the SCT cannot be applied. From a process technology perspective, the X-Hall implemented in BCD10 is larger than the one implemented in BCD8 [13]. It is realized as an octagon inscribed in a circle of radius 40 μm with minimum-size sensing contacts, whereas the X-Hall realized in BCD8 was inscribed in a circle of radius 36 μm with larger contacts.

The X-Hall probe is biased at DC to overcome the methodological bandwidth limit of current-spun Hall sensors [18] and, therefore, to maximize the bandwidth. In particular, the biasing is applied by feeding two bias currents through two opposite bias contacts (i.e., B and T), while the other two bias contacts (i.e., L and R) are connected to a low-impedance node, typically a ground node. This configuration creates a uniform current distribution in the active region, while polarizing the probe in four orthogonal directions [13].

The application of two opposite bias currents leads to the generation of two output voltages V_A and V_B displaying an opposite Hall effect:

$$V_A = V_H + V_{OS,plate}^{(A)}; \tag{4}$$

$$V_B = -V_H + V_{OS,plate}^{(B)}; \tag{5}$$

where $V_{OS,plate}^{(A)}$ and $V_{OS,plate}^{(B)}$ are additive offset voltages. Since there is a unique active region, it is reasonable to assume that these two quantities will have the same sign.

The cross-like short-circuit of the sense contacts (Fig. 2b) imposes specific boundary conditions to the charge distribution, implying the following relationship:

$$V_A = V_B = V_{OUT}; \tag{6}$$

which results in the minimization of the offset voltage. Indeed, the only value for $V_{OS,plate}^{(A)}$ and $V_{OS,plate}^{(B)}$ theoretically satisfying the relationships in (4), (5), and (6) is zero. In practice, there will always be local defects asymmetrically affecting V_A and V_B, so that a residual additive offset ΔV_{OS} will still be present in the actual sensor device. Therefore, the output voltage V_{OUT} can be finally written as

$$V_{OUT} = V_H + \Delta V_{OS}. \tag{7}$$

3. Characterization of the sensors

The Hall probes described in Section 2 inherently work as magnetic sensors. However, once the current-to-magnetic field transduction factor (G_{IB}) is known, they can be employed as current sensors to measure the current inducing the magnetic field.

In this implementation, the measurand current (I_{in}) flows through a strip realized on the top metal layer. Given that the process layers are geometrically well-defined, the G_{IB} is well controlled and known. Thus, the overall sensitivity of the HECS can be expressed as a combination of G_{IB} and the current-related sensitivity of the Hall probe (S_I) as [7]:

$$S = G_{IB} S_I I_{bias}. \tag{8}$$

3.1. Measurement set-up

The on-wafer measurement set-up used for the X-Hall is depicted in Fig. 3a, while its photograph is shown in Fig. 4. A similar set-up was used for the square-Hall, with minimal changes required to adapt the measurement to the specific topology. The die, whose photograph is shown in Fig. 3b, features 22 pads contacted by a custom 22-needle DC probe system. The global device supply (V_{DD}) and the bias for the p-well layer (V_p) are applied via two slots of a modular DC supply (Agilent N6705B). The HECS-under-test is biased using a Keithley 2450 SMU with accuracy of 0.012% and 6.5-digit resolution, enabling the direct imposition of the bias current (I_{bias}) in the mA range and the measurement of the voltage at the same bias port (V_{bias}) in the V range.

The measurand current (I_{in}) flowing through the metal strip is generated by applying a DC voltage (V_{in}) to a 10-Ω power resistor via an additional slot of the modular DC supply. The value of I_{in}, which is crucial for accurately characterizing the sensitivity of the sensor, is acquired using a digital multimeter (Agilent 34401A with 6.5-digit resolution) in ampermeter mode (DMM2 in Fig. 3). The output voltage (V_{out}) is acquired using another digital multimeter (Agilent 34401A, DMM1 in Fig. 3) in voltmeter mode.

Based on the same functional setup, additional measurements are carried out on the packaged versions of the same HECSs. They are positioned in a climatic chamber for temperature tests, and within a Helmholtz coil for magnetic sensitivity tests with direct excitation of the magnetic field.

3.2. Process spread

Fig. 5 reports the static characteristics for both the square-Hall and the X-Hall topologies realized in BCD10, respectively considering 34 and 32 *sites* on the same wafer for the two topologies, where the term

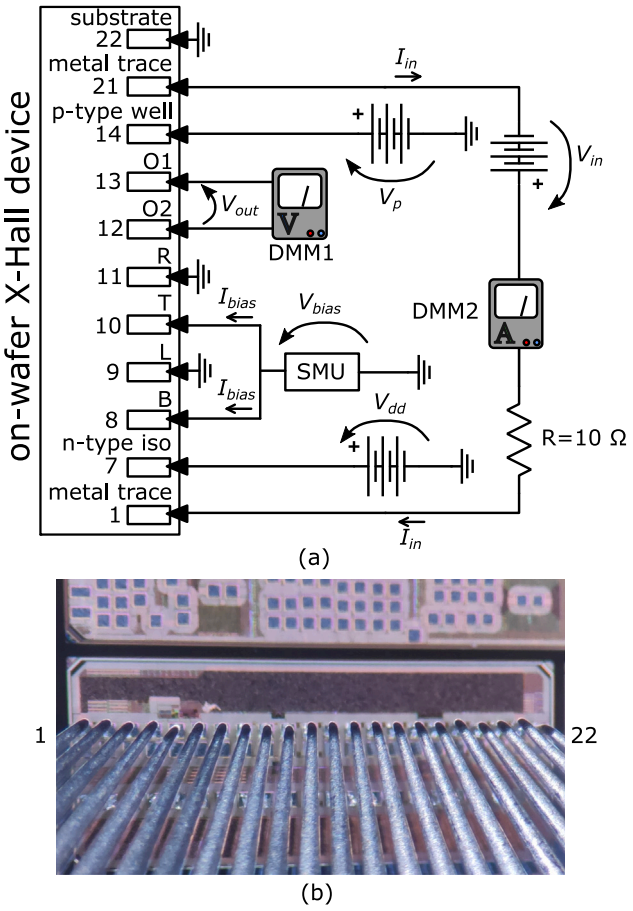

Fig. 3. (a) On-wafer measurement set-up with specific highlight on the pad connections of the X-Hall device. (b) Photo of the X-Hall sensor die contacted with a 22-needle DC probe system.

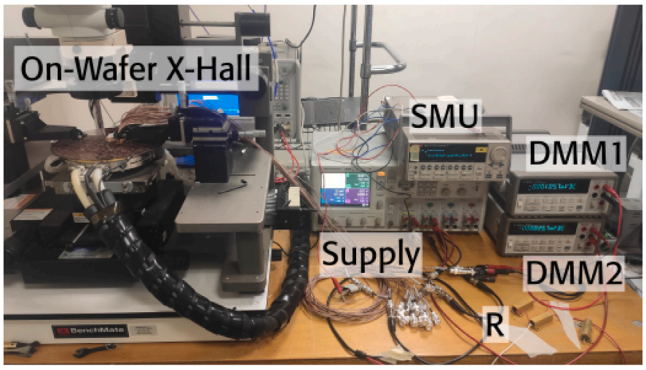

Fig. 4. Photo of the on-wafer measurement set-up including the X-Hall wafer under test.

sites refers to the separate spatial positions of the single sensor devices in a given wafer.

In accordance to the four-phase SCT, the acquisitions for the square-Hall device, biased at I_{bias} = 1.5 mA, were sequentially repeated for four times (one acquisition corresponds to one phase), each time exchanging the connections for biasing and readout. The reported values are thus calculated as the average over the four acquisitions as defined in (1). In order to impose a similar power consumption across the tests, a current of I_{bias} = 0.75 mA per contact was applied at the two biasing contacts (T and B) for the characterization of the X-Hall probe.

All the measured static characteristics are substantially linear over the entire input range, with a maximum deviation from the linear relationship of 33 μV and 15 μV for the square-Hall and the X-Hall, respectively. Fig. 5 clearly shows that the X-Hall topology displays a higher process dispersion and offset, the latter caused by the reduced effectiveness of the static offset cancellation with respect to the SCT [13].

Fig. 6 reports the statistical distribution of the main static parameters of the square-Hall sensor across a 400-mA range for the measurand current. The average overall sensitivity across the tested population is $\bar{S}$ = 1030 μV/A with a standard deviation of 36 μV/A, whereas the average residual offset is $\Delta\bar{V}_{OS}$ = −26 μV with a standard deviation of 30 μV. Also the input resistance of the Hall probe R_{IN}, defined as the resistance shown at the biasing port of the probe during a single phase of the SCT, was estimated. In this case, the average input resistance is $\bar{R}_{IN}$ = 3.34 kΩ with a very small process dispersion, quantified by 0.3 Ω of standard deviation. The mean sensitivity and input resistance are in agreement with the theoretical values.

The measurement procedure over a reduced input range was repeated over a population of 32 X-Hall sensors placed on the same wafer to obtain the process dispersion of sensitivity, residual offset, and input resistance, as reported in Fig. 7. The average sensitivity over the entire test population is $\bar{S}$ = 847 μV/A with a standard deviation of 400 μV/A, whereas the average offset is $\Delta\bar{V}_{OS}$ = −466 μV with a standard deviation of 553 μV. The average input resistance is $\bar{R}_{IN}$ = 2.23 kΩ with a standard deviation of 29 Ω. The X-Hall sensors demonstrate a good sensitivity, comparable to those of the Square Hall, but an offset ten times higher.

Being the X-Hall device realized by utilizing the same type of wells, and being them within the same die of the square-Hall device, similar process dispersion due to doping should be expected. However, the statistical analysis revealed a much higher process dispersion for the X-Hall with respect to the square-Hall device, which could be ascribed to the more complex geometry of the octagon shape. Indeed, edge angles at 135° (45° deviation with respect to the usual masks) imply suboptimal spatial accuracy across the BCD10 process steps. In addition, the absence of a dynamic offset cancellation procedure makes the X-Hall even more prone to geometrical errors and anisotropy effects.

3.3. Impact of technology on X-Hall

The technological innovations of BCD10 described in Section 2 should mostly impact the sensitivity. For both the sensors, the metal stack of the BCD10 allows the measurand current to flow closer to the active area, with an expected improvement on the current-to-magnetic field transduction. As far as the X-Hall is concerned, the longer trajectory of the carriers occurring in a larger probe should increase the sensitivity [19]. At the same time, the larger active area can imply a less focused magnetic field, thus a reduction of the sensitivity. Yet, the smaller bias contacts should increase the sensitivity, but they may imply a larger spread of the offset.

To assess the resulting effect of all these mechanisms, the static response of a single X-Hall sample was measured by directly applying the magnetic field using an external Helmholtz coil, as shown in Fig. 8a. The current-related sensitivity extracted from this data results S_I = 260 V/AT, which is coherent with the statistical analysis of Fig. 7 and it is 13% higher than the X-Hall in BCD8 [10], confirming the positive impact of a larger active area. By combining these results with those reported in Section 3.2, an average current-to-magnetic field transduction of the on-chip trace of G_{IB} = 2.2 mT/A is obtained, which is 10% higher than the one realized by the on-chip trace in BCD8 (2 mT/A), demonstrating the beneficial effect of the reduced distance between the probe and the strip in the top metal layer.

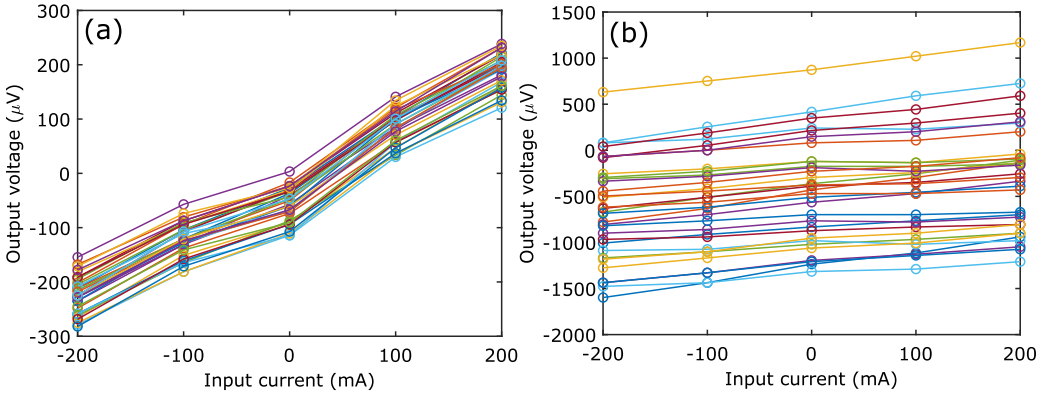

Fig. 5. (a) Measured static characteristic for the square-Hall sensor across 34 sites (I_{bias} = 1.5 mA). (b) Measured static characteristic for the X-Hall sensor across 32 sites (I_{bias} = 0.75 mA).

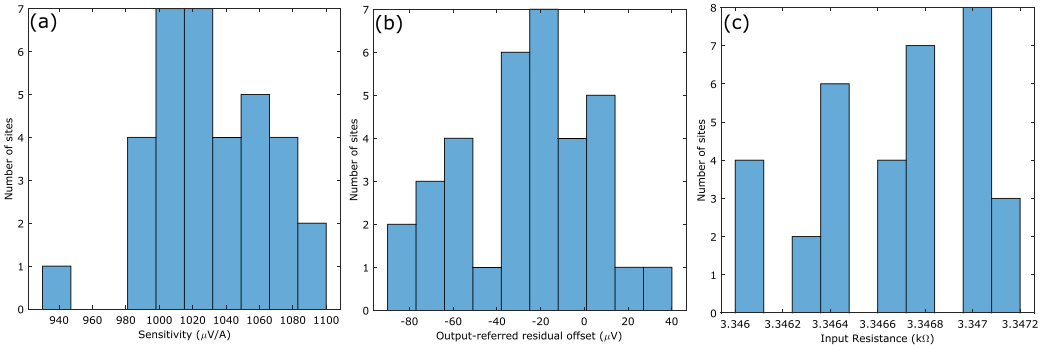

Fig. 6. Distribution of (a) sensitivity, (b) output-referred offset, and (c) input resistance across 34 sites for the square-Hall sensor device in BCD10 technology.

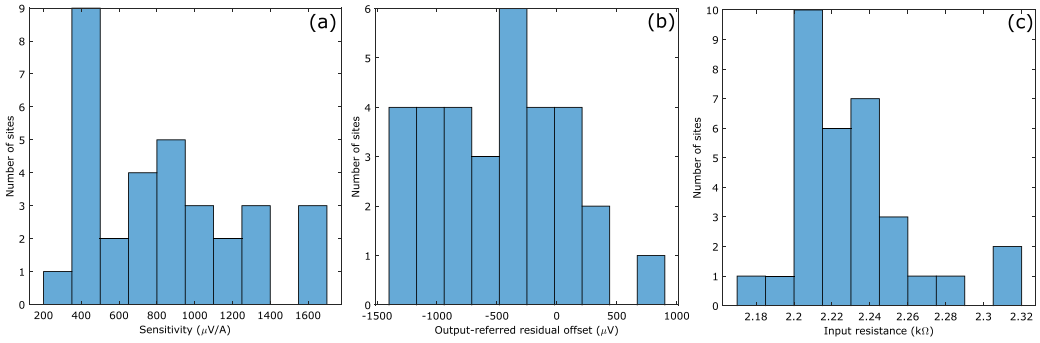

Fig. 7. Distribution of (a) sensitivity, (b) output-referred offset, and (c) input resistance across 32 sites for the X-Hall sensor device in BCD10 technology.

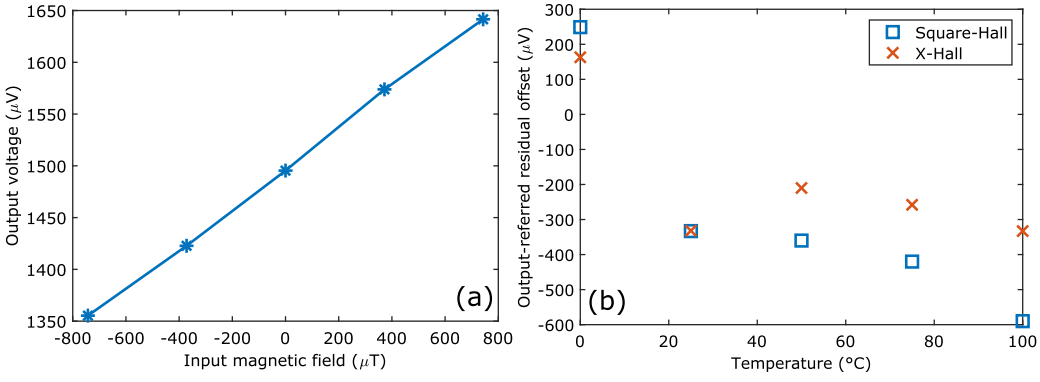

Fig. 8. (a) Voltage output of the X-Hall sensor in the presence of an incident magnetic field generated by a Helmholtz coil. (b) Temperature drift of the residual offset for the square-Hall and the X-Hall in BCD10.

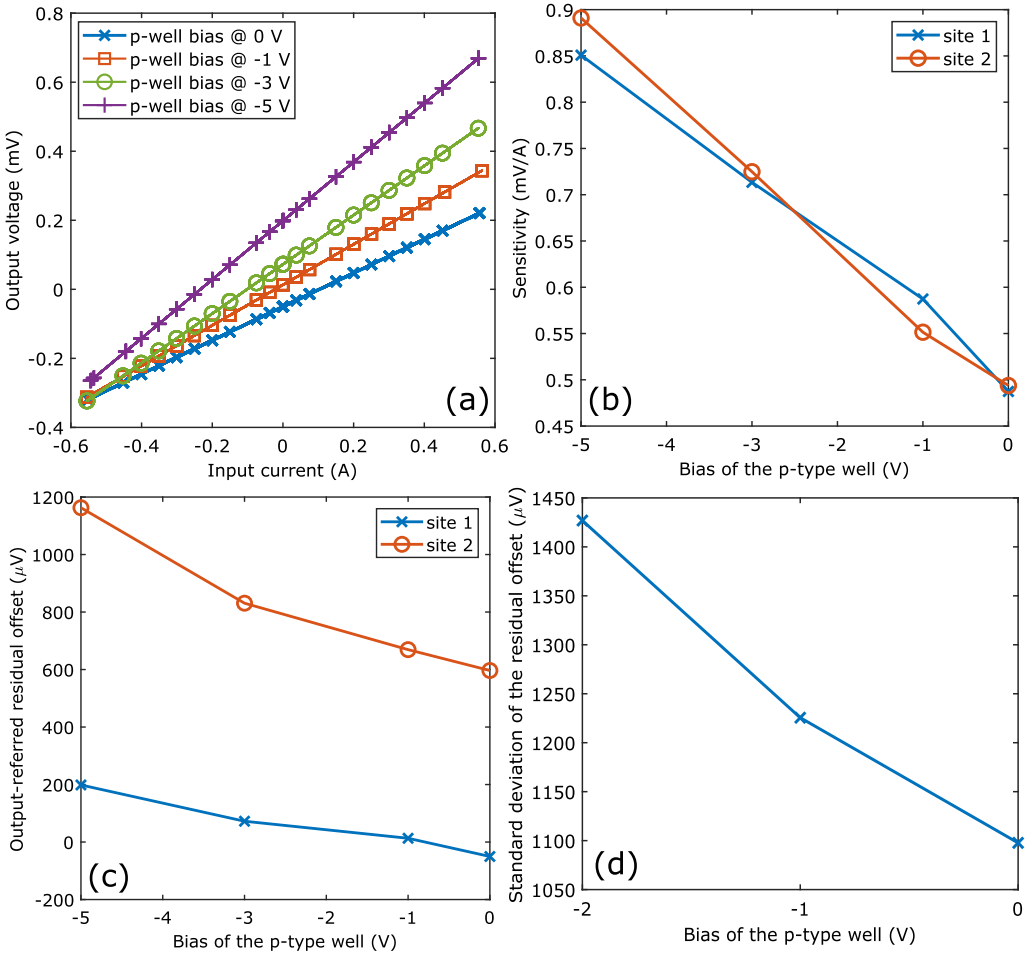

Fig. 9. (a) Static characteristic (single site) of the X-Hall for different polarization voltages of the p-type encapsulation well. (b) Effect of the p-type well voltage on sensitivity (two sites). (c) Effect of the p-type well voltage on the residual offset (two sites). (d) Effect of the p-type well voltage on the standard deviation of the residual offset (calculated across 12 sites).

Table 1
Performance comparison of the X-Hall topology between BCD8 and BCD10 technologies and among different topologies on the same BCD10 platform.

Technology	Topology	$\hat{S}$ (μV/A)	$\hat{V}_{OS}$ (μV)	$\sigma(V_{OS})$ (μV)	R_{IN} (kΩ)	G_{IB} (mT/A)
BCD10	Square-Hall	1030	−26	30	3.34	2.5
BCD10	X-Hall	847	−466	553	2.29	2.2
BCD8	X-Hall	345	100	700	2.50	2.0

4. Assessment of influence quantities

The characterization under nominal conditions, as reported in Section 3, is necessary to estimate the specifications of the HECS. Indeed, by leveraging on this data, calibration techniques could be envisaged to improve the performance. Nevertheless, the actual performance of HECS, and in particular the residual offset, is substantially influenced by environmental factors as well as bias settings, and assessing the impact of such quantities is fundamental from an industrial and commercial perspective.

To estimate the thermal stability of the residual offset, both the HECS topologies were assembled into the same plastic package and placed into a climatic chamber, sweeping the temperature from 0 °C to 100 °C. Note that the plastic package adds mechanical stresses that inevitably act as source of additional offset with its own thermal instability. The results are reported in Fig. 8b, showing that both the topologies present a similar behavior of the drift, despite the square-Hall employing the SCT technique and the pairing of two probes.

Another element of interest concerns the depletion layer resulting at the interface between the active region and the surrounding p-type encapsulation well (see Fig. 1). Such a layer involves the junction-field effect, eventually causing nonlinearity due to the modulation of the effective thickness of the active region [7]. In this context, a negative voltage on the p-type well should allow to further shrink the effective thickness t and achieve higher sensitivity values.

Thus, the effect of the depletion region on the effective thickness t was investigated by repeating the measurement procedure with different negative voltages applied to the p-type well. The measured static characteristics, featuring a much denser current sweep than the one employed for estimating the process spread in Section 3.2, are reported in Fig. 9. When no bias is applied to the depletion layer, the resulting sensitivity and offset values are aligned with those of Fig. 7, while the application of negative voltages nearly doubles the sensitivity for an applied voltage of $V_p = -5$ V. However, as expected, the thinner active region also affects the offset, generally increasing its value (Fig. 9c) yet spreading the offset distribution of the entire population (Fig. 9d).

5. Discussion

The main parameters extracted for the X-Hall sensor realized in BCD8 and BCD10, as well as those of the square-Hall in BCD10, are summarized in Table 1 for comparison. The data for the X-Hall sensor implemented in BCD8 and found in Table 1 is reported from [13] by performing a linear extrapolation of measurements previously obtained at different bias current levels, so to allow for a fair comparison. To

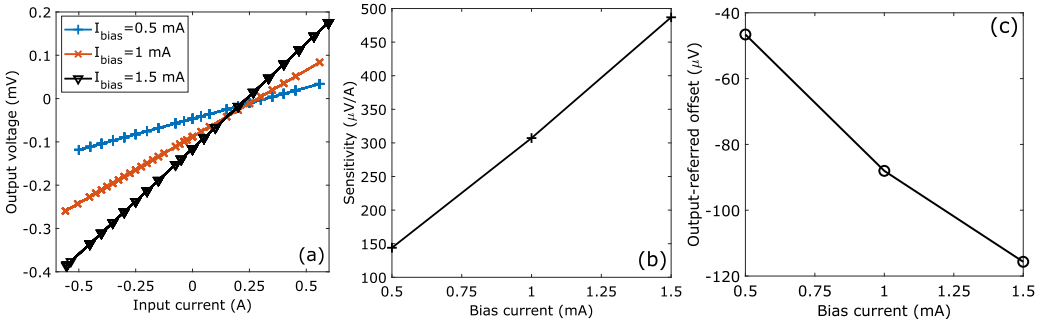

Fig. 10. Effect of the bias current on (a) output voltage, (b) sensitivity, and (c) offset for the DUT in BCD10 technology.

prove the linear extrapolation procedure, the static characteristic of a single sample in BCD10 technology was estimated for three values of I_{bias}, namely 500 μA, 1 mA, and 1.5 mA. Sensitivity and residual offset are estimated from the characteristic and reported in Fig. 10, demonstrating a substantially linear relationship. As can be clearly seen, higher values of I_{bias} improve the sensitivity, but they also increase the residual offset, hindering the accuracy.

As from Table 1, BCD10 technology generally allows for clear improvement in the sensitivity, which is due to both an higher G_{IB} transduction factor and a more sensitive Hall plate. As discussed in Section 3.3, the higher G_{IB} is principally due to the miniaturized metal stack placed closer to the active region. Nevertheless, it should be noted that this solution is of interest only for values of the measurand of up to a few tens of Ampere. Indeed, for higher values, it is not possible to force the input current to flow on the top metal layer due to electromigration limitis.

The X-Hall in BCD10 also displays a high $S_I = 513$ V/AT (as extracted from the values reported in the Table 1), approximately two times higher than the same sensor realized in BCD8 [13]. This improvement can be ascribed to the lower doping level of the active well as well as to the smaller sensing contacts. Small contacts also imply higher offset values, as confirmed by the higher mean offset of the X-Hall in BCD10.

Regarding the comparison between the two topologies in the same BCD10 technology, the square-Hall sensor outperforms the X-Hall sensor in terms offset. This results was expected because of the SCT employed by the square-Hall, which grants a strong offset reduction, yet at the cost of a hard methodological limit in terms of bandwidth [10, 18]. The current-related sensitivity offered by the X-Hall is comparable to that achieved by square-Hall in view of the greater G_{IB} due to a narrower metal strip in the square-Hall implementation.

6. Conclusion

In this work, the X-Hall sensor implemented in the new BCD10 technology provided by STMicroelectronics has been experimentally characterized and compared against a similar device realized in the previous BCD8 technology and a standard HECS topology in the same BCD10 platform. The experimental characterization has been limited to static performance since the broadband capability of the X-Hall sensor does not depend on the technology platform.

The performance comparison here reported outlined the advantages in terms of sensitivity provided by the BCD10 technology. The metal stack closer to the silicon area, the lower doping level of the active region as well as its reduced thickness due to the superficial STI layer led to a global improvement of the HECS sensitivity with respect to the previous technology. The offset spread across process technology is similar to that assessed for the BCD8 technology.

Regarding the comparison between the two sensor topologies realized in the same BCD10 technology, the square-Hall operated by SCT offers the lowest residual offset in terms of both mean value and process spread, resulting in a value that is approximately ten times lower than the one achieved by the X-Hall sensor. Indeed, the static offset compensation realized by the X-Hall sensor has not the same effectiveness of the SCT. Nevertheless, the sensitivity as well as the temperature dispersion of the offset of the X-Hall were similar to those reported by the square-Hall. These substantial improvements allowed by the BCD10, together with its intrinsic broadband capabilities largely outperforming SCT-based HECSs [14], make the X-Hall a promising solution for a wide range of modern applications in which accuracy must be supplemented with adequate sensitivity and large bandwidth.

CRediT authorship contribution statement

Gian Piero Gibiino: Conceptualization, Data curation, Formal analysis, Investigation, Methodology, Resources, Software, Validation, Visualization, Writing – original draft, Writing – review & editing. **Marco Marchesi:** Conceptualization, Data curation, Funding acquisition, Investigation, Methodology, Project administration, Resources. **Marco Cogliati:** Data curation, Investigation, Methodology, Resources. **Sana F. Syeda:** Investigation. **Aldo Romani:** Funding acquisition, Resources, Supervision. **Pier Andrea Traverso:** Resources, Supervision, Writing – review & editing. **Marco Crescentini:** Conceptualization, Data curation, Formal analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Supervision, Validation, Visualization, Writing – original draft, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

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