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Design of a 350 kW DC/DC Converter in 1200-V SiC Module Technology for Automotive Component Testing

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Abstract: In this paper, the design and implementation of a DC/DC converter for automotive component testing with state-of-the art performance is described. The converter is the core of a battery emulator for the characterization and development of automotive batteries, electronic chargers, traction inverters, DC-DC converters, E-motors and E-axles. Cutting edge performance, flexibility and compactness are obtained by exploiting 1200-V SiC modules, high switching frequency, planar transformer technology, suitable topology solutions and fast digital control strategies. The implemented system is a liquid-cooled, bidirectional converter with galvanic isolation capable of 350 kW continuous output power, output voltage range 48-1000 V, continuous output current up to 800 A (1600 A peak), voltage/current ramp-up time below 10/2 ms and 0.1% current/voltage accuracy. The entire instrument is implemented in a standard full-height 19-inch rack cabinet.

Keywords: DC-DC converter; battery emulator; SiC; SiC modules; planar transformer; DAB converter; interleaving; high switching frequency; ZVS commutations; low inductance bus bar; low ESL capacitors

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1. Introduction

Nowadays, the strong drive towards electrification in the automotive sector has made electronic power converters and traction batteries key components of the energetic transition, gaining investments from industrial organizations and attention from the scientific community. In particular, the development of new generations of power converters with enhanced characteristics in terms of power density, efficiency and dynamic response is fundamental to extend the performance of hybrid (HEV) and electric vehicles (EV). High power bidirectional DC-DC converters are used in several parts of the vehicle: as regulators between the high voltage and low voltage DC buses, as voltage booster between the battery pack and the high voltage bus, in on-board and off-board battery chargers and also for lower power applications to drive different points of load in the vehicle. Switching-mode inverters are used for traction and energy recovery in both EV and HEV. Additionally, battery centrality is evident considering that it can represent up to 50% of an Electric Vehicle (EV)'s value [1]. Several technologies are available on the market, such as lead–acid, Nickel and Lithium-ion [2] (even though the last is the most used in the automotive field [3]), with different nominal voltages and characteristics.

The performance of automotive electronic power converters connected to traction batteries as power sources or loads depends on the battery characteristics and state. Since the battery behavior is strongly affected by numerous factors (State of Charge (SOC), State of Depletion (SOD), temperature, humidity, age, etc.), performing tests in different conditions becomes strategic for the development and verification of power electronic components. However, the battery procurement and the pre-conditioning procedure are highly costly

and time-consuming. Moreover, in this way the measurements are not fully repeatable since the battery changes its status in every test cycle. To overcome these issues, a Battery Emulator (BE) system can be employed. The BE is a programmable power electronic system capable of providing a voltage/current profile to a load or to a source, behaving as a real battery. To fulfil this aim, it must be capable of source and sink DC supply behavior (bidirectional current flow). The emulation capabilities are strictly dependent on the BE electrical performance in terms of power rating, accuracy and dynamic behavior and on the battery model used by the control as a reference. Several modeling methods have been reported in the literature, such as the Thevenin-based approach in combination with the Shepard equation [4–6]; however, this is beyond the scope of the paper, which focuses on the BE hardware design and control fulfilment.

In this paper, we describe the design of a 350 kW DC-DC converter, which is the core of a battery emulator set up. Desirable characteristics of the battery emulator are the capability of large voltage/current swings, high accuracy and fast dynamic response; maximizing all these requirements in a compact, easily deployable solution is an important goal for the implementation of a highly flexible instrument that can be exploited in a large set of applications. In particular, the aim of the BE prototype here described is to provide a testing system employable in the development and testing of automotive power converters and batteries, with state-of-the-art performance when compared to existing commercial products [7–10]. For this reason, in this design non-conventional solutions are exploited in terms of circuit topology, power electronic devices and magnetic components. Simulations of the power converters are carried out in PSIM environment [11], whereas the control strategy is implemented in Simulink. For dynamic assessment, co-simulations between Simulink and PSIM are performed.

The paper is organized as follows. In Section 2, the technological choices and the design and simulations of the power system are described; in the Section 3 the control strategy and its implementation are detailed, along with some additional simulations on the dynamic performance of the converter; finally, in Section 4 the system implementation is shown in combination with a preliminary functional test at de-rated power regimens.

2. Power System

The battery-emulator (BE) system envisages the design of a bidirectional (two-quadrant) and isolated DC/DC power converter, comprehensive of digital control board and a sensor network, according to the electrical specifications in Table 1.

Table 1. BE specifications.

Vin	Vout	Iout	Pmax
750 V	48–1000 V	±800 A	350 kW
Current, Voltage ramp-up time	**Current, Voltage reproducibility**	**Current, Voltage ripple**	
<1 ms, <10 ms	$<0.1\%I_{out}$, $<0.1\%V_{out}$	$<0.5\%I_{out}$, $<0.5\%V_{out}$	

To the best of our knowledge, these specifications represent the state-of-the-art specifications in the market of BE instruments for automotive component testing ([7–10]) and are not met by any product within the very limited space of a single standard full-height 19-inch rack cabinet. Several examples of implementations of battery emulator setups can be also found in the scientific literature [12–20]. None of them have characteristics comparable with the specifications of Table 1. The described emulators have limitations in terms of output voltage or current that set their power rating in the range between few kW to tens of kW. Only the system of [16] can deliver up to 500 kW, but its dimensions are very large (six cabinets) due to the use of IGBTs and a line-frequency grid-connected transformer. It is interesting to analyze the different architectures proposed in these publications on BE. In [13–15], the dual active bridge topology (DAB) is proposed, in particular for its advan-

tages in term of isolation, dual power flow, efficiency and ease of control. In [16,17,19,20] a multi-phase interleaved synchronous buck topology is addressed for its characteristics of simplicity, bi-directionality, large current capacity, and wide control bandwidth. However, the latest simple solution can be used alone only in low voltage BE applications (i.e., below 48 V) or in applications where the isolation is performed at the mains connection with a line frequency bulky transformer. On the other hand, the use of the DAB converter enables the insertion of the high frequency transformer between the first and second bridge and gives an important dimensional advantage with respect to grid-level isolation solutions. Indeed, the input of the DAB can be connected to the mains by means of a bidirectional non-isolated rectifier (typically an active front end rectifier). As will be described in the following, the tough specifications of the proposed design required the exploitation of the benefits of both the topological solutions.

The converter architecture, topology and technologies were selected to meet the demanding requirements of Table 1, while minimizing complexity. The solution of a single stage DC/DC converter was discarded due to the wide output voltage range (to emulate both high-voltage and low-voltage buses of HEV/EV) and the necessity for a high equivalent switching frequency to fulfil demanding dynamic specifications. Thus, the selected converter architecture is based on a two-stage approach, as summarized in Figure 1. In the operative installation of the converter, the V_{in} = 750 V input voltage is provided by the commercial 500 kW AFE200-72000 Active Front End (AFE) by Gefrem [21] connected to the three phase mains. As will be described in the following, the two-stage approach enables the possibility of operating the two cascaded converters in their optimal operating conditions, while delivering the high frequency galvanic isolation and precise current/voltage output values required by the application.

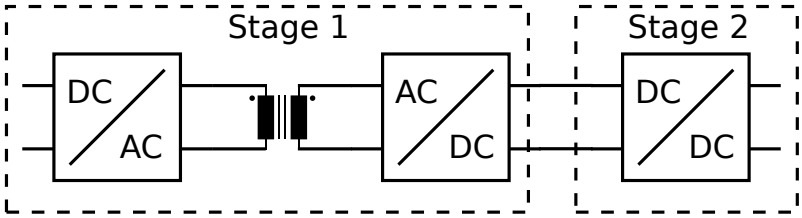


Figure 1. Two-stage topology.

For the first stage, a Dual Active Bridge (DAB) isolated converter was chosen: this topology assures bidirectionality and a fairly wide output voltages range and ZVS region, along with simplicity in the control [13,15]. The second stage is realized by means of a multi-way synchronous Buck converter with interleaved control, which allows improved control bandwidth [22,23] and a fine regulation of the output characteristics due to a higher equivalent switching frequency of the interleaved regime. Alongside boosting the control bandwidth, the interleaved-induced equivalent-frequency step-up enables magnetic and capacitors form-factors reduction in the filter, without increasing semiconductor switching losses, thus permitting a higher volumetric power density of the system. Multiple double-stage topologies are possible: the final selection depends on several considerations, involving various aspects such as transistor maximum blocking voltage (V_{BR}), transformer manufacturing, current management, control strategies and others. One important driving factor for the topology/technology selection in this application is the requirement of a maximum output voltage of 1000 V; that specification has implications in the selection of the technology (650 V, 900 V, 1200 V and 1700 V technologies are the possible candidates) and requires the consideration of topologies characterized by device stacking to sustain the voltage. Moreover, the 800 A current requirement practically rules out the use of discrete switches and is a clear indication of the necessity to exploit power modules. In Figure 2, four possible solutions that have been considered in the preliminary design phase are depicted.

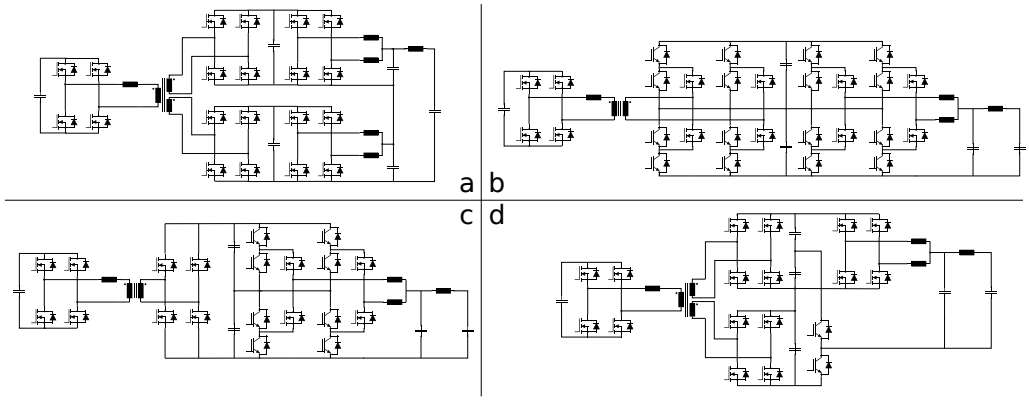


Figure 2. Four possible topologies for the implementation of the battery emulator power converter.

In Figure 2a, the first stage is implemented by a DAB converter with double secondary while the second stage is made of two synchronous Buck interleaved converters series-connected with an additional output filter. In this way, each transistor in the system shares the same V_{BR}. In Figure 2b, the DAB secondary is realized through a multilevel approach, which is also exploited in the cascaded Buck converter. In this solution, a double-secondary transformer is avoided. The multilevel structure allows the exploitation of lower voltage technology in the secondary side of the converter. In Figure 2c, the DAB secondary is simplified compared to Figure 2b thanks to the exploitation of devices capable of withstanding higher V_{BR}, while in Figure 2d the series connection is directly at the end of DAB converter since the Buck converter is a three-level interleaved single stage. Summarizing, all the illustrated alternatives, except for the first, make use of multilevel solutions; however, their additional complexity in terms of controls, the limited availability of suitable multilevel modules and the relatively few advantages assured by them suggested the use of a simpler two-level approach. Moreover, the need for a high switching frequency to minimize dimensions and optimize the instrument dynamic response practically ruled out the possibility of selecting 1700 V technology. For these reasons, topology Figure 2a was adopted. With this topology (which is shown in more detail in Figure 3), the isolation of the two secondaries of the transformer enables the series connection of the secondary-side converters. In this way, the overall 1000 V maximum output voltage is equally divided between the series-connected legs of the secondary-side converters, halving the voltage stress on the power switches and enabling the exploitation of 900 V or 1200 V technologies.

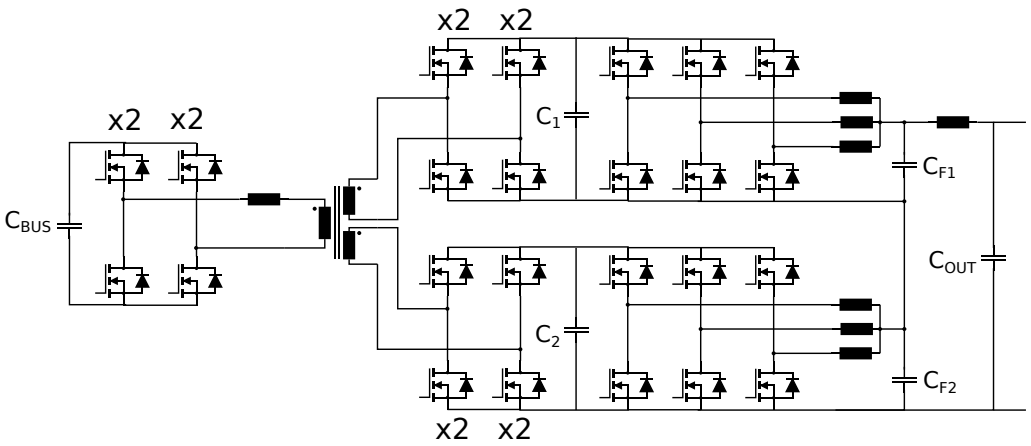


Figure 3. Selected topology for the implementation of the BE power converter.

In order to obtain a cost-effective system with an attractive market value in the automotive testing industry, it is important to take into consideration the overall system efficiency and volume. Typically, the bulkiest components in a power converter are the

magnetics and the DC-link capacitors; in addition, large magnetic components typically degrade the power dissipation budget. By increasing the switching frequency, the overall power density of the converter rises up, the dimensions of magnetics and capacitors are reduced and the control algorithm is able to meet higher dynamic requirements. Frequency up-scaling is possible by replacing traditional IGBT power devices with Wide-Bandgap (WBG) transistors such as Silicon Carbide (SiC) or Gallium Nitride (GaN) switches. Their lower gate charge and reduced parasitic capacitances enable faster commutations, allowing switching at tens of kHz instead of few kHz units [24] for the power ratings needed for this application. This is achieved without penalties in terms of conduction losses, since $R_{DS,ON}$/mm is also lower than for Si devices [24]. Thus, coming back to the selected topology, considering the very high power rating required, 900 V or 1200 V power modules rather than discrete transistors must be addressed. Since there are no commercially available GaN modules at these voltage ratings, the choice went to SiC modules, which are products that have already gained a good standing in the market and can assure the required characteristics of availability and reliability needed for the development of a commercial product. The selected power module is Wolfspeed CAB425M12XM3 [25]; it is a 1200 V, 2.6 mΩ half-bridge module capable of delivering 450 A of continuous drain current at 25 °C backside temperature. Since the module is also rated to operate with more that $400 A_{RMS}$ current switching at 50 kHz, due to its very limited E_{ON}/E_{OFF} losses [25], this frequency has been preliminary selected for the design and then confirmed with the simulations computing the associated switches losses, as described in the following. It is worth noticing that a 1200 V technology was selected since we cannot find in the market 900 V SiC modules with similar performance to the selected Wolfspeed CAB425M12XM3 when operating at 50 kHz and $400 A_{RMS}$.

Four relevant examples of the implementation of state-of-the-art DAB converters with similar power ratings (100–500 kW) and voltage levels (i.e., 400–800 V) are available in the literature [26–29]. It is interesting to notice, for all the published DAB converters at this power ratings with state-of-the-art performance, the selected technology in SiC FET modules. The designs of [26,28] are 100 kW converters at 20 kHz and 16 kHz switching frequency, respectively; the converter in [27] delivers 200 kW at 50 kHz, whereas the one in [29] is a 500 kW DAB converter at 20 kHz. In the design described in this paper, high power (350 kW) and high switching frequency (50 KHz) are combined in the same product. The measured peak efficiency in [26–29] is around 98%: this efficiency can represent a maximum target for the system described in this paper.

Referring to Figure 3 of the proposed convert, in first stage the DAB converter ([30–32]) regulates the power exchange of the system and sets the input voltage of the second-stage synchronous interleaved Buck converter. In the DAB converter topology, the H bridges at the primary and secondary sides of the transformer operate at a 50% fixed duty cycle and at the same fixed frequency. The power flow is bidirectional, and is controlled with the phase shift between the primary and the secondary square voltage wave-forms.

The Single Phase Shift (SPS) control law is used among the possible controlling strategies of the DAB converter [30]. SPS law is described in Equation (1), where n, V_1, V_2, f_s, L and ϕ are, respectively, the transformer primary to secondary turn ratio, the input voltage, the DAB output voltage, the switching frequency, the transformer leakage inductance and the phase-shift between gate signals of primary and secondary bridges.

$$P = \frac{nV_1V_2}{2\pi^2 f_s L}\phi(\pi - |\phi|) \tag{1}$$

More complex controlling strategies for the DAB had been considered and discarded to avoid further complexity in addition to the double-secondary configuration, which already imposes an extra task to the control algorithm to maintain the voltage balancing of the secondaries. Nonetheless, precise control of the power regulation is provided by the high resolution control of the phase shift enabled by the micro-controller. In particular, the high resolution PWM step of 150 ps of the microcontroller enables a power flow control

discretization of 30 W, which facilitates the required high resolution control of the output voltage and current implemented by the second stage.

Equation (1) [30] refers to the primary side, and therefore V_2 is the sum of the output voltages of the two secondaries. The turn ratio n is selected such that the voltage transfer ratio $d = (n \cdot V_2)/V_1$ is in unity with the nominal input voltage $V_1 = 750$ V and nominal maximum output voltage $V_2 = 1000$ V. This, indeed, guarantees that, for the proper selection of the leakage inductance, both primary and secondary H bridges experience soft switching (ZVS) commutation for a broad range of output power [31]. Therefore, $n = 6/8$ in Equation (1), where physically the two secondaries will have half of the secondary turn due to the output series connection. Choosing $\phi = 45°$ for nominal conditions of maximum output power, i.e., $P_{out} = 350$ kW, $V_1 = nV_2$, and $f_s = 50$ kHz, L is approximately 3 uH, providing a good setup to obtain a wide output voltage range as described in Figure 4, where Equation (1) is graphically analyzed for a series of noticeable operating regimes.

Here, the choice $\phi = 45°$ has been as a trade off between controllability and circulating current levels ([31]); moreover, a lower value of ϕ would result in an L value that could be lower than the typical leakage inductance of the planar transformer.

The y-axis Figure 4 represents the sum of secondary voltages (V_2), while the x-axis is the "equivalent" input mean current at the primary side of the DAB (i.e., output power divided by input voltage, neglecting efficiency). The area limited by the green power-constant curve at 350 kW and the V_{min}, V_{max} lines represents the V_2 range for which every $P_{out} \leq P_{out,max}$, while the converter operative region also extends below V_{min}, accounting for a power de-rating. V_{min} is selected to limit the device peak and RMS currents for $P_{out} = 350$ kW at a level compatible with the module maximum ratings, whereas V_{max} is selected to be 1150 V to guarantee a large soft switching region (the higher V_2 is, the smaller the soft-switching region for fixed power). On the other hand, $V_2 = 1150$ V = $V_{out,max}/0.87$ enables the limiting of the duty cycle of the buck converter at 87% when delivering $V_{out} = V_{out,max} = 1000$ V.

Four example points are highlighted (A to D) in Figure 4. A to C are 350 kW full-power operating points with different combinations of voltage and current, whereas at D the DAB converter delivers roughly one half of the full power (180 kW at 200 V). Point B represents the maximum stress in terms of RMS currents for the switches and for the DAB transformer. The vertical lines represent different current levels set for for different phase-shift values. The dead-time limit curve represents the minimum phase shift between the bridges below which the dead-time effects, such as phase shift drifting and voltage polarity reversal phenomenon, become significant [33], making Equation (1) not strictly valid anymore. In this design, the selected dead time is 300 ns, corresponding to a minimum phase shift of 5.4° for the dead-time limit. The 54.3 kW curve in Figure 4 represents the edge between the normal working mode in SPS and the area where the converter characteristics are affected by the dead-time. Finally, the 38.4 kW constant power curve is covered when 48 V and 800 A are required at the output of the BE. For the selection of the switches (i.e., power module number) and the design of the transformer and magnetics, it is necessary to determine the maximum peaks of the currents and their RMS values. It is well known that, in the DAB converter, the RMS and peak current stress of the devices are quite high and are affected by the choice of the leakage inductance in series with the transformer. With SPS, the current flowing at the primary through the leakage inductance has a trapezoidal shape, where the corner values at the end of phase-shift time and at half of the period can be calculated as follows [34]:

$$i_L(\pi) = \frac{V_1\pi + nV_2(2\phi - \pi)}{4\pi f_s L} \tag{2}$$

$$i_L(\phi) = \frac{nV_2\pi + V_1(2\phi - \pi)}{4\pi f_s L}. \tag{3}$$

Specifically, when the DAB converter works in Buck-mode ($V_1 > nV_2$) Equation (2) represents the current peak, while in Boost-mode ($V_1 < nV_2$) Equation (3) becomes the new current peak. Considering case B of Figure 4, the primary current peak value calculated is 861 A. In addition, Equations (2) and (3) are useful to evaluate the soft-switching region. Indeed, the series inductance at the primary and secondary of the transformer acts as a lagging current generator that can discharge the C_{oss} of the devices of the power modules during dead-time, obtaining Zero-Voltage Switching (ZVS). This is practically verified when $i_L(\pi)$ and $i_L(\phi)$ are positive [32], indicating that the converter tends to exit the soft switching region as the phase shift decreases, and then for lower output power. From Equations (2) and (3) it is possible to plot the soft switching region of the converter in Figure 5. The ZVS region is limited by the two boundaries curves: the input bridge operates in ZVS for all the points below the "input bridge boundary curve" (blue curve), whereas the output bridges operate in ZVS for all the points above the "output bridge boundary curve" (red curve). Thus, the shaded region in the plot represents working conditions where both input and output bridges operate in ZVS. It is important to notice that the nominal condition $V_{in} = nV_{out}$ is entirely included, indicating that not only does the converter operate in ZVS at full power, but also a control strategy that aims at forcing this nominal voltage ratio is capable of extending the ZVS region down to very low output power levels. Since the input H bridge boundary is directly linked to boost-mode operations, and the PS value of the intersection with $P_{out} = 350$ kW line is lower than the value needed for maximum power at $V_2 = 1150$ V, point C of Figure 4 is also in the ZVS region.

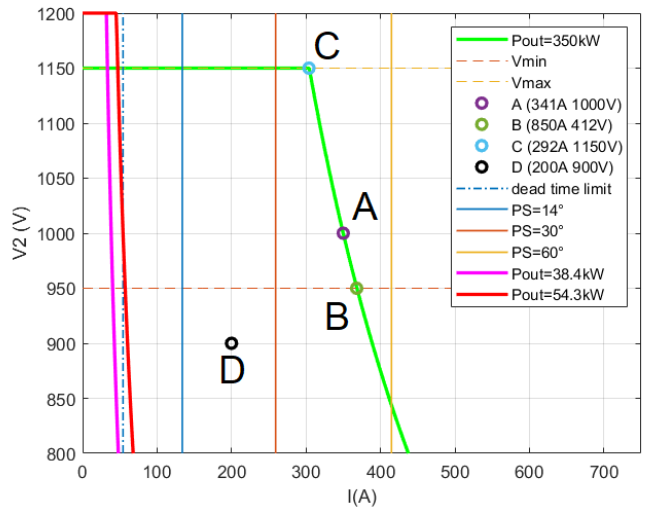


Figure 4. DAB relevant operating points.

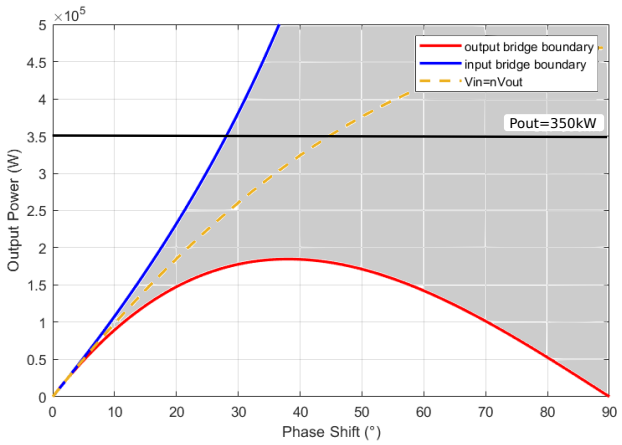


Figure 5. DAB ZVS region.

The maximum RMS current values have been preliminary evaluated by means of simulations of the converter working in the critical point B of Figure 4. For these preliminary simulations that had the goal to identify the target current ratings, almost ideal device models were adopted in the PSIM simulation environment [11]. More detailed simulations for an accurate assessment of the converter performance are describe in the following. The simulated primary currents are shown in Figure 6, along with the primary and secondary voltages. The peak value of the current is in accordance with Equation (2), whereas the RMS value is $I_{prim,RMS} = 625A_{RMS}$.

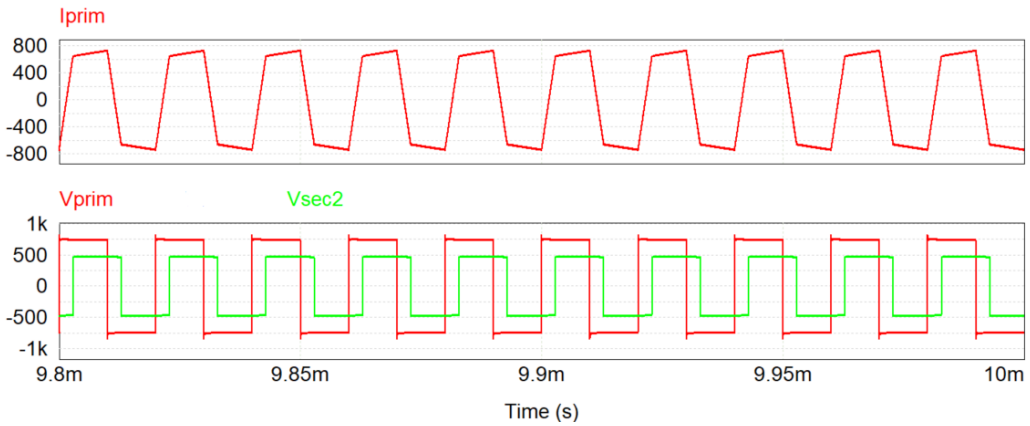


Figure 6. Primary current (Iprim in red in the upper graph) and primary (Vprim in red in the lower graph) and secondary (Vsec2 in green in the lower graph) voltages for working point B.

Since, at 25 °C backside temperature, the maximum rating of pulsed current of the CAB425M12XM3 module is 900 A and the maximum RMS current abut $450A_{RMS}$, each leg of every H bridge of the DAB converter is made of two power modules in parallel connection, also allowing a good margin in terms of reliability and a safety margin for uneven current distribution between parallel modules. The modules are mounted on cold plates that are designed to maintain the module base at 25 °C. Due to the transformer turn ratio n = 6:8 (6:4:4), the current at the secondary side is 3/4 of the primary current, thus the described sizing of two modules in parallel is even more conservative for the secondary-side H bridges.

For the Buck section, considering a maximum output current of 800 A, the mean current flowing into each leg is 267 A (neglecting the ripple) thanks to the three interleaved phases. Since the maximum DC drain current of CAB425M12XM3 is 450 A (at T_C = 25 °C), a single module for each leg of the Buck converter is adequate with a good margin (also considering a typical 10–15% additional current ripple), since the module backside is effectively cooled at 25 °C by cold-plates, as in the case of the modules in the DAB converter. It is also fair to notice that, during very fast load transient (i.e., from 0 W to 350 kW in 1 ms), the dynamic current requirement for the Buck converter to obtain a fast change in the output voltage can be much higher. With the designed set-up, the Buck converter allows the delivery of 2400 A of output current for 1 ms, due to the 900 A maximum pulsed current rating of each module combined with the transient thermal impedance characteristic of the module. The switching frequency of the Buck interleaved is set to 60 kHz in order to avoid a synchronous switching sequence with the DAB converter and consequent additional noise in sensing circuitry. Due to the three-phase interleaved operation, the equivalent output switching frequency is 180 kHz which enables large controlling bandwidth and eases the output filtering. This is also possible in terms of switching losses, since the maximum RMS current levels managed by the modules of the Buck converter are lower with respect to the ones in the DAB. For the accurate assessment of component selection, thermal management and of the converter performance, a detailed simulation setup was implemented in PSIM. The high operating frequency and the large values of currents and voltages and their derivatives di/dt and dv/dt require a detailed modeling of each

component for an accurate simulation of the converter. The SiC modules are modeled using the PSIM Thermal Module [11] modeling tool. These models allow the evaluation of both the conduction and switching losses of the power modules, exploiting a look-up-table approach, thus avoiding long waveform integration during the switching event as in Spice-like simulators. This approach is especially useful when complex systems with several semiconductors need to be simulated, as in this case: a spice-like simulation to assess switching losses would be practically unfeasible, because of computing resources requirements and unpractical long simulation times. The key parameters of the power modules, such as the V_{DS}/I_{DS} chart, E_{ON}/E_{OFF} values, thermal RC network and others provided in the component data-sheet, are inserted into the database of the model and used by the simulation engine according to the boundary conditions (i.e., switched voltage, switched current, module backside temperature). As discussed before, the operating point B of Figure 4 was tested since it is the worst case scenario (maximum input current, maximum output power). The sum of the secondary voltages of the DAB is 850 V, while V_{out} and I_{out} at the BE output are 500 V and 700 A. The simulation results are presented in Table 2.

Table 2. System assessed in working point B using thermal modules of CAB425M12XM3 in PSIM.

I_{RMS} *prim*	I_{peak} *prim*	T_j *prim*	T_j *sec*	P_{diss} *prim*	P_{diss} *sec*
$624A_{RMS}$	710 A	121 °C	99 °C	3.91 kW	3.01 kW
I_{RMS} *sec*	I_{peak} *sec*	P_{diss} *buck*	T_j *buck*	efficiency [1]	
$470A_{RMS}$	574 A	1.45 kW	88 °C	96.5%	

[1] Magnetics and capacitor losses not considered.

I_{RMS} *prim*, I_{peak} *prim*, T_j *prim*, P_{diss} *prim* and P_{diss} *sec* are, respectively, the *RMS* and peak values of current at the transformer primary, the junction temperature of the devices in the primary full-bridge and the total power dissipation (conduction and switching) of the primary and one secondary H-bridge, while P_{diss} *buck*, T_j *buck* and efficiency are the dissipated power of the Buck interleaved, the junction temperature of a single device in the Buck and the total system efficiency. The values of the RMS and peak current at the primary and secondary are in accordance with the initial predictions, and confirm the correct sizing of the H bridges. They are also used as specifications for the transformer. The junction temperature of the switches in the worst case condition is largely within the 175 °C limit. The relative high switching frequency (i.e., high for this voltage/current levels) enabled by the SiC technology allows for the design of a compact planar transformer. The transformer was designed under the specification provided in Table 3. Moreover, the transformer is designed to sustain RMS currents as high as 1300 Arms for 1 ms to allow fast dynamic control of sudden changes in the load. Planar transformers [35] provide very good thermal characteristics and high power density thanks to their lower profile and a more extended flat surface of the core than conventional wire-wound ones. This allows better thermal management and assembly. In addition, the process of PCB winding realization can be easily automated, obtaining strong repeatability, accuracy and characterization of parasitics. Additionally, in terms of efficiency, the planar configuration is attractive for the simpleness of interleaving the PCB windings to reduce eddy currents and proximity effect. Due to the very large power rating, the transformer was realized by 2 × 175 kW transformers with connected primaries. The predicted efficiency at full power (i.e., 350 kW) is about 99.5%. The 1.5 kW of dissipated power is managed by a cold plate at 25 °C coolant temperature. The transformer is very compact, (373 × 375 × 75 mm) and weighs 35 kg. The measured leakage inductance at the primary side is 0.8 uH; hence, an additional external power inductor was designed to obtained the target 3 uH series inductance for the proper operation of the DAB converter. The power inductor has an inductance of 2.2 uH, dimension of 105 × 146 × 198 mm and weighs 12 kg. The estimated losses of 240 W can be practically neglected in nominal full power conditions. Litz wire windings and a ferrite

core were used for the high operation frequency. To obtain a stable inductance value for a wide range of current values, the implemented air-gap extends the saturation current to 1600 A, assuring a stable inductance in a wide range of current values. In Figure 7, the picture of the transformer and of the series inductor are shown.

Table 3. Planar transformer specifications.

Pout	Freq.	Magn. Ind.	Turn Ratio	In/Out Current (RMS)	In/Out Voltage	Dimensions
2 × 175 kW	50 kHz	410 uH	6:4:4	630–560 A	800 V 200–1400 V	373 × 375 × 75 mm

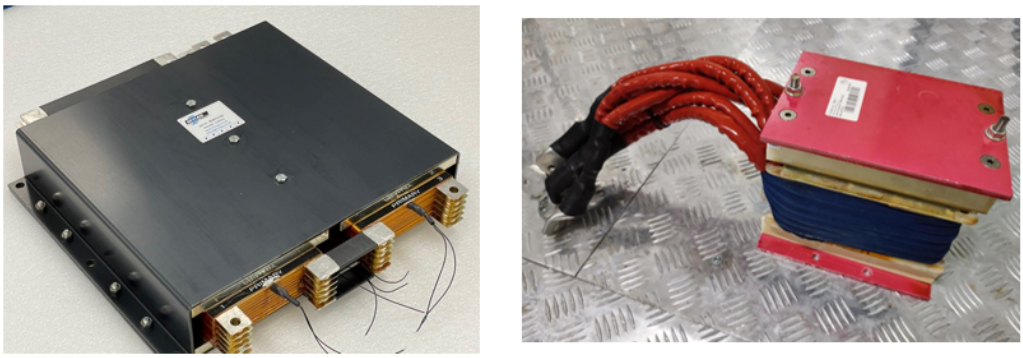


Figure 7. Picture of the planar transformer (**left**) and of the ferrite series inductor (**right**).

As described in Figure 3, additional inductors are used in the two-stage low pass filter at the converter output. The inductors are designed (along with capacitors) for the output current ripple and dynamic control requirements of Table 1. Requirements for L_1 and L_2 are summed up in Table 4, with particular attention to the inductance in overload conditions during fast steps of the load. L_1 is implemented with a nanocrystralline core for lower power dissipation, while L_2 has a grain-oriented core due to the low AC residual ripple (second stage of the LC filter) of the current.

Table 4. L_1 and L_2 specifications.

Inductor	Nom. Inductance	Nom. Curr.	Ripple p-p	f_{sw}	Overload Curr.	Residual Ind.
L_1	50 uH	267 A	50 A	60 kHz	800 A	25 uH
L_2	15 uH	800 A	*negligible*	180 kHz	2400 A	7.5 uH

A picture of these inductors is provided in Figure 8.

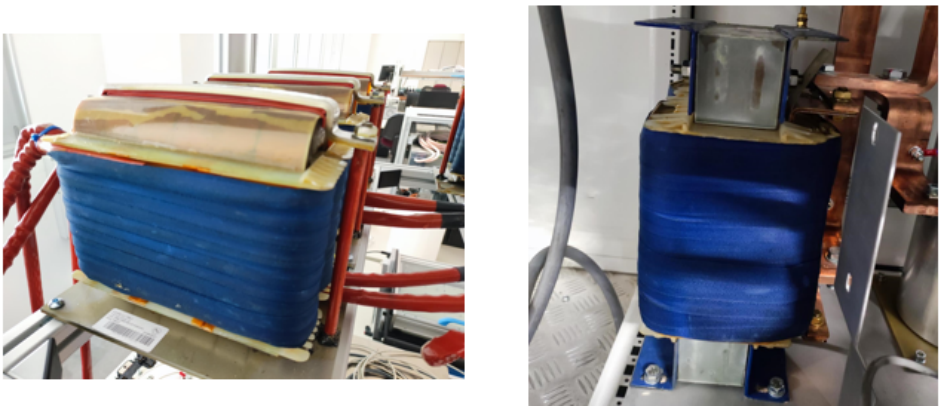


Figure 8. Buck filter inductor (**left**) and output filter inductor (**right**).

The selection and sizing of the capacitors depends on their function in the converter. Referring to Figure 3, C_{BUS} and $C_{1,2}$ are DC-link capacitors, whereas $C_{F1,F2}$ and C_{OUT} are LC-filter capacitors. DC-link capacitors need to meet several requirements simultaneously: transient energy-related, PWM-ripple-related and di/dt-related requirements. As far as regarding energy-related requirements, C_{BUS} must maintain a DC voltage close to 750 V in case of overload, while delivering the high required RMS currents without overheating. The PWM ripple generated by the DAB converter is at 100 kHz ($2 \times f_s$), whereas the low-frequency ripple from the AFE is at 300 Hz. Transient simulations performed with Simulink with a control bandwidth of 30 kHz (see next section on the control) were used to identify $C_{BUS} = 15$ mF as the minimum value necessary to maintain a DC link voltage over 680 V during the maximum power step of 1 ms. In this condition, the RMS current to be delivered by C_{BUS} is about $520A_{RMS}$ with a peak value of 1330 A. With this value of capacitance, the ripple requirements are automatically satisfied provided that low ESR/ESL capacitors are used. Considering the capacitor ESL, the most stringent requirements come from the very high di/dt required from the DC-link capacitors during SiC modules commutation. Since the estimated di/dt is $di/dt = 9$ A/ns, the maximum allowed parasitic inductance should be $L_{TOT} = 11$ nH to limit the maximum overshoot around 100 V. This value is chosen to have a large safety margin with respect to the 1200 V and 1100 V voltage rating of power module and C_{BUS}, respectively, minimize the component stress and reduce the generation of EMI which can be problematic for the control signals. The contributions to L_{TOT} are the power module inductance (3.5 nH for two modules in parallel), the ESL of the capacitors and the parasitic inductance of the bus bars connecting the SiC modules to the capacitors. Custom laminated DC bus-bars that allow magnetic field cancellation for inductance minimization have been adopted for the connection of the SiC modules to the DC-link capacitors: with this solution, implemented by a specialized bus-bar provider under our specifications, the resulting parasitic inductance of this connection is less than 2 nH; this is also in accordance with the number obtained in [36], with a similar bus-bar solution adopted for the same SiC modules. This leaves about 5.5 nH for the maximum value for the equivalent ESL of the C_{BUS}.

Considering all these constrains (along with the space requirement constrain), the adopted solution was to implement the 15 mF C_{BUS} with a combination of electrolytic and polypropylene film technologies: 12.6 mF of 550 V electrolytic capacitors (series connection) are used as the main energy bulk, whereas 2.4 mF of 1100 V film capacitors provide the required very low ESL and very high peak current [37]. For the identification of $C_{1,2}$ the considerations are similar, but in this case the requirement in terms of energy bulk for dynamic response is more relaxed due to the fast response of the DAB converter that feeds this DC link. Thus, the identified value for this component is $C_{1,2} = 1.2$ mF and it is entirely implemented in polypropylene film technology. For the capacitors $C_{F1,F2}$ and C_{OUT} in the two-stages output filter, there is no di/dt stress due to the presence of the inductors. Moreover, in steady-state, the RMS currents through the capacitors are quite small. However, in dynamic conditions large variations of output power and voltage levels produce high dynamic currents, so the ESR must be very small, high peak current capability is required and capacitance value is selected to maintain a stable voltage during transient (PWM ripple requirement is less stringent). Therefore, polypropylene film capacitors are also chosen in this section. The selected values are: $C_{F1,F2} = 1.2$ mF (900 V film capacitors providing 450 A peak); $C_{OUT} = 2.4$ mF (1400 V film capacitors providing 2000 A peak).

3. Control System

In this section, the overall control system is described along with some details on the PCB boards developed for its implementation. The sensing and command set-up that interfaces the power and control systems is shown in Figure 9. As described in the Figure 9, the system counts 15 analog sensors (current and voltage sensors), 18 CAB425M12XM3 modules with relative CGD12HBXMP driver boards by Wolfspeed and 24 PWM signals to control the power flow.

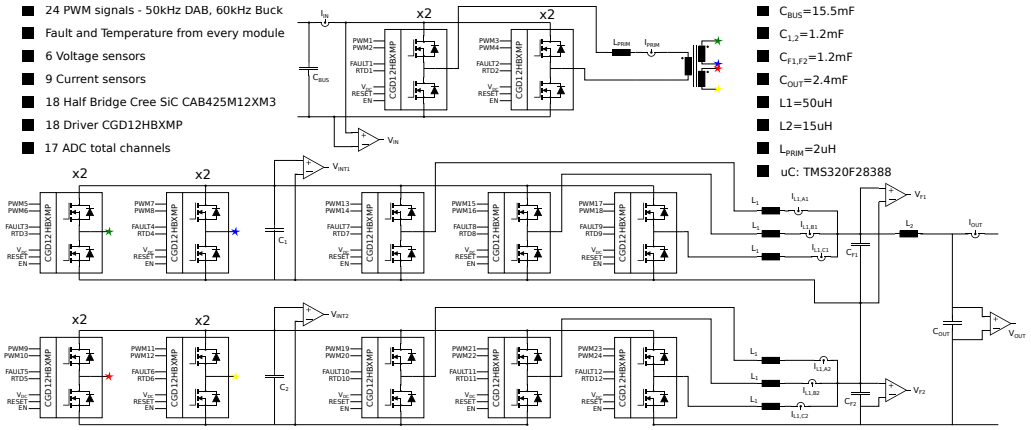


Figure 9. Sensing and commands structure.

In the implementation of the system prototype, several sensing points are used; some of them can be avoided in the final set-up. In addition to the BE output current and voltage I_{out} and V_{out}, voltages at output ports of AFE, DAB and Buck ($V_{in,DC}$, $V_{int1,DC}$, $V_{int2,DC}$, $V_{out1,DC}$ and $V_{out2,DC}$) and currents at input port, transformer primary winding and each Buck interleaved phase ($I_{in,DC}$, I_{prim}, $I_{L1,a1}$, $I_{L1,b1}$, $I_{L1,c1}$, $I_{L1,a2}$, $I_{L1,b2}$ and $I_{L1,c2}$) are sampled. At the output stage, the demanding specifications in terms of dynamics and accuracy require the adoption of top-of-the-line sensors. For the current, the ITN 900-S ULTRASTAB by LEM provides the capability to sense $\pm$900 A with a 300 kHz bandwidth and 0.0011% accuracy, whereas the CV-3 2000 voltage sensor by LEM senses the output voltage up to 1400 V with a 300 kHz bandwidth and 0.2% accuracy. I_{prim} and $I_{in,DC}$ are used for protection purposes, so the LF 1005-S by LEM ($\pm$1500 A, 1000A_{RMS}, 150 kHz bandwidth, 0.4% accuracy) is chosen, while for the current balancing among Buck interleaved phases the LF 510-S by LEM ($\pm$800 A, $\pm$500A_{RMS}, 200 kHz bandwidth, 0.5% accuracy) has been selected. All the previous transducers have closed loop compensation for performance enhancement. The remaining voltage measurements are carried out by inexpensive resistive dividers and isolated Op-Amps.

A dedicated CGD12HBXMP driver board has been chosen to drive each power module, since it provides full compatibility to XM3 Wolfspeed Half Bridge Power Modules in terms of optimal assembly, high-frequency operations and fault protection. High-side and low-side gate signals are supplied to the board in differential modes for noise immunity, and are transformed into single-ended signals before reaching the two single-channel ADuM4135 (Analog Devices) isolated gate drivers used inside the driver board. The ADuM4135 is able to furnish $\pm$10 A peak gate current for fast commutations and embeds de-saturation circuitry which, in combination with external over-voltage and shoot-though prevention circuits, generates the main output fault signal of the driver board. Moreover, the driver board acquires the temperature of the power module from a die-level NTC sensor and outputs, it applying a frequency modulation.

3.1. Control Strategy

The control strategy aims to regulate the DAB and the Buck interleaved converters shown in Figure 3 with a single voltage closed loop and a double voltage-current closed loop, respectively.

3.1.1. Buck Control

Two feedback loops are implemented for the Buck control: the external and slower one regulates the output voltage, while the internal and faster one the current of each interleaved phase, also providing current balancing.

The inputs of the voltage regulator are V_{out} (potential of C_{out}), the voltage set-point V^*_{out}, the output current I_{out}, requested from the load for the feed-forward contribution, and the output voltages V_{F1} and V_{F2} of the two Buck interleaved for balancing purposes.

The output of the controller is the reference I_1^* for the internal loop that represents the current sum of each interleaved phase contribution. For clarity's sake, the control loop is schematized in Figure 10, where the main characteristics are reported (for the complete acquired characteristics, refer to Figure 9).

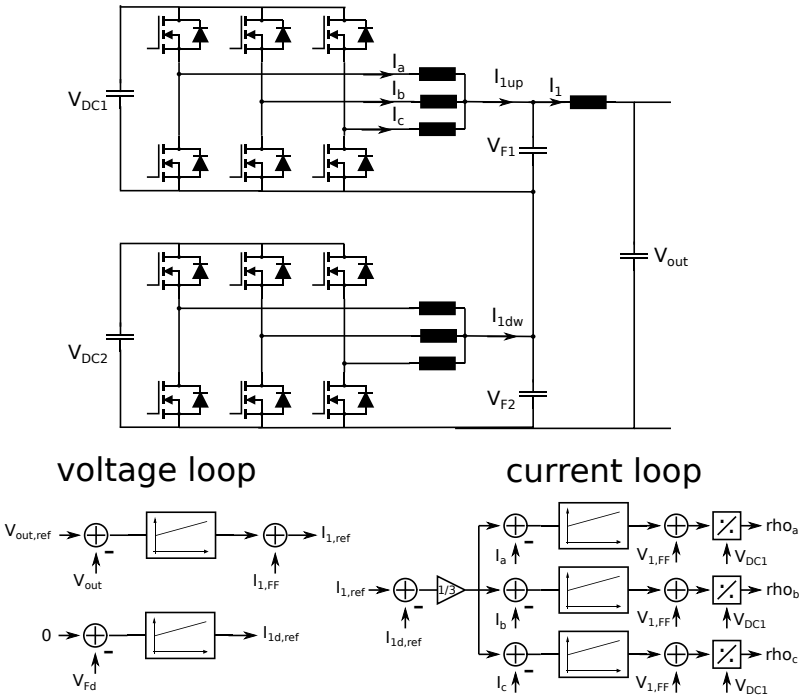


Figure 10. Control diagram of the output section. Only the current loop for the upper Buck interleaved converter is shown.

The plant consists, basically, of the cascade of the Buck filter and the output LC-filter ($C_{F1,2}$, L_1 and C_{out}, L_2, respectively), resulting in a system described by the following state equations:

$$\begin{aligned} C_{out}\frac{dv_{out}}{dt} &= i_2 - i_{out} - \frac{v_{out}}{R_{dout}} \\ L_2\frac{di_2}{dt} &= (v_{F1} + v_{F2}) - v_{out} - R_{L2}i_2 \\ C_{F1}\frac{v_{F1}}{dt} &= i_{1up} - i_2 - \frac{v_{F1}}{R_{df1}} \\ C_{F2}\frac{v_{F2}}{dt} &= i_{1dw} - i_2 - \frac{v_{F2}}{R_{df2}} \end{aligned} \tag{4}$$

where i_2 is the current in L_2, R_{dout} is the external discharge resistance in parallel to C_{out}, R_{L2} is the ESR of L_2, i_{1up} and i_{1dw} are the current sum of the two Buck interleaved, and R_{df1} and R_{df2} are discharge resistances of C_{F1} and C_{F2}. Considering

$$C_{F1} = C_{F2}; \quad v_{Fs} = v_{F1} + v_{F2}; \quad v_{Fd} = v_{F1} - v_{F2} \quad i_1 = \frac{i_{1up} + i_{1dw}}{2}$$

the following equations can be obtained:

$$\begin{aligned} C_{out}\frac{dv_{out}}{dt} &= i_2 - i_{out} - \frac{v_{out}}{R_{dout}} \\ L_2\frac{di_2}{dt} &= v_{Fs} - v_{out} - R_{L2}i_2 \\ \frac{C_{F1}}{2}\frac{v_{F1}}{dt} &= i_{11} - i_2 - \frac{v_{F1}}{2R_{df1}} \\ C_{F1}\frac{v_{Fd}}{dt} &= i_{1d} - i_2 - \frac{v_{Fd}}{R_{df2}} \end{aligned} \tag{5}$$

From the first three equations of Equation (5), the transfer functions (t.f.) $G_{v1} = \frac{i_{out}}{v_{out}}$ and $G_{v2} = \frac{i_1}{v_{out}}$ are computed and shown in Figure 11, where G_{v2} is the one used for the control. The control bandwidth must be above 1 krad/s to have a time constant less than 1 ms, and distant from the resonance peak at 19 krad/s (3 kHz). In any case, the feed-forward terms and additional resistive losses help against the resonant peak. The feed-forward term i_{1ff} can be calculated as

$$\begin{aligned} i_{2ff} &= i_{out} + \frac{v_{out}}{R_{dout}} + C_{out}\frac{dv^*_{out}}{dt} \\ v_{Fsff} &= v^*_{out} + L_2\frac{di_{2ff}}{dt} + R_{L2}i_{2ff} \\ i_{1ff} &= i_{2ff} + \frac{C_{F1}}{2}\frac{v_{Fsff}}{dt} + \frac{v_{fs}}{2R_{df1}} \approx i_{out} + (C_{out} + \frac{C_{F1}}{2})\frac{dv^*_{out}}{dt}. \end{aligned} \tag{6}$$

Hence the current reference i^*_1 for the current loop can be computed

$$i^*_1 = i_{1ff} + PI(v^*_{out} - v_{out}) \tag{7}$$

where the Proportional-Integral (PI) regulator bandwidth is sufficiently slow to exclude the resonant peak.

Considering the last equation of Equation (5), the current balancing among the two Buck interleaved is implemented by

$$i^*_{1d} = PI(0 - v_{Fd}) \tag{8}$$

and used for the reference values of the current loop:

$$\begin{aligned} i^*_{1up} &= i^*_1 + \frac{i^*_{1d}}{2} \\ i^*_{1dw} &= i^*_1 - \frac{i^*_{1d}}{2} \end{aligned} \tag{9}$$

For the current internal loop, only the upper Buck interleaved is treated since it is identical to the other. The plant is described as follows:

$$\begin{aligned} L1\frac{di_{1up,a}}{dt} &= v_{up,a} - v_{F1} - R_{L1}i_{up,a} \\ L1\frac{di_{1up,b}}{dt} &= v_{up,b} - v_{F1} - R_{L1}i_{up,b} \\ L1\frac{di_{1up,c}}{dt} &= v_{up,c} - v_{F1} - R_{L1}i_{up,c} \end{aligned} \tag{10}$$

where the a, b and c letters indicate the three interleaved phases. Each phase current is sensed and employed for the error calculation in combination with the $i^*_{1up}/3$ set-point, and

provided to a *PI* regulator to obtain the voltage reference for duty calculation. Additionally, in this case a feed-forward term is used:

$$v_{up,a,b,c} = v_{up1ff,a,b,c} + PI\left(\frac{i^*_{1up}}{3} - i_{1up,a,b,c}\right) \quad v_{up1ff,a,b,c} = v_{F1} + L_1\frac{di^*_{1up}}{dt} \tag{11}$$

The bandwidth of the *PI* current regulator is set to be ten times that of the *PI* voltage regulator in order to be able to have noise rejection with a PWM frequency of 60 kHz and a control frequency of 30 kHz. Nevertheless, it is important to have synchronous current sampling with the PWM signal to regulate the mean value of the phase current and acquire the middle of ON time for low switching noise . The very fast ADC operating at 200 MHz provided with the selected TMS320F28388D microcontroller largely facilitated this task. Once $v_{up,a,b,c}$ are calculated, the modulation indices are retrieved:

$$\rho_{a,b,c} = V_{DC1}/v_{up,a,b,c}$$

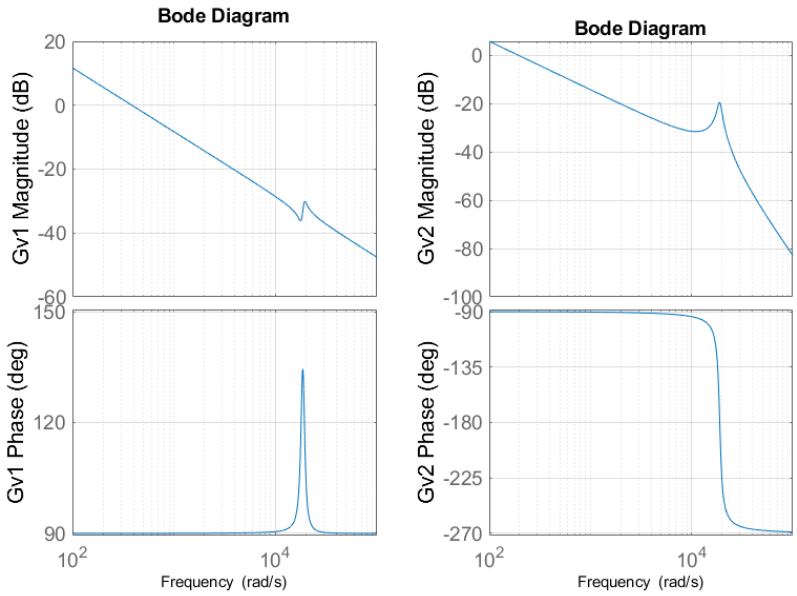


Figure 11. Bode plots of G_{v1} (**left**) and G_{v2} (**right**).

3.1.2. DAB Control

The role of the DAB converter is to maintain a stable voltage at the input of the Buck converter, also providing a fast dynamic variation of power transfer according to the load requests. For this purpose, the V_{C1} and V_{C2} voltages of the C_1, C_2 capacitor between the DAB and the Buck converter are sensed and the correspondent phase-shift to be applied to the gate signals is obtained. Since the power transfer is determined by the voltage across the series inductor at the transformer input (i.e., leakage inductance + additional series inductance), it is important that the square voltages of the two transformer secondaries must be as equal as possible in terms of amplitude and delay. Therefore, two separate phase-shift terms, ϕ_{up} and ϕ_{dw}, are used. In Figure 12, the control diagram is depicted along with the scheme indicating where V_{C1} and V_{C2} are located.

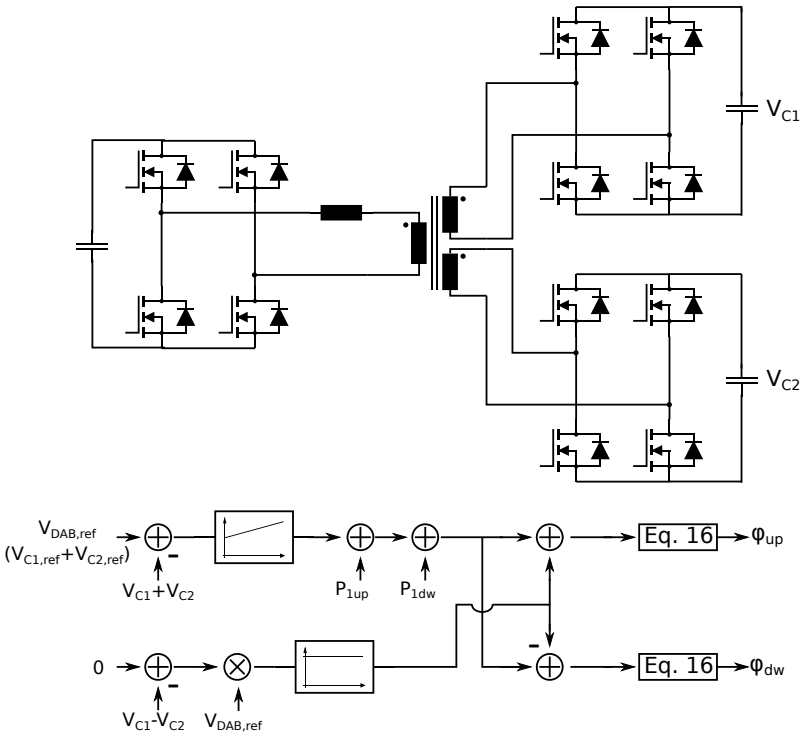


Figure 12. Control diagram of the DAB converter.

Considering the V^*_{C1} and V^*_{C2} reference nominal values for v_{C1} and v_{C2}, we can write:

$$\begin{aligned} C_1 \frac{dv_{C1}}{dt} &\approx \frac{p_{outDAB,up} - p_{1up}}{V^*_{C1}} - \frac{v_{C1}}{R_{dC1}} \\ C_2 \frac{dv_{C2}}{dt} &\approx \frac{p_{outDAB,dw} - p_{1dw}}{V^*_{C2}} - \frac{v_{C2}}{R_{dC2}} \end{aligned} \tag{12}$$

where p_{1up} and p_{1dw} are the power levels requested by the load from the upper and lower branches, while $R_{dC1,2}$ represent the discharge resistances of C_1 and C_2. Imposing the following constraints:

$$v_{C1} + v_{C2} = v_{outDAB}; \quad v_{C1} - v_{C2} = v_{dDAB}; \quad C_2 = C_1; \quad R_{dC2} = R_{dC1};$$

$$V^*_{C2} = V^*_{C1}; \quad p_{DAB} = p_{outDAB,up} + p_{outDAB,dw}; \quad p_{dDAB} = p_{outDAB,up} - p_{outDAB,dw}$$

the following equations can be obtained:

$$C_1 \frac{dv_{outDAB}}{dt} = \frac{p_{DAB} - (p_{1up} + p_{1dw})}{V^*_{C1}} - \frac{v_{outDAB}}{R_{dC1}} \tag{13}$$

$$C_1 \frac{dv_{outDAB}}{dt} = \frac{p_{DAB} - (p_{1up} - p_{1dw})}{V^*_{C1}} - \frac{v_{dDAB}}{R_{dC1}} \tag{14}$$

From Equation (13), the control for the power flow demanded from the DAB converter is computed by a *PI* regulator on voltage error and feed-forward contributions.

$$p_{DAB} = p_{1up} + p_{1dw} + PI(2V^*_{C1} - v_{outDAB}) \tag{15}$$

Once the power is computed, the phase-shift is calculated (from Equation (1)) as

$$\phi = \pm \frac{\pi}{2} \left(1 - \sqrt{1 - \frac{8 f_s L}{V_1 n (v_{C1} + v_{C2})} |p_{DAB}|} \right) \tag{16}$$

To keep v_{C1} and v_{C2} balanced, a proportional control on the voltage difference is sufficient:

$$\phi_{up} = \phi + k_{vdiff} v_{dDAB} \quad \phi_{dw} = \phi - k_{vdiff} v_{dDAB}$$

In addition, a further control is implemented to avoid transformer saturation according to the technique described in [38].

In the implemented control strategy, the reference voltages V_{C1}^* and V_{C2}^* are kept at nominal values ($\frac{1}{2}\frac{V_1}{n} = 500$ V) in order to let the DAB work in the optimal condition (ZVS, low current stress), as long as the output requires less than 1000 V or the Buck converter reaches the minimum possible duty cycle value ρ_{min}. In the first case, the DAB output voltages are increased to 600 V, while in the second the DAB output is decreased until the BE output set point is reached, with the Buck duty cycle at $\rho = \rho_{min}$. Finally a soft start procedure is implemented for converter turn-on: the gate signals of secondary side bridges are kept OFF while the phase-shift between the two diagonals of the full-bridge at primary side is ramped-up from 0 to π, i.e., the point where the H-bridge diagonals work alternatively. In this way, C_1 and C_2 are slowly charged through the body diodes of the devices of secondary side bridges until the nominal voltage is reached. Once the target voltage is sensed, the control turns ON all the gate signals of DAB and Buck interleaved converters.

3.1.3. Software Architecture

The final user of the system can check the DC/DC converter status and set voltage/current reference value by means of an external master system that communicates with the control board by EtherCat protocol, as in Figure 13.

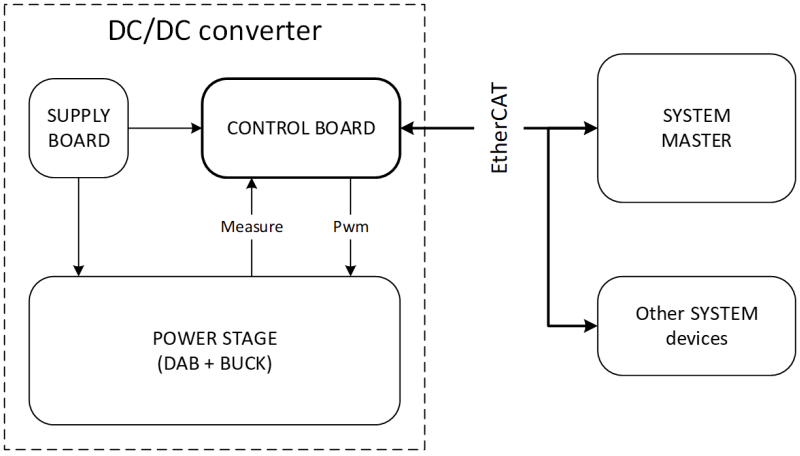


Figure 13. Schematic of external communication with the DC/DC control.

Currently, the Master interface application is under development and therefore the control board is accessed with accessory peripherals such as CAN and RS485. In this way, the microcontroller is flashed and the task's time constraints are verified. For communication purposes, the Cortex M4 within the microcontroller is used, while the two C2000 cores are dedicated to DAB and Buck control, respectively. It has been verified that the tasks in charge of the computation for control algorithms, the most critical ones, fit the control period, and therefore the CLA resource is not exploited. In particular, only 18% and 40% of the process time is used in core 1 (DAB) and core 2 (Buck), respectively. This confirms the good choice of the Texas Instruments F28388D microcontroller.

3.2. Simulations of the Battery Emulator

The described simulation strategy has been implemented in Simulink, and the PSIM–Simulink co-simulation feature (i.e., PSIM SimCoupler) was exploited for a detailed simula-

tion of the entire system, including the control dynamics. Figure 14 shows some details of the PSIM and Simulink schematics.

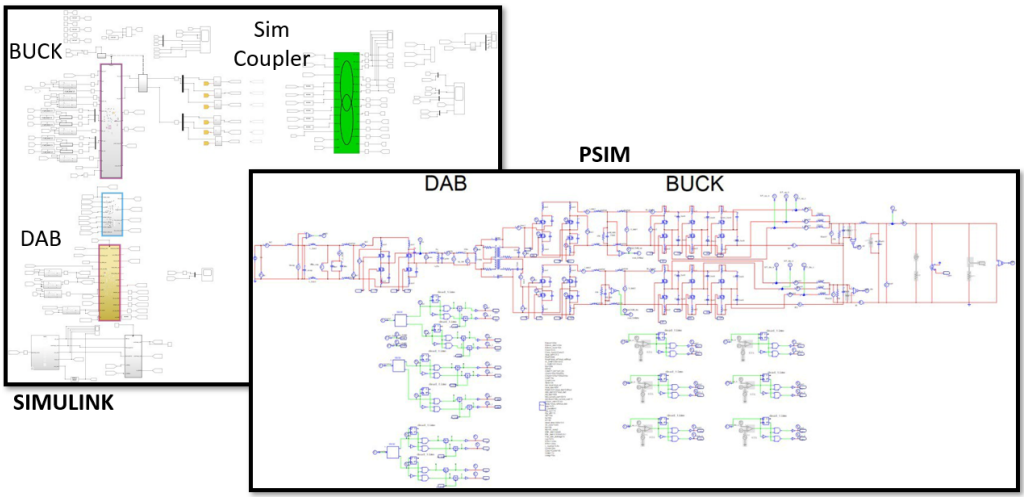


Figure 14. PSIM and Simulink schematics for the system co-simulation.

The Simulink engine takes as input the sensed characteristics from the PSIM schematic, providing in return the gate signals according to the described control strategy; the power systems simulation in PSIM is controlled by these signals generated in Simulink. The PSIM simulation takes into account all the main parasitics introduced by passive components, such as ESR, ESL, bus-bar stray inductance and conduction/commutation losses of the switches.Thus, this simulation set-up is capable of an accurate evaluation of the converter performance, both in terms of steady state regime and transient response to load or command changes. The same solver settings have been arranged in Simulink and PSIM (fixed time step at 1/10 of the dead time), following the procedure described in [39]. Moreover, to reduce the simulation time, initial voltage levels of capacitors and current levels on inductors were set for every simulation, according to the different operating condition under test.

The results of the simulation of three relevant steady-state working points of the entire battery emulator, exploiting the co-simulation feature, are shown in Table 5. As described in the caption of the table, Case A is a full-power working point at the maximum output current, Case B is a full-power point at the maximum output voltage and Case C is a low-power working point corresponding to the combination of minimum voltage and maximum current.

Table 5. System performances in steady-state conditions. Case A: V_{out} = 437.5 V, I_{out} = 800 A, P_{out} = 350 kW. Case B: V_{out} = 1000 V, I_{out} = 350 A, P_{out} = 350 kW. Case C: V_{out} = 48 V, I_{out} = 800 A, P_{out} = 38.4 kW.

Case	I_{RMS} *p.*	I_{peak} *p.*	T_j *p.*	T_j *s.*	T_j *b.*	P_{diss} *p.*	P_{diss} *s.*	P_{diss} *b.*	P_{in}	P_{out}	eff.
A	590 A	709 A	122 °C	99 °C	83 °C	4.28 kW	2.51 kW	1.78 kW	361 kW	348 kW	96%
B	536 A	798 A	81 °C	110 °C	104 °C	2.39 kW	2.5 kW	0.76 kW	354 kW	348 kW	98%
C	298 A	622 A	85 °C	33 °C	70 °C	2.47 kW	0.28 kW	1.17 kW	46 kW	38 kW	83%

The data listed in Table 5 are the primary current *R* ms and peak value, the total power dissipation for the primary full-bridge (P_{diss} *p.*), one secondary full-bridge (P_{diss} *s.*) and a Buck interleaved converter, the hottest device junction temperature, the overall input and output power and the efficiency. Simulations highlight a large safety margin for the junction temperatures and elevated efficiency at full power. The efficiency decrement in Case C is due to the low reference voltage adopted for the DAB converter; indeed, to produce 48 V

at the emulator output, the Buck converter input voltage must be low (e.g., 200–300 V), since it is not possible to operate it at a very low duty cycle because of the required 800 A output current. Consequently, the DAB converter works far from the nominal condition (i.e., $V_{out,DAB} = 240$ V) . The consequence is a high peak primary current and higher power dissipation compared to the secondary side. For the evaluation of the dynamic response of the converter, three different cases are described as relevant examples. Figure 15 describes the converter response to a 0–800 A, 10 ms load step in the worst case, i.e., when the out voltage is at its minimum $V_{out} = 48$ V and DAB and Buck converters are working far from nominal condition. The response of the system is fast, with a maximum undershoot of V_{out} of 6.5 V and an almost total recovery of the nominal value after less than 2 ms. In Figure 16, the converter response to a load current of steps 0–800 A is described in terms of the output voltage variation from the nominal point $V_{out} = 437.5$ V at no load condition. The low frequency ripple is due to the null output power condition when $I_{out} = 0$ A. It can be appreciated that the maximum variation of the output voltage is about 2%.

Finally, Figure 17 shows how V_{out} follows the 1000 V–48 V reference step within 10 ms as specified.

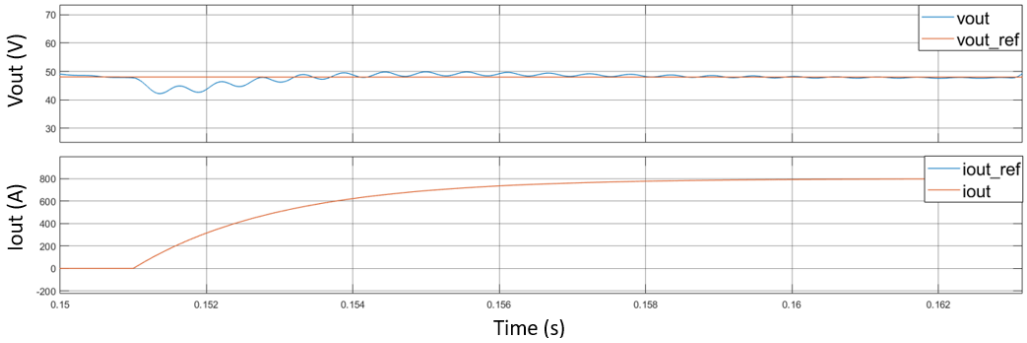


Figure 15. System response to a 0–800 A current load request with fixed $V_{out} = 48$ V.

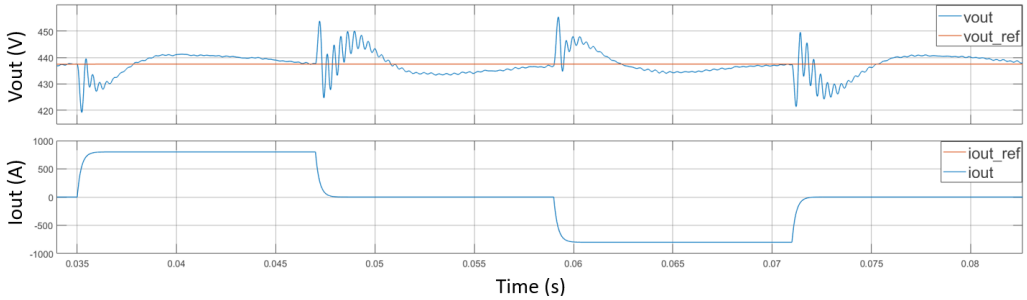


Figure 16. System response to a 0–800 A current load request with fixed $V_{out} = 437.5$ V.

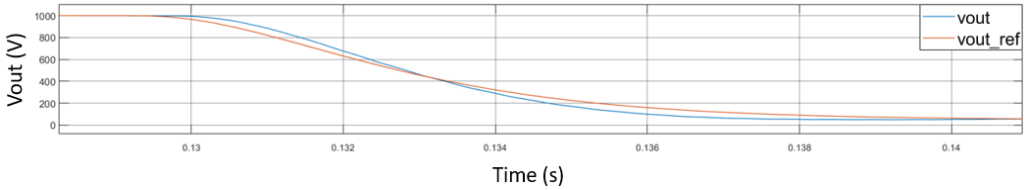


Figure 17. System response to a 1000 V–48 V output voltage step.

3.3. Hardware for the Control System

As described in Figure 9, due to the complexity of the converter, the control system must provide 24 high frequency (50–60 kHz) PWM signals, read several sensors and provide many dedicated power supplies to drivers, sensors and signal conditioning chains. The hardware dedicated to control purposes has been split into two separated PCBs, an Auxiliary Supply Board and a Control Board. In this way, the power generation for analog

circuits (including sensors) and digital circuits is confined in the Auxiliary Supply Board, avoiding additional switching noise in the Control Board where the micro-controller, the communication peripherals and signal conditioning are placed. In addition, the single-board solution would have a very large dimension with less immunity to electromagnetic interference and more complex housing into the rack.

3.3.1. Auxiliary Supply Board

From the external AFE, the Supply Board receives an already-filtered $230V_{AC}$ mono-phase voltage and a 150 W 12 V DC isolated voltage. The latter is used for the supply of CGD12HBXMP drivers and digital circuits (12 V and 5 V, referring to GND), while the second is used by sensors and analog circuits ($\pm$18 VA and +5 VA, referring to GNDA, where the suffix A stands for Analog). The scheme is presented in Figure 18. The 12 V are directly passed as output and also used to obtain 5 V through a 20 W buck converter realized with the TPS5450DDARG4 Texas Instrument IC considering a 500 kHz switching frequency and $100mV_{pp}$ output voltage ripple.

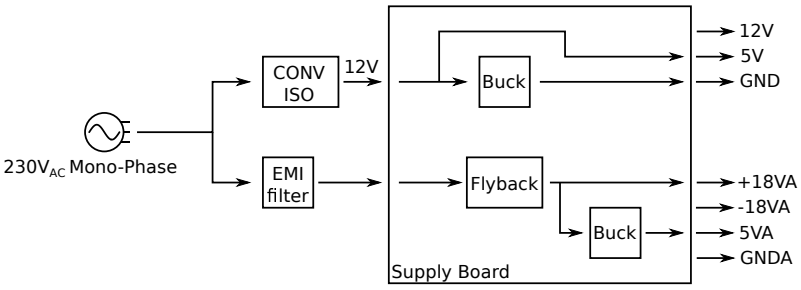


Figure 18. Supply Board scheme.

Concerning the analog section, the converter is designed considering a maximum power request of 40 W, where a large part of it is ascribed to LEM sensors (36 W). Since the LEM sensors need a stable $\pm$15 V, the Supply Board generates a switching $\pm$18 VA voltage, which is scaled down by linear converters in the Control Board. The converter topology is a Flyback with bipolar output, as shown in Figure 19, where at the input the alternate voltage is rectified by a diode bridge and filtered. The control and the main switch are integrated in the same TOP257YN IC [40] by power integration, that regulates at 132 kHz switching frequency an overall 36 V (18 V + 18 V) output voltage by an opto-isolator. The transformer is a custom design. The converter is designed to provide 80 W, not only for safety margin but also because, in the unlikely event in which each current sensed by LEM has same polarity and is at the maximum peak allowable, the current drawn from the Flyback is concentrated in just one branch of the bipolar output. The last voltage, 5 VA, is generated by the TPS5450DDARG4 integrated buck converter by Texas Instruments, like for the 5 V, starting from the +18 VA with a 15 W maximum output power.

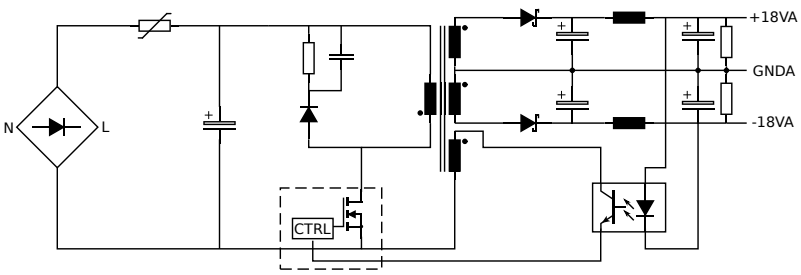


Figure 19. Bipolar Flyback scheme.

3.3.2. Control Board

The Control Board is the hardware platform in which the control algorithm is executed, taking advantage of sensors measurements and producing PWM signals, with the features of diagnostic and external communication. Its basic scheme is shown in Figure 20.

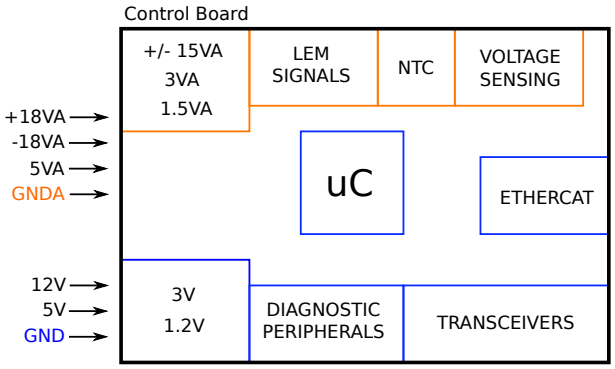


Figure 20. Control Board conceptual scheme.

The microcontroller adopted is the TMS320F28388D [41] of the C2000 family by Texas Instruments. To the best of our knowledge, it was the best real-time microcontroller available on the market for industrial application at the time of design. The elevated number of frequency-independent PWMs (32) and the 200 MHz system clock perfectly fit the requirements of complex power converter topologies that exploit WBG devices as SiC technology. The dual-core architecture, in combination with the CLA, furnishes the necessary computational resources for executing a complex control algorithm quickly, while high resolution sampling is guaranteed by 24 ADC inputs settable in 12-bit or 16-bit mode. Moreover, the TMS320F28388D embeds the EtherCAT Slave Controller, reducing the bill-of-material of the PCB. Such a protocol is used for master communication so that the user can set output conditions and check the system status.The KSZ8081MLXIA is chosen as a physical layer transceiver among the options suggested by Beckhoff [42] and set to 100 Mbit speed. Due to high-speed communication, the RX and TX lines traces are matched in terms of impedance and shielded RJ45 connectors with embedded transformers are used. Two other peripherals, RS485 and CAN, are present in the board for diagnostic purposes during test operations.

For the supply of the board, the input voltages are provided by the Auxiliary Supply Board and opportunely scaled. For the digital circuits, 5 V is used to generate 3.3 V and 1.2 V (used by uC cores) through LDO regulators.The $\pm$15 V, 3 VA and 1.5 VA voltages are obtained by LDO regulators, as well. Since the $\pm$15 V voltages are dedicated to the LEM sensors, the most power-consuming elements in the control system, and linear regulators show typically poor efficiency, three couples of 15 V, $-$15 V LDO are deployed. In particular, for balanced power-sharing, the first and second couples supply three LF510-S and LF1005-S (Buck-interleaved, input and primary currents), while the last deals with the more powerful ITN900-S ULTRASTAB and CV3-2000 current and voltage transducers. For a correct working operation, the uC also checks the status of 12 V and $\pm$18 VA voltages through two voltage dividers that generate power-good signals.

Concerning the acquisition network of current signals, the LEM sensors produce a current-mode output which has to be transformed in voltage, conditioned by an opamp and then supplied to the ADC. The current-mode signal is more immune to interference and can easily travel unchanged through the cabinet and the board up to the burden resistor. The burden resistor is placed as close as possible to the opamp in the control board to minimize voltage noise. Then, the signal must scaled and positively biased to take into account bidirectional current. For this purpose, an opamp in differential configuration with a level-shifter is used.

Regarding the voltage sensing, as said previously V_{out} is acquired by the CV3-2000 LEM sensor, while voltage dividers are exploited for the others. The voltage dividers are directly placed on the Control Board, meaning that very high voltage must be accounted for in the PCB. This choice allows better measurement resolution because a high voltage is less sensitive to switching noise when terminated to high impedance, as in this case; however, a 6 mm creepage distance is kept among potentials referring to different grounds. Of course, isolation is needed [43], so the ACPL-C87AT-500E isolated differential amplifier by Broadcom is used for the acquisition of these signals. Its isolated voltage supply is generated by a very low-power push-pull converter. Since the voltages are referred to three bus-bars , three push-pull converters are adopted and power-good signals are provided to uC for measurement consistency through opto-couplers. For V_{out}, the LEM sensor directly outputs a voltage that can be conditioned. Since this signal can be affected by noise, a back-up voltage divider is deployed in case of issues on CV3-2000 output. From a safety and normative point of view, the most critical section is the sensing of V_{in}. This voltage comes from the AFE without galvanic isolation. Hence, the Annex K of IEC 61010-1 [43] normative must be followed. In particular, the voltage category II is considered where the creepage distance is 3 mm. However, to implement double-isolation, a creepage of 6 mm is kept. For the other voltages, the situation is less critical thanks to the high-frequency transformer but the same distance is kept anyway.

The Control Board interacts with power modules by means of 18 CGD12HBXMP driver boards. The signals between the Control Board and the drivers are PWM gate control, fault, temperature, enable and reset signals. Except for the last two, the other signals are differential, so TX and RX line driver transceivers are used. In particular, transceivers with four differential inputs for TX ones in the same chip and four differential outputs for RX ones in the same chip have been chosen. This allows the management of a couple of power modules with a couple of TX/RX transceivers, simplifying the routing and minimizing the skew delay on PWM signals. The minimization of the skew is very important because of the high commutation frequency, the fast commutation of SiC devices and the short dead time adopted for efficiency maximization. The source of skew in the PWM signal has been accurately investigated, and its minimization is obtained by accurate component selections. The main components' contributions to this misalignment of time delays of different gating signals are shown in Figure 21: the TX transceiver [44] in the Control Board, the RX transceiver [45], the shoot-through protection circuit and isolated drivers in the driver board.

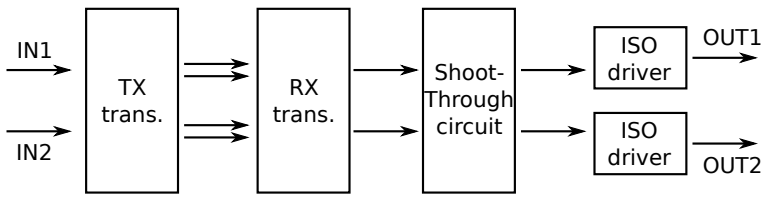


Figure 21. PWM signal path.

Summing up all the contributions, considering opposite delay terms for the signals in every chip, a maximum skew of 43 ns could be estimated. However, this is an unrealistic computation, and therefore a more realistic value of 25–30 ns can be considered. This skew can be considered acceptable given an estimation of the SiC module minimum commutation time of around 50 ns and the selected dead time of 300 ns. Regarding the frequency-modulated signals for monitoring the temperature of the SiC modules, given the slow dynamic of this characteristic, they are multiplexed and acquired one by one through the eCAP embedded peripheral by the CPU, while the fault inputs are in OR-ing configuration to obtain a main fault signal for the DAB converter and another for the Buck interleaved stage.

For temperature measurement purposes, in particular for magnetic components, ten NTC inputs are handled by typical voltage divider configuration and opamp for signal

buffering. Then, a multiplexer controlled by uC acquires each temperature signal for a fixed period, still faster than temperature time-constants.

4. System Implementation and Preliminary Functional Tests

4.1. Hardware System

The compactness of the design enabled by the described choices on technologies and operating frequency enabled the placement of the entire DC-DC converter in a single standard 19' rack cabinet (2200 × 800 × 800 mm). The layout of the entire system was accurately developed in a 3D CAD: the accuracy of the 3D design of the system is very important for an accurate placement of all the components: this is fundamental to minimize parasitic effects, avoid strong interference and spurious signal couplings and to optimize the cooling system effectiveness. Figure 22 gives a frontal view of the system, highlighting three main sections. Section A is made of the primary bus-bar, capacitors forming C_{bus}, the primary-side full-bridge of DAB and the planar transformer. In section B, there are the two secondary-side bus-bars that connect the secondary-side full-bridges of the DAB and Buck-interleaved converters, including the first filtering stage (L_1, $C_{F1,2}$). Lastly, section C is basically the output filter of the system, consisting of L_2 and C_{out}. In the picture of Figure 23, a secondary side bus bar connecting the SiC modules of the secondary-side bridge of the DAB to the SiC modules of the Buck converter is provided. It is interesting to notice that the connections among sections have different requirements. In the DAB stage, the AC current flowing between power modules and the transformer has a 50 kHz fundamental and a non-negligible third harmonic. Considering, in addition, the skin effect, Litz cables have been chosen. The currents flowing into Buck filters have a reduced AC component at 50 kHz ($20A_{RMS}$) thanks to L_1 inductors; however, the same previous Litz cables are used for maximum performance. Instead, simple connection bars are used in section C given the negligible PWM content of output current.

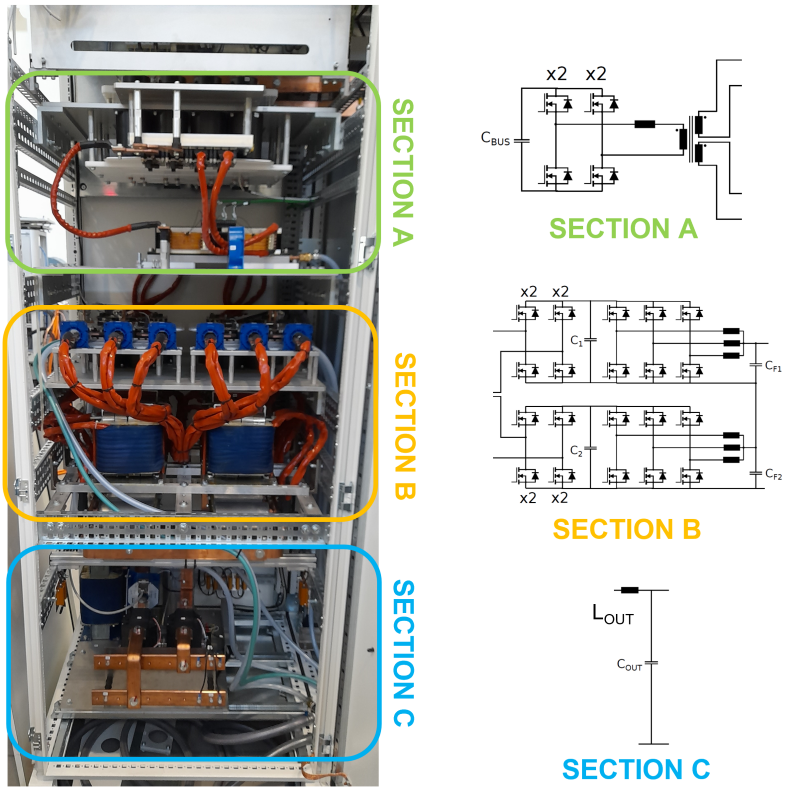


Figure 22. Power system picture and associated block diagrams.

The developed Control Board and the Auxiliary Supply Board are shown in Figure 24. They have been implemented in four-layer FR4 PCBs. The dimensions of the Control Board are 215 × 301 mm. This board can be divided into five macro sections, highlighted by rectangles in the picture. The central rectangle (white) includes the CPU and the communication peripherals, the bottom rectangle (yellow) the driver connectors and transceivers, the right one (red) the supply signals for the digital and analog components, the upper left (orange) the voltage sensing, and the last one (blue) the current sensing. The Auxiliary Supply Board has dimensions of 150 × 160 mm. The Flyback circuit is within the yellow rectangle, while the Buck for the digital 5 V is in the blue one.

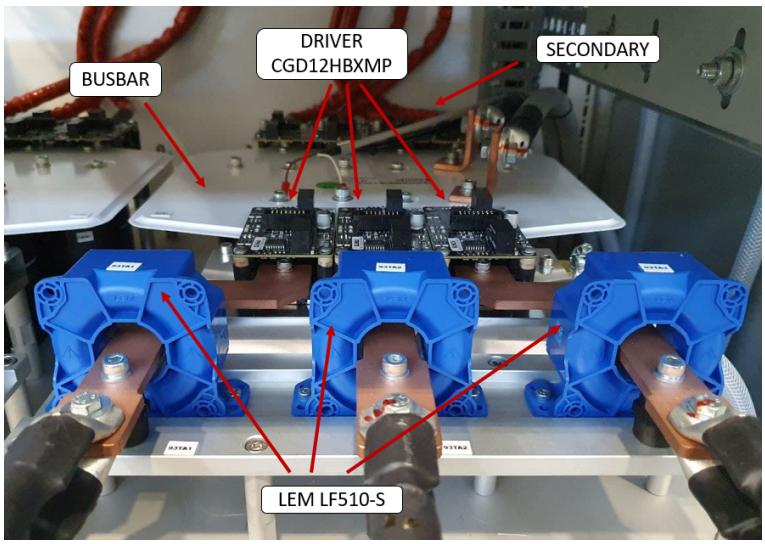
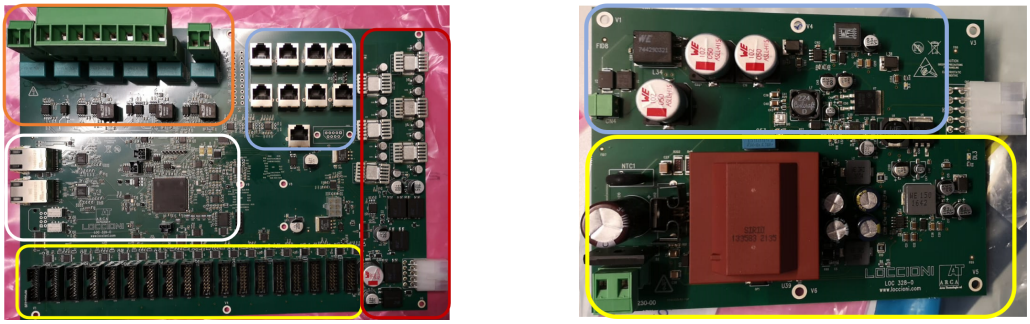


Figure 23. Secondary side Bus-bar and SiC power modules with drivers.



(**a**) Control Board (**b**) Supply Board

Figure 24. PCBs for the control algorithm managing.

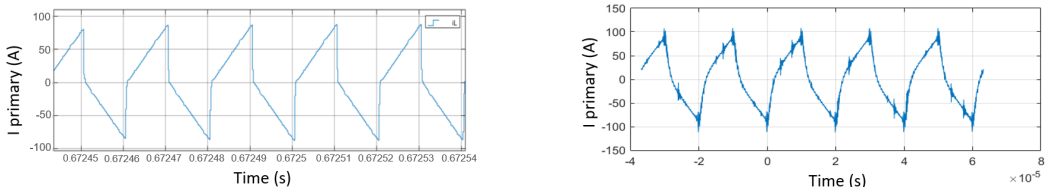
4.2. Experimental Results

Some preliminary functional tests have been carried out on a part of the prototype converter. The testing setup is made of the DAB converter kept in open-loop (fixed ϕ), with one secondary left in open circuit, while the other is connected to the Buck interleaved converter in closed-loop control. The input voltage is provided by the ITECH IT6018C-1500-40 power supply, while the load is made of four parallel power resistors of 10 Ω, 6 kW each. The characteristics of the power supply limit the test to 18 kW of input power. A 16kW output power test was carried out to preliminarily test the functionality of the system. A PSIM-Simulink co-simulation was carried out with the same conditions. The expected voltages for the different sections of the converter in this test are listed in Table 6.

Table 6. 16 kW test.

V_{in}	V_{DAB}	V_{out}	P_{out}
420 V	280 V	200 V	16 kW

It can be noticed that the voltage produced by the DAB converter V_{DAB} is just V_{in} multiplied by the transformer winding factor. Indeed, for this low power target, the phase-shift value is absorbed by the dead-time without regulating V_{DAB}. The measured values of the primary current of the transformer and of the voltages are shown in Figures 25 and 26, and are in fairly good accordance with the simulations. This test is a preliminary indication of the effectiveness of the design of the power converter and controlling boards, and of the usefulness of the developed simulation set up that is capable of reproducing the actual converter operation even in a regime very far from nominal operation.



(**a**) Simulation (**b**) Scope acquisition

Figure 25. Primary current of the transformer in the 16 kW functional test.

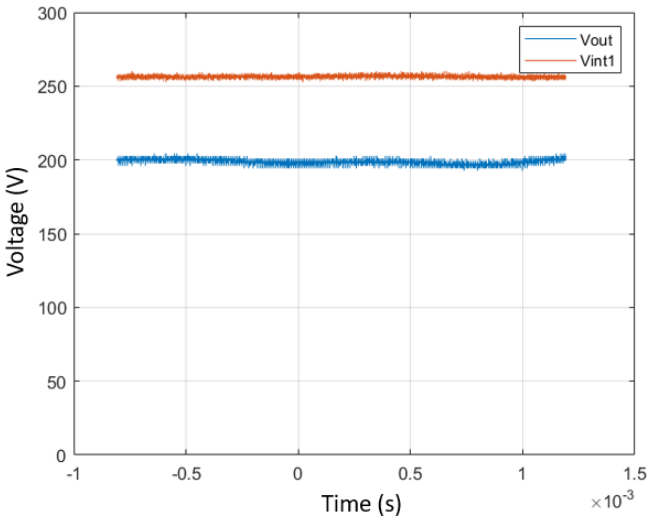


Figure 26. V_{DAB} and V_{out} scope acquisitions for the 16 kW test.

After these preliminary functional tests, the same configuration of the set up (i.e., with a single branch of the secondary side of the DAB connected to an interleaved Buck converter) has been connected to a 100 kW power supply and an 80 kW electronic load to test the system in an higher power regime. In this high-power test bench, the converter was tested in three different steady state conditions, with the DAB converter working in Boost Mode, Buck mode and Nominal mode (i.e., $Vin = nVout$ in the DAB waveforms). The measured waveforms of the primary side current and primary/secondary side voltages of the DAB converter for these characterizations are shown in Figures 27–29: the waveforms are very clean and the shape of the primary side current (i.e., the slope of the current) is clearly representative of Boost mode (Figure 27), Buck mode (Figure 28) and Nominal mode (Figure 29) operating regimes. In Table 7, the corresponding measured performances of the converter for these three tests are listed. It can be noted that the overall efficiency is very high, even for those operating points at about a third of full power (considering that only half of the converter is operating), and the results are in very good accordance with what

was expected from the simulations. The complete system will undergo a complete set of functional and performance e tests at the Loccioni Laboratories before final industrialization and commercialization.

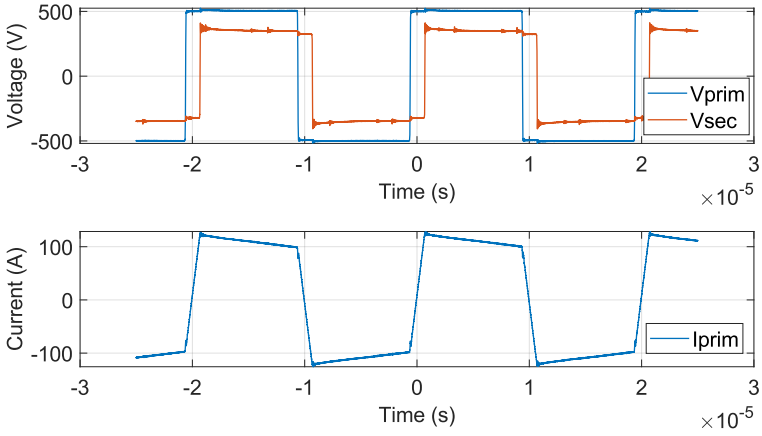


Figure 27. Measured primary and secondary voltage waveforms and input current of the DAB operating in Boost mode with the system delivering $Pout = 49.6$ kW.

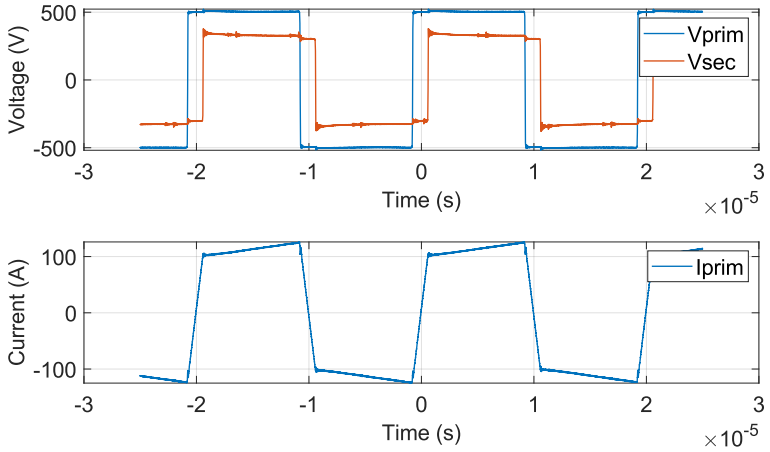


Figure 28. Measured primary and secondary voltage waveforms and input current of the DAB operating in Buck mode with the system delivering $Pout = 49.6$ kW.

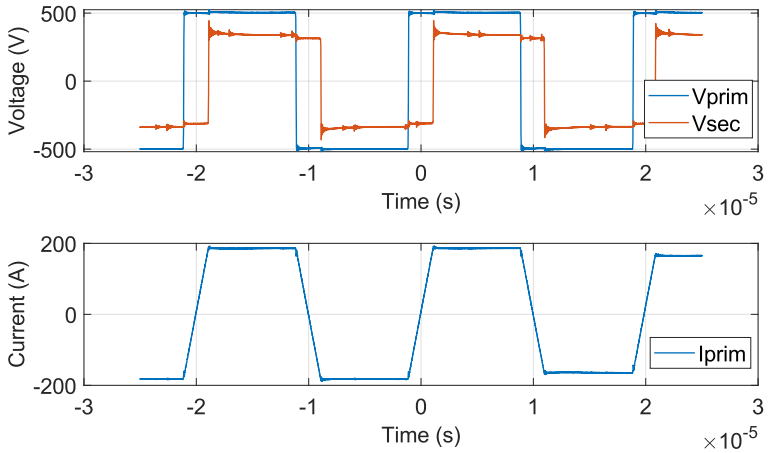


Figure 29. Measured primary and secondary voltage waveforms and input current of the DAB operating in nominal mode (i.e., unit voltage gain) with the system delivering $Pout = 70$ kW.

Table 7. Main results for the test in steady-state condition for the single-branch working configuration (with parallelized power modules on DAB primary side).

Case	ϕ	V_{in}	I_{in}	P_{in}
Boost Mode	23.7°	510 V	101.18 A	51.6 kW
Buck Mode	24.9°	510 V	101.18 A	51.6 kW
Nominal Mode	40.2°	510 V	143 A	72.9 kW
$V_{out,DAB}$	V_{out}	I_{out}	P_{out}	**efficiency**
350 V	200 V	248 A	49.6 kW	96.1%
330 V	200 V	248 A	49.6 kW	96.1%
340 V	200 V	350 A	70 kW	96%

5. Conclusions

The design of a 350 kW DC-DC power converter to be used as a battery emulator for automotive component testing has been described. The design choices in terms of components, technologies, circuit topologies and control architecture enable state-of-the-art performance in a compact and easily deployable instrument solution. The instrument has been fully implemented, and tests at up to more than one third of full power have shown results that match the design goal and simulations. The system is undergoing final testing before industrialization and commercialization.

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References

1. König, A.; Nicoletti, L.; Schröder, D.; Wolff, S.; Waclaw, A.; Lienkamp, M. An Overview of Parameter and Cost for Battery Electric Vehicles. *World Electr. Veh. J.* **2021**, *12*, 21. [CrossRef]
2. Rubén, H.L.; Gonzalo, A.P.; Pablo, J.R.; Guillermo, S.I.; Javier, U.G. A Survey on Technologies to Implement Battery Emulators based on DC/DC Power Converters. In Proceedings of the 14th LACCEI International Multi-Conference for Engineering, Education, and Technology, San José, Costa Rica, 20–22 July 2016.
3. Schmuch, R.; Wagner, R.; Hörpel, G.; Placke, T.; Winter, M. Performance and cost of materials for lithium-based rechargeable automotive batteries. *Nat. Energy* **2018**, *3*, 267–278. [CrossRef]
4. Ding, X.; Zhang, D.; Cheng, J.; Wang, B.; Luk, P.C.K. An improved Thevenin model of lithium-ion battery with high accuracy for electric vehicles. *Appl. Energy* **2019**, *254*, 113615. [CrossRef]
5. Xiong, R.; He, H.; Zhao, K. Research on an Online Identification Algorithm for a Thevenin Battery Model by an Experimental Approach. *Int. J. Green Energy* **2015**, *12*, 272–278. [CrossRef]
6. Shepherd, C.M. Design of Primary and Secondary Cells. *J. Electrochem. Soc.* **1965**, *112*, 657. [CrossRef]
7. ERS-BIC High Dynamic DC-Source-Sink. Available online: https://www.heinzinger.com/en/power-supplies/bi-directional-energy-recovery-capable/ers-bic-battery-simulation/ (accessed on 20 February 2023).
8. FEV Website. Available online: https://www.fev-sts.com/en.html (accessed on 20 February 2023).
9. HEV/EV/Grid Emulators and Test Systems. Available online: https://www.keysight.com/us/en/products/hev-ev-grid-emulators-and-test-systems.html (accessed on 20 February 2023).
10. Battery Simulator/Emulator. Available online: https://unicous.com/automotive-testing/ev-and-hev-testing/battery-emulator (accessed on 20 February 2023).
11. Powersim. PSIM User's Guide, Rev. 1. 2020. Available online: https://powersimtech.com/wp-content/uploads/2021/01/PSIM-User-Manual.pdf (accessed on 20 February 2023).

12. Klitzing, J.; Schäfer, U. A Highly Dynamic 600 V/300 A Battery Emulator for Testing of Automotive Electric Drive Trains. In Proceedings of the 2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), Ghent, Belgium, 6–10 September 2021; pp. 1–10. [CrossRef]
13. Dash, S.; Chandorkar, M. Battery Emulation Using Dual-Active Bridge Converter. In Proceedings of the 2019 National Power Electronics Conference (NPEC), Tiruchirappalli, India, 13–15 December 2019; pp. 1–6. [CrossRef]
14. Mishra, S.; Sreekanth, T.; Mohan, N. Bidirectional AC/DC Converter using GaN HEMT based Non-Isolated DAB for Battery Emulation. In Proceedings of the 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 11–15 October 2020; pp. 5641–5647. [CrossRef]
15. Mishra, S.; Tamballa, S.; Pallantala, M.; Raju, S.; Mohan, N. Cascaded Dual-Active Bridge Cell Based Partial Power Converter for Battery Emulation. In Proceedings of the 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, ON, Canada, 17–20 June 2019; pp. 1–7. [CrossRef]
16. Deda, S.; Eder, A.; Mhetre, V.; Kuchling, A.; Greul, R.; Koenig, O. Designing a Battery Emulator/Tester from Scratch to Prototyping to Automated Testing within a HIL Digital Twin Environment. In Proceedings of the PCIM Europe Digital Days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremburg, Germany, 7–8 July 2020; pp. 1–8.
17. Baumhöfer, T.; Waag, W.; Sauer, D. Specialized battery emulator for automotive electrical systems. In Proceedings of the 2010 IEEE Vehicle Power and Propulsion Conference, Lille, France, 1–3 September 2010; pp. 1–4. [CrossRef]
18. Li, R.; Ji, Y.; Fu, Y.; Hu, B.; Hu, H. Design and implementation of a parametric battery emulator based on a power converter. *IET Electr. Power Appl.* **2022**, *16*, 1300–1316. Avaliable online: https://ietresearch.onlinelibrary.wiley.com/doi/pdf/10.1049/elp2.12228 (accessed on 20 February 2023). [CrossRef]
19. Michalczuk, M.; Ufnalski, B.; Grzesiak, L.; Rumniak, P. Power converter-based electrochemical battery emulator. *Prz. Elektrotechniczny* **2014**, *90*, 18–22. [CrossRef]
20. Thanheiser, A.; Meyer, W.; Buecherl, D.; Herzog, H.G. Design and investigation of a modular battery simulator system. In Proceedings of the 2009 IEEE Vehicle Power and Propulsion Conference, Dearborn, MI, USA, 7–10 September 2009; pp. 1525–1528. [CrossRef]
21. Gefran. AFE200-72000-KXX-4-MS Instruction Manual, Rev. 0.11. 2016. Avaliable online: https://www.manualslib.com/manual/1912655/Gefran-Afe200-Series.html (accessed on 20 February 2023).
22. Qiu, Y.; Yao, K.; Meng, Y.; Xu, M.; Lee, F.; Ye, M. Control-loop bandwidth limitations for multiphase interleaving buck converters. In Proceedings of the Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04, Anaheim, CA, USA, 22–26 February 2004; Volume 2, pp. 1322–1328. [CrossRef]
23. Aprilianto, R.A.; Firmansyah, E.; Wijaya, F.D. Review on Control Strategy for Improving The Interleaved Converter Performances. In Proceedings of the 2021 4th International Seminar on Research of Information Technology and Intelligent Systems (ISRITI), Yogyakarta, Indonesia, 16–17 December 2021; pp. 312–317. [CrossRef]
24. Millán, J.; Godignon, P.; Perpiñà, X.; Pérez-Tomás, A.; Rebollo, J. A Survey of Wide Bandgap Power Semiconductor Devices. *IEEE Trans. Power Electron.* **2014**, *29*, 2155–2163. [CrossRef]
25. CREE-Wolfspeed. CAB425M12XM3 Datasheet. 2020. Avaliable online https://assets.wolfspeed.com/uploads/2020/12/cab425m12xm3.pdf (accessed on 20 February 2023).
26. Lagier, T.; Chédot, L.; Ghossein, F.W.L.; Lefebvre, B.; Dworakowski, P.; Mermet-Guyennet, M.; Buttay, C. A 100 kW 1.2 kV 20 kHz DC-DC converter prototype based on the Dual Active Bridge topology. In Proceedings of the 2018 IEEE International Conference on Industrial Technology (ICIT), Lyon, France, 20–22 February 2018; pp. 559–564. [CrossRef]
27. Sommer, F.; Menger, N.; Merz, T.; Soltau, N.; Idaka, S.; Hiller, M. Design and Characterization of a 500 kW 20 kHz Dual Active Bridge using 1.2 kV SiC MOSFETs. In Proceedings of the 2022 International Power Electronics Conference (IPEC-Himeji 2022-ECCE Asia), Himeji, Japan, 15–19 May 2022; pp. 1390–1397. [CrossRef]
28. Bündgen, D.; Thönnessen, A.; Fritz, N.; Kamp, T.; De Doncker, R.W. Highly Integrated 200 kW SiC Three-Phase Dual-Active-Bridge Converter with 3D-Printed Fluid Coolers. In Proceedings of the 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Redondo Beach, CA, USA, 7–11 November 2021; pp. 182–187. [CrossRef]
29. Haneda, R.; Akagi, H. Power-Loss Characterization and Reduction of the 750-V 100-KW 16-KHz Dual-Active-Bridge Converter With Buck and Boost Mode. *IEEE Trans. Ind. Appl.* **2022**, *58*, 541–553. [CrossRef]
30. Krismer, F. Modeling and Optimization of Bidirectional Dual Active Bridge DC–DC Converter Topologies. Ph.D. Thesis, ETH Zurich, Zürich, Switzerland, 2011.
31. Song, L.; Ramakrishnan, H.; Navaneeth Kumar, N.; Bhardwaj, M. Bi-Directional, Dual Active Bridge Reference Design for Level 3 Electric Vehicle Charging Stations. Technical Report TIDA-010054, Texas Instruments. 2019. Avaliable online: https://www.ti.com/tool/TIDA-010054 (accessed on 20 February 2023).
32. Giuliani, F. Dc-Dc Power Converters Featuring Wide-Bandgap Devices. Ph.D. Thesis, Università di Parma, Parma, Italy, 2016.
33. Zhao, B.; Song, Q.; Liu, W.; Sun, Y. Dead-Time Effect of the High-Frequency Isolated Bidirectional Full-Bridge DC–DC Converter: Comprehensive Theoretical Analysis and Experimental Verification. *IEEE Trans. Power Electron.* **2014**, *29*, 1667–1680. [CrossRef]
34. Mi, C.; Bai, H.; Wang, C.; Gargies, S. Operation, design and control of dual H-bridge-based isolated bidirectional DC–DC converter. *IET Power Electron.* **2008**, *1*, 507–517. [CrossRef]

35. Ouyang, Z.; Andersen, M.A.E. Overview of Planar Magnetic Technology—Fundamental Properties. *IEEE Trans. Power Electron.* **2014**, *29*, 4888–4900. [CrossRef]
36. 300kW XM3 Three-Phase Inverter. Avaliable online: https://assets.wolfspeed.com/uploads/2021/06/CPWR-AN30.pdf (accessed on 20 February 2023).
37. Yi, P.; Cui, Y.; Vang, A.; Wei, L. Investigation and evaluation of high power SiC MOSFETs switching performance and overshoot voltage. In Proceedings of the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4–8 March 2018; pp. 2589–2592. [CrossRef]
38. Tang, Y.; Li, X.; Zhou, S.Z.; Sun, C.; Chen, G. Comprehensive study of fast load modulation with volt-second balance in a dual-active-bridge converter. *IET Power Electron.* **2019**, *12*, 1357–1367. Avaliable online: https://ietresearch.onlinelibrary.wiley.com/doi/pdf/10.1049/iet-pel.2018.5894 (accessed on 20 February 2023). [CrossRef]
39. POWERSIM. TUTORIAL SimCoupler Module. 2020. Avaliable online: https://powersimtech.com/resources/tutorials/simcoupler-module (accessed on 20 February 2023).
40. Power Integration. TOP252-262, TOPSwitch-HX Family, Rev. H. 2013. Avaliable online: https://www.power.com/products/topswitch/topswitch-hx/top252gn (accessed on 20 February 2023).
41. Texas Instruments. TMS320F2838x Real-Time Microcontrollers with Connectivity Manager, Rev. 2. 2021. Avaliable online: https://www.ti.com/microcontrollers-mcus-processors/c2000-real-time-control-mcus/overview.html (accessed on 20 February 2023).
42. Beckhoff. EtherCat Slave Controller. 2019. Avaliable online: https://www.beckhoff.com/en-en/products/i-o (accessed on 20 February 2023).
43. British Standards Institution. *International Electrotechinical Commission;* British Standards Institution: London, UK, 2019; ISBN 2832265014/9782832265017.
44. Texas Instruments. DS90LV032ATMTCX Datasheet. 2016. Avaliable online: https://www.ti.com/product/DS90LV032A (accessed on 20 February 2023).
45. Texas Instruments. SN65C1167EPWR Datasheet. 2016. Avaliable online: https://www.ti.com/product/SN65C1167E (accessed on 20 February 2023).