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Investigation on the performance limits of Dirac-source FETs

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ABSTRACT

In this work, we develop a two-dimensional (2D) simulation tool addressing Poisson's equation within the semiconductor section of a 2D Dirac source (DS) field-effect transistor under the assumption of ballistic transport. Next, we compute the current curves using the WKB approximation for the calculation of the transmission probability. The current turns out to be quite sensitive to the tunneling probability at the graphene-semiconductor heterojunction. Different gate-insulating materials and gate lengths are considered with the aim of identifying any possible limitations in the performance of DS-FETs. The obtained results highlight some important issues, while confirming that a minimum subthreshold swing (SS) of 40 mV/dec can be achieved and that SS values below 60 mV/dec can be extended up to three and a half decades.

1. Introduction

In recent years, much effort has been devoted to the investigation of steep-slope FETs [1–4] with the aim of lowering the supply voltage as well as the power consumption in logic circuits. Several physical mechanisms have been devised to achieve this goal, including, but not limited to: (i) energy filtering of electrons injected into the channel, (ii) negative-gate capacitance, (iii) nanoelectromechanical switching and (iv) regenerative effects based on impact-ionization. None of the above proposals has reached the industrial development stage, due to a variety of limitations widely discussed in literature.

The investigation in the area of the first device-class mentioned above has been recently enriched by a novel proposal: exploiting the conical band structure of graphene to control high-energy electron injection into the channel of a transistor based on a two-dimensional (2D) channel material [5–8]. Due to the properties of electrons in graphene, behaving as massless Dirac-fermions, these devices are called Dirac-Source FETs (DS-FETs). Subsequent studies have investigated their potential based on semi-quantitative considerations [7] and discussed possible limitations [8] related with various material non-idealities.

In this work, we pursue a 2D numerical solution of Poisson' s equation within the semiconductor section of the DS-FET under the assumption of ballistic transport. Simulation results are carried out for different gate lengths and gate-insulating materials. Next, we compute the current curves using the WKB approximation for the calculation of the transmission probability. The current turns out to be quite sensitive to the tunneling probability at the graphene-semiconductor heterojunction. This highlights the importance of obtaining a precise 2D solution for the electrostatic potential within the semiconductor. To conclude, some remarks on the results are provided.

2. Device electrostatics

Device electrostatics is investigated under the assumption of a zero thickness for the 2D semiconductor (2DSC) monolayer, resulting in a delta-like electron distribution. This assumption is, in our view, legitimate, since the thickness of a two-dimensional semiconductor is minimal, leading to a practically negligible voltage drop across the semiconductor [9]. For instance, in this work we focused on monolayer MoS_2, which has a thickness of approximately 0.65 nm. With this approach, it is sufficient to solve the Laplace equation within the oxide and use the charge density per unit area to establish the appropriate non-homogeneous Neumann boundary condition at the semiconductor interface. Dirichlet conditions, instead, are applied at the top edge of the domain (gate electrode) and at the two bottom corners (source and drain contacts). A sketch of the device structure is shown in Fig. 1(a). The green dashed box highlights the region where the 2D Poisson equation is solved. Additionally, a sketch of the band structure is depicted in Fig. 1(b). The source Fermi level E_{FS}, and the energy difference between the Dirac point energy under the control gate and the source Fermi level ($\tilde{E}_{Dirac}$) are also indicated. In the following, we denote x as the coordinate that has its origin at the Gr-MoS_2 heterojunction and extends in the transport direction. Graphene is considered as an injecting contact. The two-dimensional charge density is the sum of the source and drain contributions $n = n_S + n_D$. However, when V_{DS} is sufficiently large, the electrons available for transport are only those from the source contact. Thus, the total electron charge can

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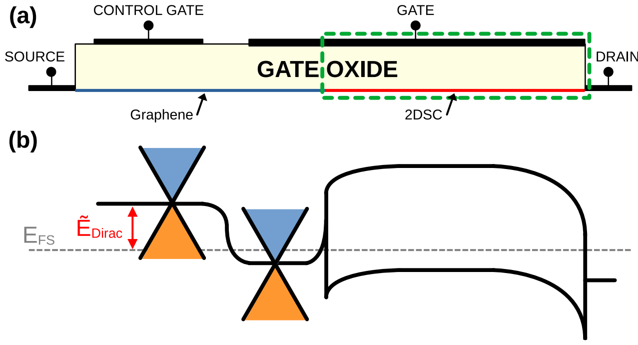

Fig. 1. (a) Device structure. Graphene (blue region) is directly contacted to the MoS_2 channel (red region). The control gate is used to change the position of $\tilde{E}_{\rm Dirac}$, the energy difference between the Dirac point energy and the source Fermi level $E_{\rm FS}$. The green dashed box highlight the simulation domain. (b) Schematic band structure showing the density of states of graphene and the conduction and valence band of the semiconductor.

be simplified as

$$n(x) \simeq n_S(x) = N_{\rm 2D}\, \mathcal{F}_0 \left[\frac{E_{\rm FS} - E_c(x)}{k_{\rm B}{\rm T}} \right], \tag{1}$$

where $\mathcal{F}_0(\xi) = \ln[1+\exp(\xi)]$ is the Fermi integral of order zero, E_c the conduction band profile in the semiconductor channel, $E_{\rm FS,D}$ the Fermi energies at the source and drain contacts respectively, $k_{\rm B}$ the Boltzmann constant, and T the temperature. $N_{\rm 2D} = g_c k_{\rm B}{\rm T}\, m^*/\pi\hbar^2$ is the effective density of states of the 2D semiconductor, with g_c the conduction band valley degeneracy, m^* the electron effective mass, and $\hbar$ the reduced Planck constant. In the case of monolayer MoS_2, the parameter $N_{\rm 2D} = 2k_{\rm B}{\rm T}\,(0.51\, m_0)/\pi\hbar^2 = 11.01 \times 10^{12}\,{\rm cm}^{-2}$ at room temperature. Eq. (1) clearly indicates that the electron density consists of one half of the electrons with positive velocity coming from the source contact, plus another half with negative velocity coming from the drain. As the charge density depends on the local potential, an iterative procedure is required to solve the problem. Eq. (1) neglects the filtering action of graphene on the charge entering the semiconductor channel. Nevertheless, it provides a quick, "first-order" estimation of the electron density, even though it is not fully consistent. The filtering action is taken into account in the current calculation. It is worth noting that the simulation approach can be extended to a double-gate structure by simply considering a doubled amount of charge $Q_n^{\rm DG} = 2\,Q_n$.

Fig. 2 shows the MoS_2 conduction band profiles in the transport direction for two gate insulators, namely HfO_2 and SiO_2, and two gate lengths, namely L_g = 10 nm and L_g = 3 nm, at different gate voltages. In all cases, an effective oxide thickness (EOT) of 1 nm is considered. The HfO_2 gate insulator induces a significant reduction in the barrier height within the channel at low gate voltages, along with a smoother transition of the electrostatic potential from the boundaries to the central values, predominantly influenced by the gate bias. Consequently, for a fixed gate length, the high-κ dielectric is expected to lead to a rise in short-channel effects.

3. Drain current

Under the assumption of ballistic transport, the device turn-on characteristics can be computed using Landauer's equation [10,11]. Specifically, the ballistic current equation can be modified to account for the low-pass energy filtering effect of graphene, as in [7,8]

$$\begin{aligned} I_{\rm DS} &= \frac{2q}{h} \int M(E)T(E)[f(E-E_{\rm FS}) - f(E-E_{\rm FD})]\,{\rm d}E \\ &\simeq \frac{2q}{h} \int_{E_c(0)}^{\infty} M_{\rm Gr}(E)T(E)[f(E-E_{\rm FS}) - f(E-E_{\rm FD})]\,{\rm d}E, \end{aligned} \tag{2}$$

where q is the elementary charge, h the Planck constant, $T(E)$ the transmission probability, and $f(E-E_{\rm FS,D})$ the Fermi distribution function

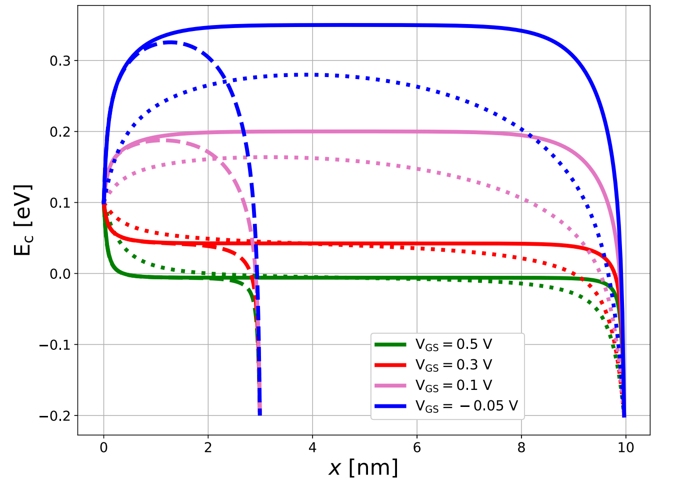

Fig. 2. Conduction band profiles in the lateral direction for two gate lengths, namely L_g = 10 nm and L_g = 3 nm and two gate-insulating materials, SiO_2 and HfO_2, at different gate voltages, ranging from −0.05 V to 0.5 V. $E_c(0)$ = 0.1 eV is assumed. Solid lines: SiO_2 gate insulator and L_g = 10 nm. Dotted lines: HfO_2 gate insulator and L_g = 10 nm. Dashed lines: SiO_2 gate insulator and L_g = 3 nm. All curves refer to a device having an EOT of 1 nm. A substantial lowering of the potential barrier occurs within the channel at low gate voltages with the HfO_2 dielectric.

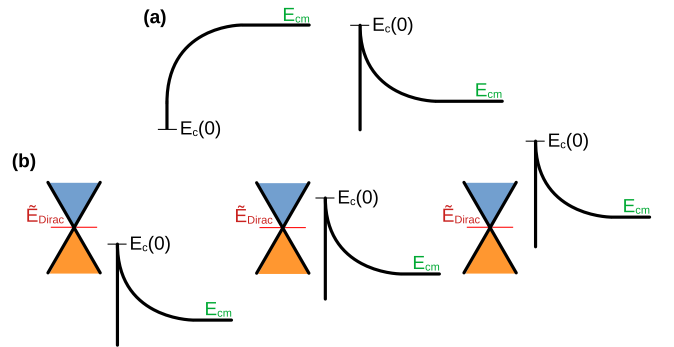

Fig. 3. (a) Schematic shape of the initial portion of the MoS_2 conduction band in substhreshold and strong inversion regimes. (b) The relative energy position of graphene DoS with respect to the channel conduction band is an essential factor to be considered. The Dirac point $\tilde{E}_{\rm Dirac}$, the first point of the conduction band $E_c(0)$, and the minimum/maximum of the conduction band E_{cm} are highlighted. These three scenarios are pivotal for accurately estimating the tunneling current.

at the source and drain electrodes. The parameter $M(E)$ in the first of the (2) is the number of modes, or conductive channels, of the material under consideration. In the relevant energy range, the number of modes of graphene $M_{\rm Gr}(E) = W\,2|E - \tilde{E}_{\rm Dirac}|/\pi\hbar v_{\rm F}$ [7] is lower than that of the 2DSC, therefore M(E) in the Landauer formula is determined by $M_{\rm Gr}(E)$, while the semiconductor channel behaves as a gate-tunable energy barrier. The device width is denoted by the parameter W, which we assume to be 1 μm.

If we assume perfect transmission ($T = 1$) over the barrier, and zero tunneling below it, the current can be extracted analytically and it is equal to

$$\begin{aligned} I_{\rm DS} = I_0 &\left\{ (\tilde{\mu}_{\rm Dirac} - \eta_{cm}) \ln\left(\frac{1+\exp(\mu_{\rm FS} - \eta_{cm})}{1+\exp(\mu_{\rm FD} - \eta_{cm})} \right) \right. \\ &+ 2[\exp(\mu_{\rm FS} - \tilde{\mu}_{\rm Dirac}) - \exp(\mu_{\rm FD} - \tilde{\mu}_{\rm Dirac})] \\ &\left. - \sum_{n=1}^{\infty} \frac{(-1)^{n-1}}{n^2} \{\exp[n(\mu_{\rm FS} - \eta_{cm})] - \exp[n(\mu_{\rm FD} - \eta_{cm})]\} \right\}, \end{aligned} \tag{3}$$

where $\tilde{\mu}_{\rm Dirac}$, $\mu_{\rm FS,D}$, η_{cm} are the normalized energies, namely the energies divided by $k_{\rm B}{\rm T}$, E_{cm} the maximum of the conduction band (see Fig.

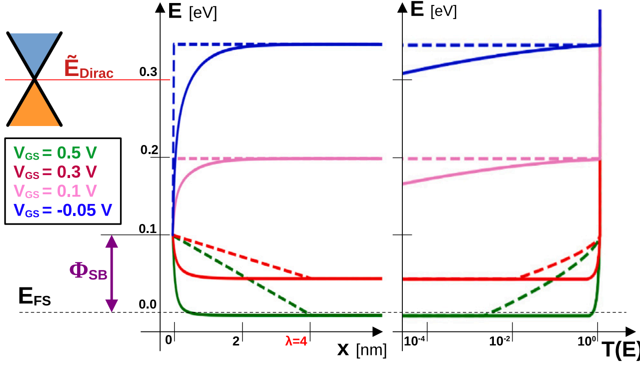

Fig. 4. Left: comparison between the numerical band profiles and the triangular band approximation used in [7], for some gate voltages. $E_c(0) = 0.1$ eV is assumed. Right: transmission probability calculated with the WKB approximation in semi-logarithmic scale. Dashed lines refer to the triangular band approximation, while solid lines to numerically extracted band profiles. $T(E)$ is underestimated with a triangular barrier of 4-nm length, thus leading to an underestimation of the current (see Fig. 5).

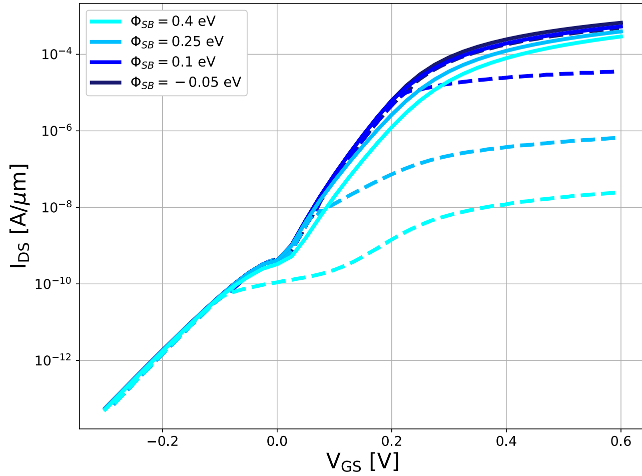

Fig. 5. Transfer characteristics of the DS-FET with a gate length $L_g = 10$ nm and a SiO_2 gate dielectric for different values of ϕ_{SB}. Solid lines: presented model. Dashed lines: Tunneling probability computed with the assumption of a triangular tunneling barrier with a base width of 4 nm [7]. Assuming a fixed tunneling barrier width clearly leads to an underestimation of the current, as it overstates the actual tunneling width.

3), and $I_0 = W\, q(k_B T)^2/\pi^2\hbar^2 v_F$. The summation comes from the series integration of (2) in the energy interval $E_{cm} < E < \tilde{E}_{\mathrm{Dirac}}$.

An important design aspect is that of matching the conduction band with the Dirac energy at zero V_{GS}, i.e. $E_{cm} = \tilde{E}_{\mathrm{Dirac}}$. In doing so, the condition $E_{cm} \leq \tilde{E}_{\mathrm{Dirac}}$ for which Eq. (3) holds transforms into $V_{GS} \geq 0$.

Alternatively, if $V_{GS} < 0$ a Boltzmann-like distribution can be assumed, i.e. $f(E - E_F) = \exp[-(E - E_F)/k_B T]$. This assumption is justified by the fact that we are far from the Fermi energy level. Therefore, the current takes a simpler form:

$$I_{DS} = I_0 \left(\eta_{cm} - \tilde{\mu}_{\mathrm{Dirac}} + 1\right) \left[\exp(\mu_{FS} - \eta_{cm}) - \exp(\mu_{FD} - \eta_{cm})\right] . \tag{4}$$

In the limiting case of $\eta_{cm} = \tilde{\mu}_{\mathrm{Dirac}}$ and sufficiently high V_{DS}, Eq. (4) reduces to

$$\tilde{\mu}_{\mathrm{Dirac}} - \mu_{FS} = \ln\left(\frac{I_0}{I_{\mathrm{OFF}}}\right) . \tag{5}$$

The latter allows us to understand how the leakage current I_{OFF} varies when shifting the Dirac point $\tilde{E}_{\mathrm{Dirac}}$ relative to the source Fermi level E_{FS}. However, the analysis presented in [7] shows that there exist an optimal graphene doping level to minimize the gate voltage needed to turn on the device (i.e. to bring the current level from I_{OFF} to I_{ON}).

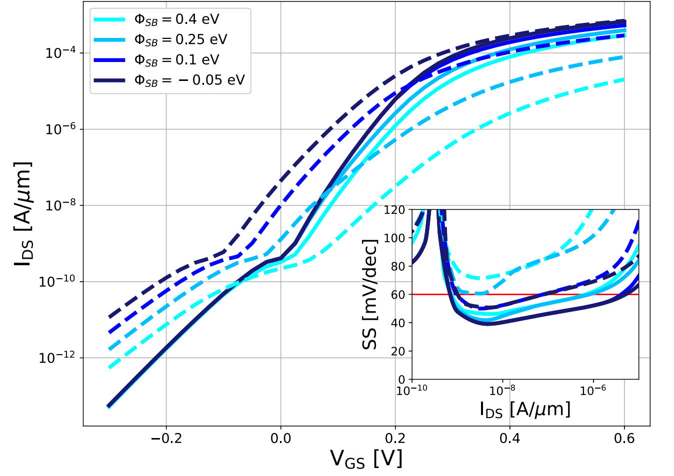

Fig. 6. Transfer characteristics of the DS-FET with a gate length $L_g = 10$ nm for different values of ϕ_{SB}. Solid lines: SiO_2 gate dielectric with thickness $t_{ox} = 1$ nm. Dashed lines: HfO_2 gate dielectric with the same EOT. Inset: SS comparison for the two devices. The use of HfO_2 as gate dielectric heavily degrades the subthreshold swing as well as the ON-state current at the highest barrier heights.

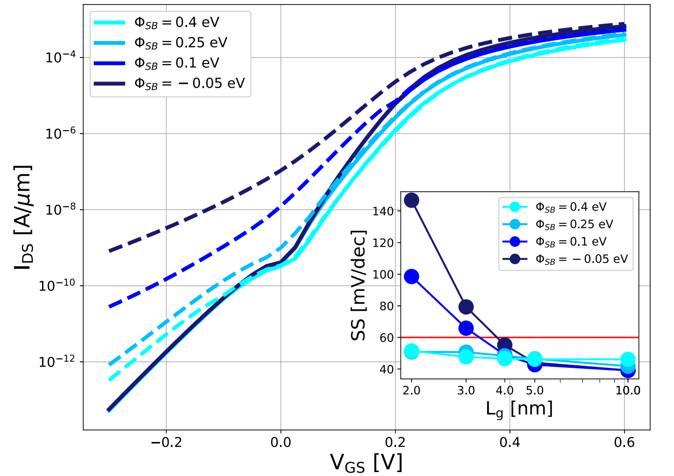

Fig. 7. Transfer characteristics of the DS-FET for two gate lengths, $L_g = 10$ nm and $L_g = 3$ nm, and different values of ϕ_{SB}. Solid lines: gate length $L_g = 10$ nm. Dashed lines: gate length $L_g = 3$ nm. Inset: minimum SS as a function of gate length in semi log axes. With low gate lengths the leakage current substantially increases and the SS degrades, as for conventional MOSFET devices.

3.1. Tunneling probability

In Eq. (3) we assumed the transmission probability $T(E)$ to be 1 for energies above E_{cm}. However, this assumption is not universally valid and results in an underestimation of the current when the Gr-MoS_2 barrier $\phi_{SB} = E_c(0) - E_{FS}$ becomes sufficiently high [7]. Therefore, to achieve a more accurate estimation of the current, it is essential to incorporate a non-ideal tunneling probability. Typically this implies numerically integrating Eq. (2). To evaluate this probability we apply the WKB approximation on band profiles obtained from the numerical solution of Poisson's equation (Section 2).

Fig. 3(a) illustrate the two possible shapes of the conduction band. One can notice that tunneling is consistent only if $E_c(0) > E_{cm}$, right case. In this case we can assume $T = 1$ above $E_c(0)$ and $T = 0$ below E_{cm}. On the other hand, Fig. 3(b) highlights some situations that must be taken into account when computing $T(E)$. The presence of the absolute value in M_{Gr} changes the definition of I_{DS} depending on whether E_{cm} is above or below $\tilde{E}_{\mathrm{Dirac}}$.

One method to reduce the simulation time and simplify the current expression is to use an analytical function to approximate the conduction band profile. A triangular barrier profile could be adopted, as shown in Fig. 4 (left), where a 4-nm length triangular barrier is plotted, as assumed in [7]. Fig. 4 (right) shows the tunneling probabilities calculated from the left-hand curves using the WKB approximation. $T(E)$ resulting from the numerically extracted bands exhibits a rapid increase with energy, owing to the steepness of the band profiles. Additionally, even in cases where $E_c(0) < E_{cm}$, these probabilities are non-zero for $E < E_{cm}$.

4. Simulation results

In this investigation, the Dirac energy below the graphene control gate is set at $\tilde{E}_{\text{Dirac}} = 0.3\,\text{eV}$, resulting in a leakage current I_{OFF} slightly below $10^{-9}\,\text{A/}\mu\text{m}$ at $V_{\text{GS}} = 0\,\text{V}$. Fig. 5 represents the turn-on characteristics of the DS-FET for various values of ϕ_{SB}. Solid lines are obtained from the numerical simulations, whereas the dashed lines are computed with the assumption of a triangular barrier with a 4-nm base width, as was done in Ref. [7]. The figure shows that the ON-state current is heavily underestimated with such a simplified potential profile, especially for the highest energy barriers. A more accurate approximation is discussed in Section 3.1. Fig. 6 shows the turn-on characteristics and SS for the SiO_2 (solid lines) and for the HfO_2 (dashed lines) gate-insulated DS-FETs. It is worth noting the degradation of both the ON-state current and SS caused by the high-κ dielectric.

Finally, Fig. 7 displays the turn-on curves for two different DS-FETs with gate length of 10 nm (solid lines) and 3 nm (dashed lines), along with the minimum SS as a function of L_g. The image shows a significant increase in the OFF-state current with decreasing channel length. Moreover, the typical 'kink' of the characteristic has disappeared. From the inset we can note that, low Gr-MoS_2 barriers ϕ_{SB} result in an increase in the inverse slope due to enhanced leakage current caused by source-to-drain tunneling.

5. Conclusions

This study proves that an accurate 2D potential profile is prerequisite for a quantitative prediction of DS-FET performances in view of future practical applications. We show that an SS below 60 mV/dec can be sustained over 3 to 4 orders of magnitude of currents. Additionally, this research demonstrates that DS-FETs can achieve an SS below 60 mV/dec even with channel lengths down to approximately 4 nm. However, the use of high-κ gate-insulating oxides is found to degrade the device performance, unless the oxide physical thickness can be scaled well below 5 nm with the aim to control 2D effects.

CRediT authorship contribution statement

Tommaso Ugolini: Writing – original draft, Software. **Elena Gnani:** Writing – review & editing, Supervision, Methodology, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

References

[1] Li X, et al. Emerging steep-slope devices and circuits: Opportunities and challenges. In: Topaloglu HS, editor. Beyond-CMOS technologies for next generation computer design. Cham: Springer, http://dx.doi.org/10.1007/978-3-319-90385-9_6.

[2] Gnani E, et al. Steep-slope devices: Prospects and challenges. J Nano Res 2016;39:3–16. http://dx.doi.org/10.4028/www.scientific.net/JNanoR.39.3.

[3] Cristoloveanu S, et al. A review of sharp-switching devices for ultra-low power applications. IEEE J the Electron Devices Soc 2016;4(5):215–26. http://dx.doi.org/10.1109/JEDS.2016.2545978.

[4] Zhang L, et al. Steep slope devices and TFETs. In: Zhang M, editor. Tunneling field effect transistor technology. Cham: Springer, http://dx.doi.org/10.1007/978-3-319-31653-6_1.

[5] Qiu C, et al. Dirac-source field-effect transistors as energy-efficient, high-performance electronic switches. Science 2018;361(6400):387–92. http://dx.doi.org/10.1126/science.aap9195.

[6] Liu F, et al. Dirac electrons at the source: Breaking the 60-mv/decade switching limit. IEEE Trans Electron Devices 2018;65(7):2736–43. http://dx.doi.org/10.1109/TED.2018.2836387.

[7] Wu P, Appenzeller J. Design considerations for 2-D Dirac-source FETs-part I: Basic operation and device parameters. IEEE Trans Electron Devices 2022;69(8):4674–80. http://dx.doi.org/10.1109/TED.2022.3181544.

[8] Wu P, Appenzeller J. Design considerations for 2-D Dirac-source FETs-part II: Nonidealities and benchmarking. IEEE Trans Electron Devices 2022;69(8):4681–5. http://dx.doi.org/10.1109/TED.2022.3181537.

[9] Ahmed Z, et al. Analytical monolayer MoS_2 MOSFET modeling verified by first principle simulations. IEEE Electron Device Lett 2020;41(1):171–4. http://dx.doi.org/10.1109/LED.2019.2952382.

[10] Landauer R. Spatial variation of currents and fields due to localized scatterers in metallic conduction. IBM J Res Dev 1957;1(3):223–31. http://dx.doi.org/10.1147/rd.13.0223.

[11] Datta S. Electronic transport in mesoscopic systems. Cambridge, U.K.: Cambridge Univ. Press; 1995.