A Bipolar Hybrid Symmetrical Cockcroft-Walton Voltage Multiplier for High-Voltage DC Power Supplies

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Sara Baldisserri
Dept. of Electrical, Electronic, and Information Engineering
University of Bologna
Bologna, Italy
sara.baldisserri2@unibo.it

Riccardo Mandrioli
Dept. of Electrical, Electronic, and Information Engineering
University of Bologna
Bologna, Italy
r.mandrioli@unibo.it

Gabriele Neretti
Dept. of Electrical, Electronic, and Information Engineering
University of Bologna
Bologna, Italy
gabriele.neretti@unibo.it

Mattia Ricco
Dept. of Electrical, Electronic, and Information Engineering
University of Bologna
Bologna, Italy
mattia.ricco@unibo.it

Andrea Cristofolini
Dept. of Electrical, Electronic, and Information Engineering
University of Bologna
Bologna, Italy
andrea.cristofolini@unibo.it

***Abstract*—Voltage multiplier circuits play a crucial role in high-voltage DC power supplies. This paper proposes a bipolar hybrid symmetrical Cockcroft-Walton voltage multiplier for DC high-voltage applications. It consists in the connection of a positive and negative symmetrical voltage multiplier and a shared diode bridge. The proposed topology combines the advantages of the most common symmetrical voltage multipliers, resulting in a smaller and better-regulated output voltage drop, as well as reduced high-voltage isolation requirements and component count. Additionally, it does not require a center-tapped high-voltage transformer, reducing the system's complexity. It fills the gap in the general framework of voltage multipliers and their respective bipolar topologies. The feasibility of the system has been numerically validated, and the performance of the proposed topology has been verified.**

***Index Terms*—Bipolar, DC high voltage, dynamic response, hybrid, output voltage regulation, symmetrical, voltage multiplier**

I. Introduction

High-voltage DC power supplies are widely used in various applications, including X-ray systems, electron microscopes, photon multipliers, and ion propulsion [1]–[8]. There are two basic approaches generally used to generate DC high voltage [9]–[11]. The first approach involves a high-turn-ratio transformer and high-breakdown-voltage diodes. However, the high-voltage transformer has several non-idealities that cause voltage and current spikes, leading to losses and noise. The second approach is to use a high-frequency inverter producing a fast, dynamic duty-cycle controllable voltage source, a transformer, and a Cockcroft-Walton voltage multiplier (VM) [12]–[15]. By using a VM, the turns ratio of the transformer, and thus the non-idealities mentioned above, can be significantly reduced. Additionally, VM circuits are characterized by high voltage step-up ratio and efficiency, low voltage stress on components, compactness, and easy implementation [16].

The concept of VMs was first introduced by Villard in 1901 and Greinacher in 1921, but gained notoriety thanks to Cockcroft and Walton nuclear experiment in 1932 [17]–[19]. The original VM was half-wave and suffered drawbacks like large output voltage ripple and drop. To overcome these problems, a symmetrical full-wave (FW) topology was developed by Heilpern in 1954 by adding an oscillating column of capacitors and a stack of diodes [20], [21]. The FW-VM has a significantly smaller output voltage ripple and drop but requires a center-tapped transformer (CTT), which increases the complexity of the system and could cause an asymmetry in the driving voltages, leading to harmonic generation in the DC output voltage [22]. In 2014, Iqbal proposed the hybrid (HY) VM by modifying the first stage, getting rid of the CTT and the first oscillating capacitor [23], [24]. Additionally, the bipolar approach was introduced to achieve a significant reduction in the high-voltage isolation requirements. The bipolar half-wave and the bipolar full-wave (BFW) VMs were proposed by Iqbal in 2007 and 2008, respectively. They consist in the connection of a positive and a negative bridge, improving the dynamic response and voltage regulation of the system [25]–[27].

In this paper, a bipolar hybrid (BHY) VM is proposed, adding a shared diode bridge between the two bridges of a BFW-VM. This topology combines the benefits of the previously introduced VMs, achieving a better-regulated output voltage drop, faster dynamic response, as well as reduced high-voltage isolation requirements and component count. Additionally, it does not require the CTT, reducing the system's complexity. The proposed BHY-VM fills the gap in the general framework of voltage multipliers and their respective bipolar topologies.

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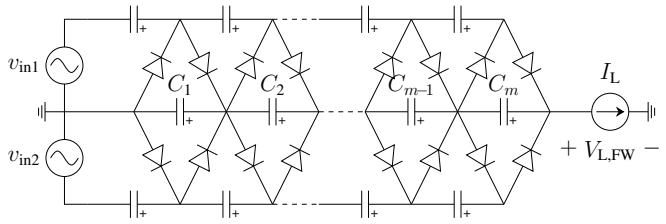
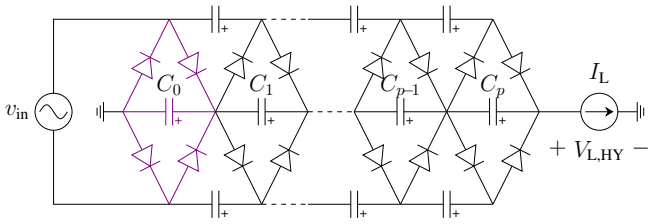
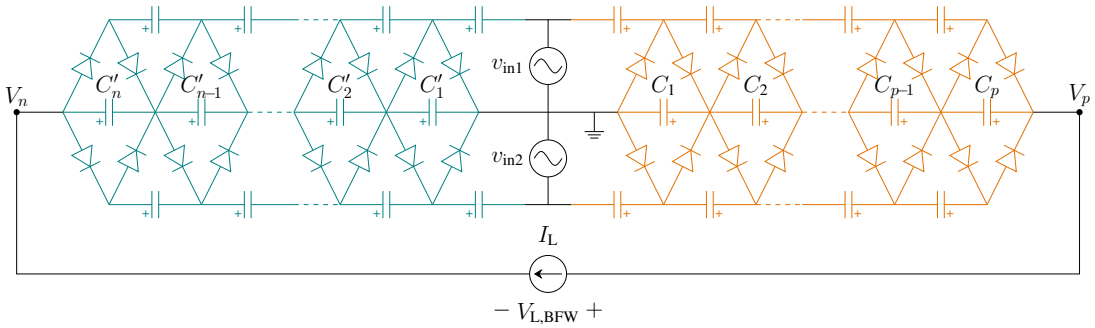


(a) m-stage FW-VM.



(b) m-stage HY-VM: diode bridge in violet and p-stage FW-VM; $p+1=m$.



(c) m-stage BFW-VM: p-stage positive FW-VM in orange and n-stage negative FW-VM in teal; $p+n=m$.

Fig. 1: Symmetrical VMs with m stages.

The rest of the manuscript is organized as follows: a background on symmetrical VMs is provided in Section II, while the proposed BHY-VM circuit topology, operation, and steady-state analysis are introduced in Section III. Section IV presents the calculation of the average output voltage of the described VMs. Section V provides the numerical validation, and Section VI draws conclusions.

II. Background on Symmetrical VMs

Fig. 1 represents the most popular symmetrical voltage multipliers used to date. In particular, Fig. 1a displays the FW-VM introduced in [21], Fig. 1b shows the HY-VM introduced in [23], and Fig. 1c depicts the BFW-VM introduced in [26]. The FW- and BFW-VMs are driven by a pair of phase-shifted AC voltage sources $v_{in1} = V_{in}\sin(\omega t)$ and $v_{in2} = V_{in}\sin(\omega t - \pi)$, commonly obtained by using a CTT, while the HY-VM is driven by an input AC voltage source $v_{in} = V_{in}\sin(\omega t)$. The m-stage FW-VM consists of two oscillating columns of capacitors, one smoothing column of capacitors $(C_1, ..., C_m)$, and two stacks of diodes. The m-stage HY-VM includes a diode bridge with a smoothing capacitor C_0 and a p-stage FW-VM, with $p+1 = m$. The BFW-VM consists of a connected p-stage positive and n-stage negative FW-VMs, with $p + n = m$.

In steady-state operation, the capacitors of the smoothing column are charged in parallel by the oscillating columns and discharged in series through the load, twice every input voltage cycle. For the sake of simplicity, the load is considered as a constant current I_L. The total output voltage V_L is the sum of the output voltages of the capacitors in the smoothing column. Given that the load, in the BFW-VM, is connected between the positive and negative output terminals, the total output voltage of the BFW-VM is the sum of the output voltages of the positive and negative FW bridges, V_p and V_n, respectively. For simplicity, it is assumed that the capacitance of each capacitor is equal to C [9]–[27]. It can be noted that, thanks to the additional oscillating column, the output voltage of the symmetrical VMs presents an half-wave symmetry. Therefore, the analysis can be limited to the half period $T/2$; $f = 1/T = \omega/2\pi$ is the AC voltage frequency.

At no load, with $I_L = 0$, each capacitor of the smoothing column will charge up to the maximum value of the input voltage: $2V_{in}$ for the FW- and BFW-VMs, and V_{in} for the HY-VM. Thus, the total output voltage of the analyzed VMs is:

$$\begin{aligned} V_{L,FW} &= 2mV_{in} \\ V_{L,HY} &= (p+1)V_{in} = mV_{in} \\ V_{L,BFW} &= 2(p+n)V_{in} = 2mV_{in} \end{aligned} \quad . \tag{1}$$

In the presence of a load current (i.e., $I_L > 0$), a voltage ripple $\hat{V}_L$ and drop ΔV_L will occur across the capacitors of the oscillating columns and, consequently, across the capacitors of the smoothing column. The voltage drop across diodes is considered negligible in this analysis, as frequently done in literature [9]–[27].

The output voltage ripple $\hat{V}_L$ and drop ΔV_L of the analyzed VMs can be determined by finding the sum of the individual voltage ripples and drops of each smoothing column capacitor, resulting in:

$$\begin{aligned} \hat{V}_{L,FW} &= \frac{q}{C}m \\ \hat{V}_{L,HY} &= \frac{q}{C}(p+1) = \frac{q}{C}m \\ \hat{V}_{L,BFW} &= \frac{q}{C}(p+n) = \frac{q}{C}m \end{aligned} \quad , \tag{2}$$

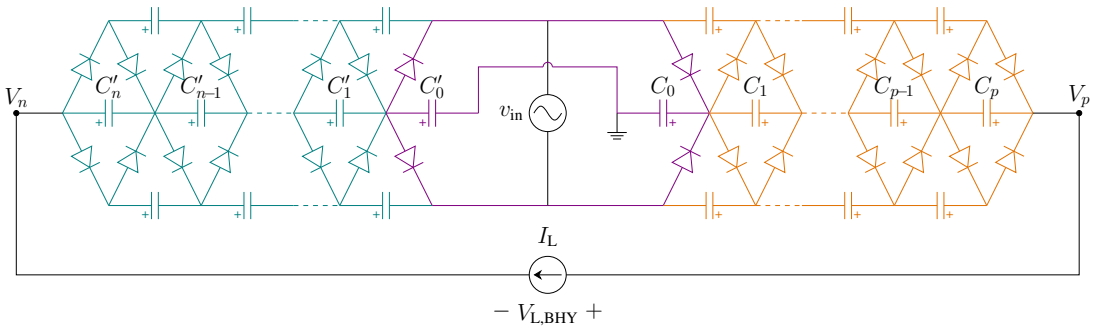


Fig. 2: m-stage BHY-VM: p-stage positive FW-VM in orange, n-stage negative FW-VM in teal, and shared diode bridge in violet; $p+n+1=m$.

$$\begin{aligned}\Delta V_{\text{L,FW}} &= \frac{q}{C}\left(\frac{m^3}{3}+\frac{m^2}{2}+\frac{m}{6}\right)\\ \Delta V_{\text{L,HY}} &= \frac{q}{C}\left(\frac{m^3}{3}-\frac{m^2}{2}+\frac{m}{6}\right)\\ \Delta V_{\text{L,BFW}} &= \frac{q}{C}\left(\frac{p^3+n^3}{3}+\frac{p^2+n^2}{2}+\frac{p+n}{6}\right)\end{aligned}\quad , \tag{3}$$

where $q = I_{\text{L}}/(2f)$ is the charge transferred to the load within half a period $T/2$ [9]–[27]. If $p=n=m/2$, the BFW-VM output voltage ripple does not change, while the drop simplifies in:

$$\Delta V_{\text{L,BFW}} = \frac{q}{C}\left(\frac{m^3}{12}+\frac{m^2}{4}+\frac{m}{6}\right)\ \Big|\ p=n=\frac{m}{2}\ . \tag{4}$$

The average output voltage $\overline{V}_{\text{L}}$ of the described VMs is calculated in Section IV.

III. Analysis of the Proposed BHY-VM

The proposed m-stage BHY-VM is shown in Fig. 2; it consists of a p-stage positive FW-VM in orange, a n-stage negative FW-VM in teal, and a shared diode bridge in violet, where $p+n+1=m$. Since simply connecting a positive and a negative HY-VM would short-circuit the source, the proposed topology is designed so that the diode bridge is shared between the two bridges. Actually, the ground is needed for the sole purpose of defining the voltages V_p and V_n. Therefore, in the following, two separate diode-bridge smoothing capacitors C_0 and C'_0 are considered to maintain the symmetry. They are respectively added to the smoothing columns of the positive and negative FW-VMs. The two bridges are connected to the AC voltage source $v_{\text{in}} = V_{\text{in}}\sin(\omega t)$, and the load is connected between the positive and negative output terminals.

In steady-state operation, the capacitors of the smoothing column are charged in parallel by the oscillating columns and discharged in series through the load, twice every input voltage cycle. Consequently, the output voltages of the positive and negative bridges V_p and V_n are the sum of the voltages of the capacitors in the respective smoothing columns. The total output voltage V_{L} of the BHY-VM is the sum of the output voltages of the two bridges.

The key steady-state waveforms of the BHY-VM are depicted in Fig. 3. Also in this case half-wave symmetry applies. At no load, with $I_{\text{L}} = 0$, each capacitor of the smoothing column

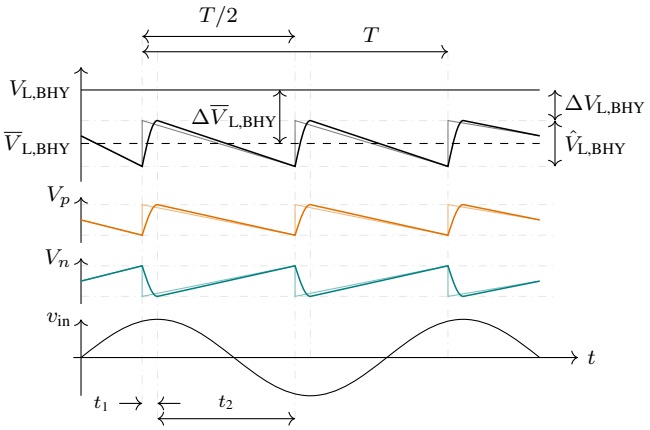


Fig. 3: Key steady-state waveforms of the BHY-VM.

will charge up to the maximum value of the input voltage V_{in}, except the two diode-bridge smoothing capacitors, which will charge up to $V_{\text{in}}/2$. Thus, the total output voltage of the BHY-VM at no load is:

$$V_{\text{L,BHY}} = (p+n+1)V_{\text{in}} = mV_{\text{in}}\ . \tag{5}$$

If load current $I_{\text{L}} > 0$, two main time intervals within half a period $T/2$ can be distinguished:

- t_1 – the smoothing column capacitors are charged by the upper oscillating column;
- t_2 – the smoothing column capacitors are discharged through the load.

As frequently done in literature, to analyze the VM circuits it can be assumed that the time interval $t_1 \ll T$ [9]–[27]. Therefore, the charging process t_1 is considered instantaneous and the discharging process lasts $t_2 = T/2$. This allows the portion of charge supplied to the load during the charging interval t_1 to be neglected, and consider the load supplied only during interval t_2. The key steady state waveforms modified according to this approach are shown in mild colors in Fig. 3.

The on-load output voltage will be less than $V_{\text{L,BHY}}$, due to output voltage ripple and drop, as visible in Fig. 3. To estimate the on-load average output voltage of the BHY-VM $\overline{V}_{\text{L,BHY}}$, it is necessary to compute the output voltage ripple $\hat{V}_{\text{L,BHY}}$ and drop $\Delta V_{\text{L,BHY}}$.

A. Output Voltage Ripple

The output voltage ripple of the BHY-VM $\hat{V}_{\text{L,BHY}}$, is the sum of the output voltage ripples of the positive and negative bridges, $\hat{V}_p$ and $\hat{V}_n$, respectively. These ripples are produced due to the periodic charging and discharging of the smoothing column capacitors.

Assuming that a charge q is transferred to the load by each capacitor of the smoothing column of both bridges in time t_2, the peak-to-peak ripple produced across each smoothing column capacitor is q/C. The output voltage ripple of the positive and negative bridge can be obtained by summing the individual voltage ripples of each smoothing column capacitor as:

$$\begin{aligned} \hat{V}_p &= q\sum_{i=0}^{p}\frac{1}{C_i} = \frac{q}{C}(p+1) \\ \hat{V}_n &= q\sum_{i=0}^{n}\frac{1}{C'_i} = \frac{q}{C}(n+1) \end{aligned} . \tag{6}$$

The total output voltage ripple can be determined from (6) by summing $\hat{V}_p$ and $\hat{V}_n$, as:

$$\hat{V}_{\text{L,BHY}} = \frac{q}{C}(p+n+2) = \frac{q}{C}(m+1) \ . \tag{7}$$

If a shared diode bridge with a total smoothing capacity equal to all the other FW-VM stages is considered, thus $C_0 = C'_0 = 2C$, (6) and (7) are modified as follows:

$$\begin{aligned} \hat{V}_p &= \frac{q}{C}p + \frac{q}{2C} = \frac{q}{C}\left(p+\frac{1}{2}\right) \\ \hat{V}_n &= \frac{q}{C}n + \frac{q}{2C} = \frac{q}{C}\left(n+\frac{1}{2}\right) \end{aligned} , \tag{8}$$

$$\hat{V}_{\text{L,BHY}} = \frac{q}{C}(p+n+1) = \frac{q}{C}m \ \Big| \ C_0 = C'_0 = 2C \ , \tag{9}$$

and corresponds to the result that is obtained by considering only a diode-bridge smoothing capacitor $C_0 = C$, without C'_0, or vice versa:

$$\begin{aligned} \hat{V}_p &= \frac{q}{C}(p+1) \\ \hat{V}_n &= \frac{q}{C}n \end{aligned} , \tag{10}$$

$$\hat{V}_{\text{L,BHY}} = \frac{q}{C}(p+n+1) = \frac{q}{C}m \ \Big| \ C_0 = C \text{ w/o } C'_0 \ . \tag{11}$$

B. Output Voltage Drop

The total output voltage drop of the BHY-VM $\Delta V_{\text{L,BHY}}$ is the sum of the output voltage drops of the positive and negative bridges, ΔV_p and ΔV_n, respectively. These drops can be determined by finding the sum of the individual voltage drops of the capacitors of each smoothing column.

The voltage drops of the positive and negative bridges are obtained from (3) by considering the BHY-VM bridges as two HY bridges with a number of stages equal to $p+1$ and $n+1$, respectively:

$$\begin{aligned} \Delta V_p &= \frac{q}{C}\left[\frac{(p+1)^3}{3} - \frac{(p+1)^2}{2} + \frac{p+1}{6}\right] \\ \Delta V_n &= \frac{q}{C}\left[\frac{(n+1)^3}{3} - \frac{(n+1)^2}{2} + \frac{n+1}{6}\right] \end{aligned} . \tag{12}$$

The voltage drops of the diode-bridge smoothing capacitors C_0 and C'_0 are zero because of the absence of oscillating capacitors at the first stage. Consequently, (12) is obtained also by considering each BHY-VM bridge as a FW bridge with p and n stages, respectively:

$$\begin{aligned} \Delta V_p &= \frac{q}{C}\left(\frac{p^3}{3} + \frac{p^2}{2} + \frac{p}{6}\right) \\ \Delta V_n &= \frac{q}{C}\left(\frac{n^3}{3} + \frac{n^2}{2} + \frac{n}{6}\right) \end{aligned} . \tag{13}$$

The total output voltage drop of the BHY-VM can be determined from (13) as the sum of ΔV_p and ΔV_n:

$$\Delta V_{\text{L,BHY}} = \frac{q}{C}\left(\frac{p^3+n^3}{3} + \frac{p^2+n^2}{2} + \frac{p+n}{6}\right) \ , \tag{14}$$

which corresponds to $\Delta V_{\text{L,BFW}}$ in (3). If $p = n = (m-1)/2$, the BHY-VM output voltage drop simplifies in:

$$\Delta V_{\text{L,BHY}} = \frac{q}{C}\left(\frac{m^3}{12} - \frac{m}{12}\right) \ \Big| \ p = n = \frac{m-1}{2} \ . \tag{15}$$

It can be noted that if $C_0 = C'_0 = 2C$, or if $C_0 = C$ without C'_0, the output voltage drop of the BHY-VM does not change because $\Delta V_{C_0} = \Delta V_{C'_0} = 0$.

IV. Average Output Voltage Calculation

The average output voltage $\overline{V}_{\text{L}}$ of the VMs introduced in Section II can be determined from (1)-(4), as $\overline{V}_{\text{L}} = V_{\text{L}} - \Delta\overline{V}_{\text{L}}$, where $\Delta\overline{V}_{\text{L}} = (\Delta V_{\text{L}} + \hat{V}_{\text{L}}/2)$ is the average output voltage drop [9]–[27]:

$$\overline{V}_{\text{L,FW}} = 2mV_{\text{in}} - \frac{q}{C}\left(\frac{m^3}{3} + \frac{m^2}{2} + \frac{2m}{3}\right) \ , \tag{16}$$

$$\overline{V}_{\text{L,HY}} = mV_{\text{in}} - \frac{q}{C}\left(\frac{m^3}{3} - \frac{m^2}{2} + \frac{2m}{3}\right) \ , \tag{17}$$

$$\overline{V}_{\text{L,BFW}} = 2mV_{\text{in}} - \frac{q}{C}\left[\frac{p^3+n^3}{3} + \frac{p^2+n^2}{2} + \frac{2(p+n)}{3}\right], \tag{18}$$

$$\overline{V}_{\text{L,BFW}} = 2mV_{\text{in}} - \frac{q}{C}\left(\frac{m^3}{12} + \frac{m^2}{4} + \frac{2m}{3}\right) \ \Big| \ p = n = \frac{m}{2} \ . \tag{19}$$

Similarly, the average output voltage of the BHY-VM can be calculated from (5), (7), (14), and (15) as:

$$\overline{V}_{\text{L,BHY}} = mV_{\text{in}} - \frac{q}{C}\left[\frac{p^3+n^3}{3} + \frac{p^2+n^2}{2} + \frac{2(p+n)}{3} + 1\right], \tag{20}$$

$$\overline{V}_{\text{L,BHY}} = mV_{\text{in}} - \frac{q}{C}\left(\frac{m^3}{12} + \frac{5m}{12} + \frac{1}{2}\right) \ \Big| \ p = n = \frac{m-1}{2} \ . \tag{21}$$

If $C_0 = C'_0 = 2C$, or if $C_0 = C$ without C'_0, (20) and (21) turn out to be:

$$\overline{V}_{\text{L,BHY}} = mV_{\text{in}} - \frac{q}{C}\left[\frac{p^3+n^3}{3} + \frac{p^2+n^2}{2} + \frac{2(p+n)}{3} + \frac{1}{2}\right], \tag{22}$$

$$\overline{V}_{\text{L,BHY}} = mV_{\text{in}} - \frac{q}{C}\left(\frac{m^3}{12} + \frac{5m}{12}\right) \ \Big| \ p = n = \frac{m-1}{2} \ . \tag{23}$$

TABLE I: Absolute error ε_A and relative error ε_R in % between numerical results and analytical prediction of the normalized average output voltage drop $\Delta\overline{N}_{L,BHY}$ of the BHY-VM with m from 1 to 10.

Equation	m	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
(20) (21)	ε_A	0.0122	0.0593	0.0985	0.226	0.343	0.529	0.712	0.920	1.18	1.39
	ε_R	2.45%	4.74%	4.93%	5.32%	5.27%	4.70%	4.45%	3.79%	3.62%	3.07%
(22) (23)	ε_A	0.00300	0.0391	0.0606	0.190	0.278	0.451	0.609	0.801	1.03	1.23
$C_0=C_0'=2C$	ε_R	1.18%	3.91%	3.46%	4.75%	4.45%	4.10%	3.86%	3.34%	3.19%	2.73%
(22) (23)	ε_A	0.00300	0.0391	0.0625	0.190	0.280	0.449	0.600	0.802	1.03	1.23
$C_0=C$ w/o C_0'	ε_R	1.18%	3.91%	3.57%	4.75%	4.48%	4.08%	3.81%	3.34%	3.19%	2.73%

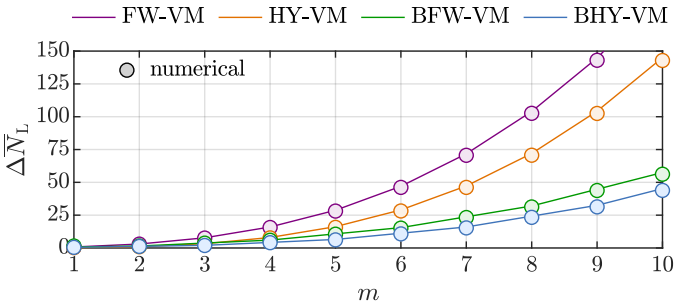


Fig. 4: Numerical validation of the normalized average output voltage drop $\Delta\overline{N}_L$ of the analyzed VMs as a function of the total number of stages m.

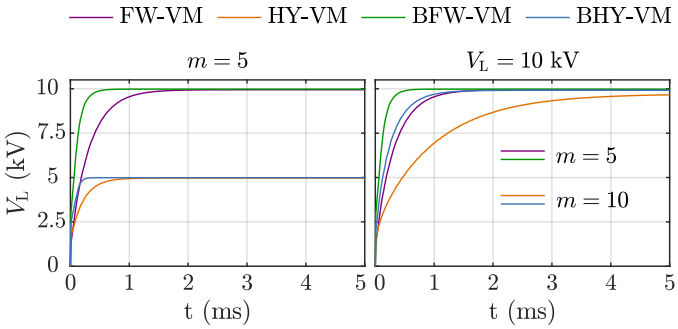


Fig. 5: Dynamic response of the analyzed VMs for $m=5$ (left) and with $V_L=10$ kV (right).

V. Numerical Validation and Comparison

The FW-, HY-, and BFW-VMs of Fig. 1, and the BHY-VM of Fig. 2 are simulated on PLECS (Plexim GmbH) environment, considering an input voltage V_{in} of 1 kV, a switching frequency f of 50 kHz, a load current I_L of 0.1 A, and a capacitance value C of 1 μF. Diodes with an on-resistance of 10 mΩ are considered in the simulations. For simplicity, it is assumed $p \geq n$, i.e., when m is even, the additional stage is placed in the positive bridge.

A. Average Output Voltage Drop

Fig. 4 shows the normalized average output voltage drop:

$$\Delta\overline{N}_L = \frac{C}{q}\Delta\overline{V}_L = -\frac{C}{q}(\overline{V}_L - V_L)\ , \tag{24}$$

of the described VMs as a function of the total number of stages m. Considering the same charge transferred to the load q and capacitance value C, the normalized average output voltage drop $\Delta\overline{N}_L$ is representative of the whole average output voltage drop $\Delta\overline{V}_L$. It can be noticed that the BHY-VM turns out to have better output voltage regulation, i.e., less load-dependent voltage drop with respect to the other topologies. As visible, numerical results (circles) fairly match the analytical predictions (solid traces).

Moreover, the absolute error ε_A and relative error ε_R between numerical results and analytical prediction of the normalized average output voltage drop $\Delta\overline{N}_{L,BHY}$ of the BHY-VM is computed and listed in Table I. As the number of stages m increases, ε_A increases. This is because the number of diodes in the VM increases, as well as the total voltage drop across them. A constant current is assumed, thus a constant voltage drop across diodes. Therefore, it can be observed as a general trend that ε_R decreases as the output voltage increases. In fact, by increasing the number of stages, the assumption of neglecting the diode voltage drop acquires validity. Although the voltage drop across diodes is not taken into account in the analysis, ε_R is anyway lower than 5%, especially for high m values, therefore validating (20)-(23).

B. Dynamic Response

Fig. 5 shows the dynamic response in time of the analyzed VMs for $m=5$ (left) and $V_L=10$ kV (right). These values have been chosen to be representative of all the other possible cases. Considering the same number of stages, i.e., Fig. 5 (left), the FW- and BFW-VMs have twice the output voltage of hybrid topologies, as anticipated in (1) and (5). However, it must be considered that full-wave topologies are fed by two AC voltage sources, thus by a total of 2 kV. It can be verified that bipolar topologies, and in particular the proposed BHY-VM, have a faster dynamic response. Furthermore, considering the same output voltage level, i.e., Fig. 5 (right), the BHY-VM has great dynamic performance despite having twice the number of stages.

C. Voltage Gain

The voltage gain $\overline{V}_L/V_{in}$ of the described VMs can be determined from (16), (17), (18), and (20) by considering the load $I_L=\overline{V}_L/R_L$, as:

$$\frac{\overline{V}_L}{V_{in,tot}} = \frac{m}{1+\dfrac{\Delta\overline{N}_L}{2fCR_L}}\ , \tag{25}$$

where, to ensure comparability, $V_{in,tot}$ is the total input voltage; $V_{in,tot}=2V_{in}$ for the full-wave topologies. It is worth noting that, besides for a scaling factor, the inverse of the voltage gain (25) is qualitatively represented in Fig. 4.

TABLE II: VMs component count.

Topology	CTT	n_D	n_C	Notes
FW-VM	✓	$4m$	$3m$	-
HY-VM	✗	$4m$	$3m-2$	-
BFW-VM	✓	$4m$	$3m$	-
BHY-VM	✗	$4m$	$3m-1$	$C_0 = C_0'$
			$3m-2$	$C_0 = C$ w/o C_0'

D. Component Count and Voltage Rating

Table II shows the component count of the considered VM circuits. Considering the same total number of stages m, the number of required diodes n_D is the same in all topologies. On the other hand, the number of required capacitors n_C is lower for the HY- and BHY-VMs. Furthermore, as mentioned above, they do not require the CTT.

The voltage rating of all diodes and capacitors of the HY- and BHY-VMs is $V_{in} = V_L/m$. Considering that full-wave topologies are fed by two AC voltage sources, thus by a total of $2V_{in}$, the voltage rating of all diodes and capacitors of the FW- and BFW-VMs is $2V_{in} = V_L/m$, except the first two (for the FW-VM) and four (for the BFW-VM) oscillating capacitors which is $V_{in} = V_L/2m$.

VI. Conclusion

A BHY-VM has been proposed for DC high-voltage power supplies. The circuit topology, operation, and steady-state analysis have been described. The proposed topology combines the advantages of the most popular symmetrical VMs. It has a smaller and better-regulated output voltage drop, faster dynamic response, and it does not require the CTT, reducing the complexity of the system, the harmonic generation, and the component count. Moreover, due to the bipolar nature, the high-voltage isolation requirements are reduced. The feasibility of the proposed BHY-VM has been numerically validated, and the performance of the proposed BHY-VM with respect to the common symmetrical VMs has been verified.

Future works can include the voltage drop across diodes in the analytical developments and the experimental validation of the proposed topology.

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