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Reliability improvement based on optimized modulations and rotating shedding frequency in modular DAB EV chargers

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ABSTRACT

Modular dual-active-bridge (DAB) converter is widely used for fast electric vehicle (EV) charging due to galvanic isolation and high power processing capability. However, the increasing high power demand for EV chargers introduces new challenges in ensuring the high reliability of power conversion systems. Various modulation techniques for DAB, such as single-phase-shift (SPS), extended-phase-shift (EPS), and dual-phase-shift (DPS), have been proposed, while the combined impact of these techniques and power sharing strategies on reliability remains underexplored. Therefore, this paper presents a comparative reliability evaluation of SPS, EPS, and DPS under the optimization schemes of minimum backflow power and peak current, along with the power sharing strategies of even sharing and module shedding with and without rotation. The results show that appropriate combinations where DPS with minimum peak current under module shedding with a rotation strategy achieve the best balance between efficiency and reliability. Furthermore, the investigation of the trade-off between rotation frequency and system-level reliability shows that high-frequency rotation leads to excessive thermal cycling and reduces the lifetime, which provides a new guideline for optimizing module shedding for increased reliability performance.

KEYWORDS

Backflow power; Dual-active bridge; EV charging; Peak current; Power sharing strategy; Reliability

Electric vehicles (EVs) are rapidly increasing in support of the goal of decarbonization. In 2024, EV sales exceeded 17 million worldwide, rising by more than 25%, and they are expected to achieve more than 40% market share in overall car sales in 2030[1]. As the adoption of EVs continues to accelerate, fast and high-power EV supply equipment (EVSE) is demanded, which requires high-performance DC/DC converters and robust system power management strategies capable of high current and power levels. For reliability, fast EVSE typically employs modular configurations, as shown in Figure 1[2]. The dual-active-bridge (DAB) converter has gained significant attention for EV fast-charging applications due to its voltage step-up/-down, galvanic isolation, high-power processing capabilities, and modularity[3].

Single-phase-shift (SPS), extended-phase shift (EPS), and dual-phase-shift (DPS) are the main modulation techniques for DAB converters, which can control the output power and optimize the performance of the converter by adjusting the phase shift ratios[4–6]. SPS is the most traditional and straightforward modulation technique, and it can provide the highest power. However, the single control variable in SPS limits its flexibility, resulting in a high value of backflow power (BFP) and current stress, which can further negatively affect the system efficiency[5]. EPS and DPS introduce an additional degree of control freedom, enhancing the flexibility but also the control complexity. Therefore, the optimization schemes, minimum BFP and inductance peak current, have been proposed, analyzing the various phase shift ratio combinations to reduce the BFP or current stress to achieve enhanced performance[7–9]. These studies focus on efficiency improvements, with limited exploration of the reliability of power switching devices under different modulation techniques and optimization schemes.

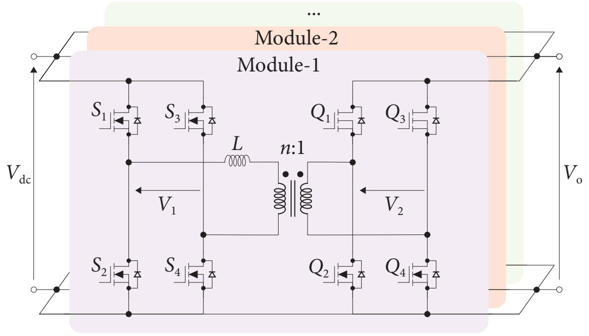

Figure 1 Architecture of modular DAB for EV charging.

In virtue of the specific requirements of EV charging application, EVSEs experience stochastic and time-varying loads according to the EV model, state-of-charge, and ambient temperature, which can cause power converter junction temperature fluctuations and suboptimal utilization[10]. Therefore, to optimize system reliability and efficiency, appropriate power-sharing strategies (PSSs) capable of allocating charging loads among EVSE modules are necessary.

The simplest PSS can be realized by evenly sharing the charging power across all modules simultaneously. However, this PSS tends to result in low efficiency under light-load conditions[11]. A common solution is to dynamically activate the optimal number of modules using a module-shedding approach based on the actual load conditions[12–14]. In the literature, conventional module shedding tends to prioritize the first modules, while high-order modules are utilized only during brief power peaks (e.g., low state-of-charge operations). In the long term, this results in an imbalanced distribution

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of loading and utilization among the modules, leading to uneven thermal stress, thus reducing system reliability[15,16]. To mitigate this issue, Alharbi et al.[11] proposed rotating phase shedding as an improved thermal management strategy. This demonstrates that rotating shedding can maintain a high efficiency identical to that of phase shedding control with rotation while balancing the thermal damage across all modules. However, the overall reliability performance at the system level still requires further research. Meanwhile, the rotating frequency is a critical parameter that has not yet been thoroughly analyzed. In fact, inappropriate values can lead to junction temperature periodic fluctuations, which negatively affect both reliability and overall efficiency[17].

In power electronic systems, thermal stress manifests through temperature cycling, characterized by temperature variations and average operating temperatures. These thermal dynamics necessitate a detailed analysis of device temperatures under real-world conditions and the development of strategies to manage them for enhanced reliability[18–20]. Notably, these temperature fluctuations are closely tied to operating conditions and environments, commonly referred to as mission profiles[21]. In high-power converters, power switching devices and DC-link capacitors are generally identified as critical and failure-prone components. However, the lifetime of DC-link capacitors is mainly determined by low-frequency thermal cycles dictated by the global mission profile and does not change appreciably with different modulations, while the influence of modulation techniques or power-sharing strategies on their stress is negligible. Therefore, this work focuses on switching devices, whose operating conditions are directly affected by the studied modulation techniques and power-sharing strategies[22].

Therefore, the main contributions are given as follows:

- A comprehensive analysis is conducted on EPS and DPS with minimum BFP and peak current schemes, covering all the operating modes and power ranges.
- The impact of different modulation techniques and power sharing strategies on the reliability performance of the modular DAB converter is evaluated, revealing the influence of the current stress and the thermal distribution across the parallel modules.
- The trade-off between the rotation frequency in module shedding power sharing strategies and system-level reliability is explored, showing how varying the rotation frequency affects thermal cycling and overall system damage.

The rest of the paper is organized as follows. Section 1 introduces the fundamental operating principles of SPS, EPS, and DPS, highlighting their performance across different operating conditions. Section 2 further analyzes the minimum BFP and peak current schemes and compares the resulting current stress and backflow power characteristics under each modulation technique. Section 3 presents the design of the modular DAB converter, detailing the system architecture and the thermal model. Based on this thermal model, the temperature swings of the switches are examined, and the junction temperature profiles over all operating conditions are compared. The mission profile generation procedure and the power sharing strategies are described in Section 4. Section 5 integrates all the above elements to perform a comparative reliability evaluation across modulation techniques, optimized schemes, and power sharing strategies and analyzes the trade-off between the power rotating frequency in modules and reliability using the mission profile established in Section 4. Section 6 provides an in-depth discussion of potential cost and future reliability enhancement methods. Finally, Section 7 summarizes the key findings and outlines possible directions for future research and development.

1 Modulation techniques of DAB

1.1 Single-phase shift

SPS is the simplest and most commonly used modulation technique for DAB converters[4]. The operational waveforms, including voltages on the primary V_1 and secondary sides V_2 of the transformer, leakage inductance current i_L, and transmission power P of the DAB under SPS for $V_1 \leqslant nV_2$ and $V_1 > nV_2$, are shown in Figure 2(a) and Figure 3(a), respectively. Under SPS, the outer phase shift ratio denoted as d between V_1 and V_2 is involved, which changes the voltage across the leakage inductor to control the transmission power and the power flow direction[9]. To simplify the analysis, the maximum power is used as the base value, which is defined as

$$P_{\max} = \frac{nV_1V_2}{8Lf}, \tag{1}$$

where L is the leakage inductance and f is the switching frequency equal to $1/T$. Therefore, the normalized power P_{in} equation under SPS is given in Table 1, and the transmission power is expressed as $P = P_{\text{in}}P_{\max}$.

SPS has a great attraction due to its high dynamic performance, ease of realizing soft switching, and high power processing capability, achieving good efficiency when V_1 and nV_2 are matched. However, when V_1/nV_2 deviates far from 1, the SPS modulation will result in a limited zero-voltage-switching (ZVS) range and circulating power[23]. The shaded regions in Figures 2(a) and 3(a) depict the BFP, which is sent back to the source. With high BFP, an increase in positive power is required to compensate for the losses, enhancing the current stress and significantly contributing to conduction loss and magnetic losses[9].

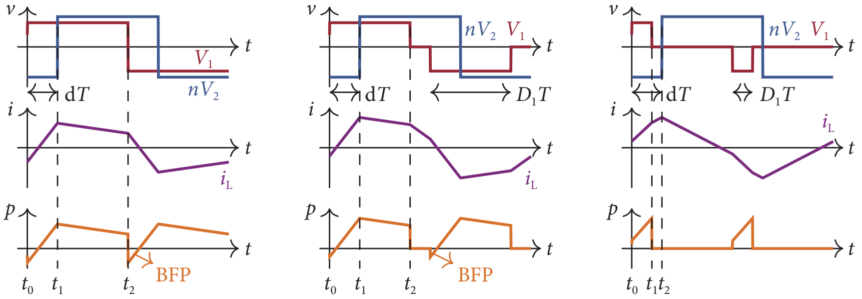
1.2 Extended phase shift

EPS introduces an additional inner phase shift ratio, denoted as D_1, between the two legs of the primary side, resulting in a three-level voltage waveform for V_1 instead of the two-level voltage of SPS[5]. This additional degree of freedom makes EPS more flexible to control, and various combinations of d and D_1 can achieve the same power conversion value. Two main modes of EPS, $D_1 \geqslant d$ and $D_1 < d$, are analyzed with the corresponding waveforms shown in Figures 2(b)–2(c) and Figures 3(b)–3(c). The power transfer equations under these two modes are given in Table 1. Full-range power can be achieved when $D_1 \geqslant d$, and when $D_1 < d$, the transmission power is limited to half of the full power[8].

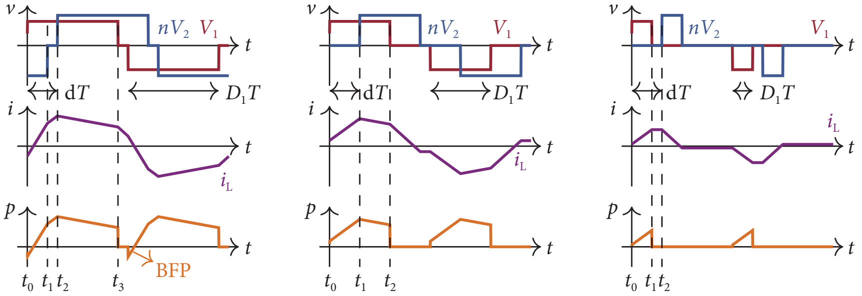
In contrast to SPS, EPS has the potential to reduce BFP. As shown in Figures 2(b) and 3(b), the presence of the 0-level voltage in V_1 shortens the duration of BFP occurrence, thus enabling a lower BFP. Furthermore, Figures 2(c) and 3(c) illustrate a mode where BFP is completely eliminated. However, this condition can lead to higher switching loss as a result of the non-ZVS condition of the switching devices.

1.3 Dual-phase shift

DPS is conceptually similar to EPS but applies the inner phase shift to both bridges. Consequently, both V_1 and V_2 exhibit three-level waveforms. The complex combinations of d and D_1 in DPS provide more flexible control advantages[6]. In this condition, the DPS is analyzed in three modes where $0.5 - d \leqslant D_1$, $d \leqslant D_1 \leqslant 0.5 - d$, and $D_1 < d$, as illustrated in Figures 2(d)–2(f) and Figures 3(d)–3(f). The power equation can be expressed in Table 1. The analysis in Ref. [6] indicates that full-range power is attainable when $0.5 - d \leqslant D_1$. In the mode where $d \leqslant D_1 \leqslant$

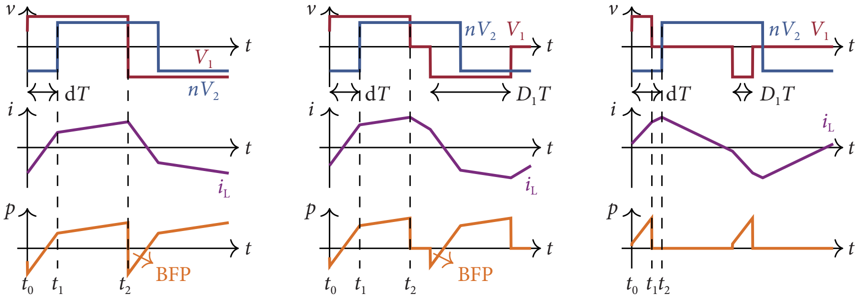


(a) SPS (b) EPS: $D_1 \geq d$ (c) EPS: $D_1 < d$

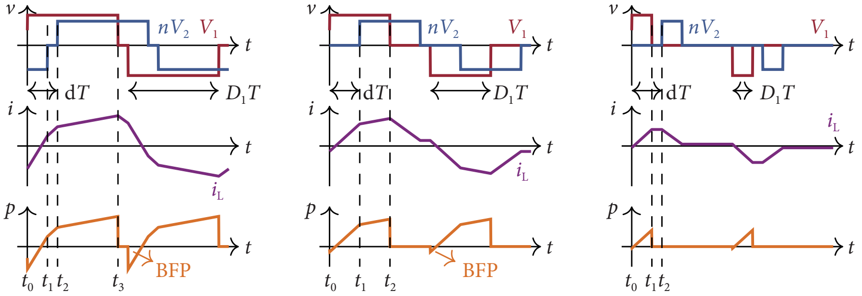


(d) DPS: $0.5-d \leq D_1$ (e) DPS: $d \leq D_1 \leq 0.5-d$ (f) DPS: $D_1 < d$

Figure 2 Operational waveforms when $V_1 \leqslant nV_2$ for (a) SPS, (b) mode 1 of EPS with $D_1 \geqslant d$, (c) mode 2 of EPS with $D_1 < d$, (d) mode 1 of DPS with $0.5 - d \leqslant D_1$, (e) mode 2 of DPS with $d \leqslant D_1 \leqslant 0.5 - d$, and (f) mode 3 of DPS with $D_1 < d$.



(a) SPS (b) EPS: $D_1 \geq d$ (c) EPS: $D_1 < d$



(d) DPS: $0.5-d \leq D_1$ (e) DPS: $d \leq D_1 \leq 0.5-d$ (f) DPS: $D_1 < d$

Figure 3 Operational waveforms when $V_1 > nV_2$ for (a) SPS, (b) mode 1 of EPS with $D_1 \geqslant d$, (c) mode 2 of EPS with $D_1 < d$, (d) mode 1 of DPS with $0.5 - d \leqslant D_1$, (e) mode 2 of DPS with $d \leqslant D_1 \leqslant 0.5 - d$, and (f) mode 3 of DPS with $D_1 < d$.

$0.5 - d$, the maximum power can reach up to two-thirds of the full power. When $D_1 < d$, only half of the full power can be delivered.

Similar to EPS, DPS solves the limits of SPS. The 0-level voltage in V_1 helps reduce the BFP. Meanwhile, the 0-level voltage in V_2 decreases the voltage across the leakage inductor during this interval, resulting in a lower peak current.

In fact, if $D_1 = 0.5$, the power expression of EPS and DPS reverts to the SPS modulation. In all cases, the inner and outer phase shift values are $0 \leqslant d \leqslant 0.25$, and $0 \leqslant D_1 \leqslant 0.5$.

2 Minimum backflow power and peak current

According to the above analysis, SPS involves only one degree of freedom, which makes it easy to determine the phase shift ratio based on the required power value. In contrast, EPS and DPS offer multiple combinations of d and D_1 for the same transmission power. To select an optimal solution for enhancing converter performance, the minimum backflow power and the minimum leakage inductance peak current based on the Lagrange multiplier algorithm are widely used[7,24]. The former aims to reduce the circulating power, while the latter focuses on minimizing the current stress

Table 1 Normalized expressions of input power, backflow power, peak current under SPS, EPS, and DPS

Description		P_{in}^{*}	$P_{\text{BFP}}^{\dagger}$	$I_{\text{Lp}}^{\ddagger}$
SPS		$8d(1-2d)$	$\frac{(4d+k-1)^2}{2k+2}$	$2k+8d-2,\ V_1>nV_2$ $-2k+8kd+2,\ V_1\leqslant nV_2$
EPS	$D_1\geqslant d$	$d(16D_1-16d)+D_1(4-8D_1)$	$\frac{(2kD_1+4d-1)^2}{2k+2}$	$8d+D_1(4k-8)+2, V_1>nV_2$ $4k(2d-D_1)+2, V_1\leqslant nV_2$
	$D_1<d$	$D_1(4-16d+8D_1)$	$\frac{(0.5kD_1-0.25+d)^2}{0.8k+0.8}$	$\frac{(0.5kD_1-0.25+d)^2}{0.8k+0.8}$
DPS	$0.5-d\leqslant D_1$	$d(8-16d)-8(0.5-D_1)^2$	$\frac{2(1-2d-kD_1-D_1)^2}{k+1}, i_L(t_1)\geqslant 0$ $\frac{2(k-1)^2D_1^2+2k(1-2D_1-2d)^2}{k}, i_L(t_1)<0$	$8d+D_1(4k-4), V_1>nV_2$ $8kd+D_1(4-4k), V_1\leqslant nV_2$
	$d\leqslant D_1\leqslant 0.5-d$	$d(16D_1-8d)$	$\frac{2(k-1)^2D_1^2}{k}, V_1>nV_2$ $0, V_1\leqslant nV_2$	$8d+D_1(4k-4), V_1>nV_2$ $8kd+D_1(4-4k), V_1\leqslant nV_2$
	$D_1<d$	$8D_1^2$	$\frac{2(k-1)^2D_1^2}{k}, V_1>nV_2$ $0, V_1\leqslant nV_2$	$D_1(4+4k)$

*Normalized input power; † Normalized backflow power; ‡ Normalized leakage inductance peak current.

on power devices. The Lagrangian function in this paper is given by the following:

$$\mathcal{L}(d, D_1, \lambda) = T(d, D_1) + \lambda[P(d, D_1) - P^*], \tag{2}$$

where $T(d, D_1)$ is the target function, which represents the formula for BFP or peak current. $P(d, D_1)$ refers to the transmission power, and the constraint condition is given by $P(d, D_1) = P^*$. λ is the Lagrange multiplier.

In this section, BFP and peak current for EPS and DPS modulations are analyzed across all possible operating modes, and the results after optimization are compared. With respect to the optimization of BFP, maintaining ZVS is the primary focus wherever possible to minimize switching losses. The detailed calculation results are provided in the Appendix.

2.1 Backflow power analysis

Under mode 1 of EPS, when the inductor current satisfies $i_L(t_0) < 0$ and $i_L(t_1) > 0$, the switching devices operate in the ZVS conditions. Similarly, for EPS mode 2, the case $i_L(t_0) < 0$ also occurs during low power. The corresponding BFP in these cases are listed in Table 1, where $k = V_1/nV_2$. By substituting these expressions into the power equation (2), the solutions for d and D_1 can be obtained. It is worth noting that under the constraints of d and D_1, these conditions do not cover the full range power. Therefore, the ZVS boundary where $i_L(t_0) = 0$ is considered, and the BFP is reduced to 0.

For DPS, the BFP for all modes are summarized in Table 1. In mode 1, when $i_L(t_0) \leqslant 0$ and $i_L(t_1) \geqslant 0$, ZVS is maintained, but this condition achieves only a portion of the full power. To enable a wider power range, scenarios with $i_L(t_1) < 0$ are considered. In mode 2, when $V_1 \leqslant nV_2$, $i_L(t_0)$ is always larger than 0, resulting in no BFP in this case. When $V_1 > nV_2$, $i_L(t_0) < 0$, and the corresponding BFP is shown in Table 1. For mode 3, its current behavior is similar to mode 2 and therefore is not discussed in detail.

2.2 Peak current analysis

Compared with BFP, the analysis of peak current is easier, and the results for various modulation cases are illustrated in Figures 2 and 3. For EPS mode 1, the peak current occurs at time t_1 when $V_1 \leqslant nV_2$ and occurs at t_2 when $V_1 > nV_2$. This indicates that two cases must be considered separately when determining the optimal solution of d and D_1. In EPS mode 2 with $D_1 < d$, the value of V_1/nV_2 does not affect the shape of the inductance current waveform, as shown in Figures 2(c) and 3(c). In this case, the peak current occurs consistently at t_2. All the corresponding equations of the peak current are provided in Table 1. For the current normalization, the maximum value of the peak current is used as the base value, which can be expressed as

$$I_{\max} = \frac{nV_2}{8Lf}. \tag{3}$$

For DPS, the peak current behavior in mode 1 and mode 2 is influenced by the relationship between V_1 and nV_2. As illustrated in Figures 2(d) and 3(d), the peak current occurs at t_2 when $V_1 \leqslant nV_2$ and at t_3 when $V_1 > nV_2$. Similarly, in mode 2, the peak current appears at t_1 and t_2 under the two respective voltage conditions, as shown in Figures 2(e) and 3(e), respectively. In mode 3, where $D_1 < d$, V_1 and nV_2 do not stress the inductor simultaneously. As a result, the voltage magnitude has no impact on the shape of the current waveform, and the peak current occurs at t_1 in both cases, as depicted in Figures 2(f) and 3(f). All corresponding expressions are summarized in Table 1.

2.3 Backflow power and peak current comparison

Based on the above analysis, Figure 4 shows the values of d and D_1 for EPS and DPS under different optimization schemes, along with a comparison with SPS, at voltage conversion ratios of $k = 0.5$, $k = 1$, and $k = 1.5$. For both EPS and DPS operating under the minimum BFP scheme, the modulation parameters tend to converge with those of SPS at high power levels. For EPS under the minimum peak current scheme, when $k = 0.5$ and $k = 1$, the optimized value yields $D_1 = 0.5$, which corresponds to SPS. Additionally, at $k = 1.5$, EPS coincides with SPS in the low-power region. This indicates that SPS offers significant advantages over EPS in reducing the current stress of components. For DPS under the minimum peak current scheme, the case of $k = 1$ also results in $D_1 = 0.5$, implying operation under SPS. For $k = 0.5$ and $k = 1.5$, the DPS gradually approaches the SPS condition as the power increases. Overall, these results show that SPS performs well under high-power operating conditions, effectively minimizing both backflow power and peak current.

To verify the effectiveness of the two optimization schemes, Figures 5 and 6 show the comparison of backflow power and peak current performance between EPS and DPS under these schemes, respectively, including the comparison with SPS. As depicted in Figure 5, EPS with the minimum BFP scheme can reduce the BFP to 0 within the low- to medium-power range. Although the BFP

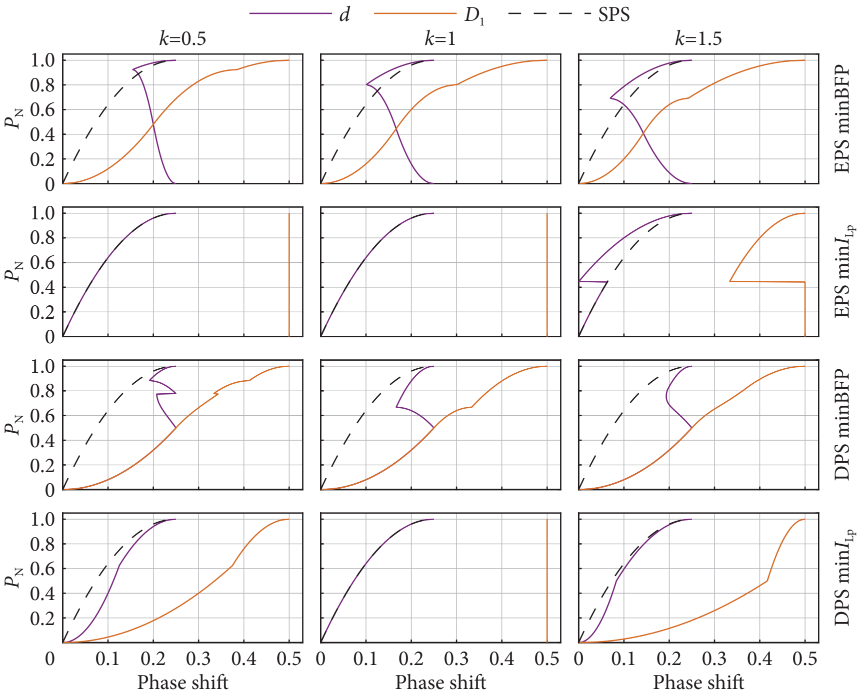


Figure 4 Relation curves of the normalized power with d and D_1.

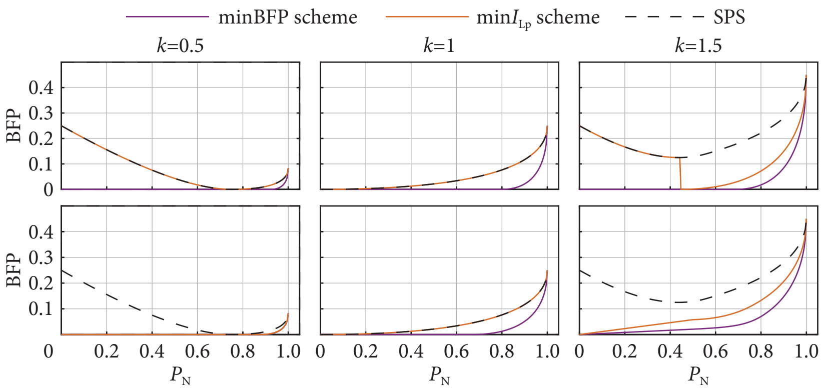


Figure 5 Comparison of backflow power value between EPS and DPS under minimum BFP scheme, minimum peak current scheme, and SPS, at voltage conversion ratios of $k = 0.5$ (left), $k = 1$ (middle), and $k = 1.5$ (right).

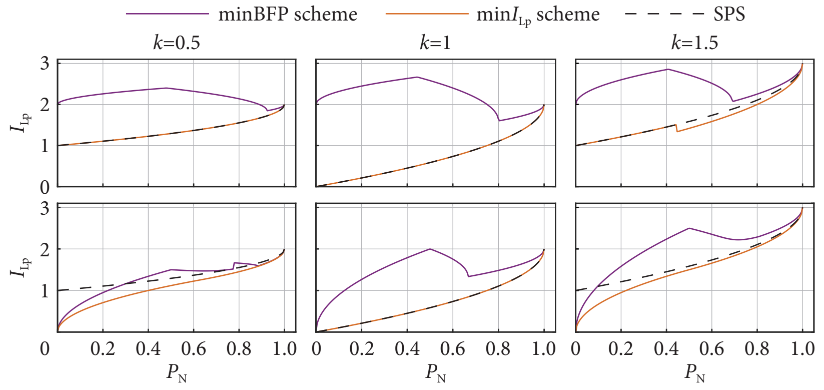


Figure 6 Comparison of leakage inductance peak current value between EPS and DPS under minimum BFP scheme, minimum peak current scheme, and SPS, at voltage conversion ratios of $k = 0.5$ (left), $k = 1$ (middle), and $k = 1.5$ (right).

value increases as the power rises, it remains lower than that of SPS and EPS with the minimum peak current scheme. For DPS at $k = 0.5$ and $k = 1$, the minimum BFP method has a similar performance to that of EPS, effectively minimizing the BFP across the entire power range. In the case of $k = 1.5$, the BFP remains larger than 0, but it is significantly lower than the SPS and DPS with the minimum peak current scheme. Overall, these results demonstrate that EPS provides superior BFP reduction performance in the range of full power and has a higher possibility of keeping the BFP at 0, although under various operating conditions.

In Figure 6, the EPS with the minimum peak current scheme has a comparable performance to SPS. In contrast, DPS achieves superior results by reducing the peak current. It can also be observed that although the minimum BFP scheme effectively minimizes the BFP, it causes a higher peak current stress, resulting in an increased switching loss of the power devices.

3 EV charging system design

3.1 EV charging system description

To handle the high power of the EV charging system, a modular architecture consisting of 10 DAB modules has been selected, as shown in Figure 1. Each module is rated 25 kW with a maximum output voltage of 500 V, resulting in a total system power P of 250 kW. In this work, Wolfspeed SiC MOSFETs E3M0032120J2 (1200 V, 74 A) and E4M0015075J2 (750 V, 156 A) are utilized on the primary and secondary sides, respectively. The operational parameters are shown in Table 2.

3.2 Thermal network design

A comprehensive analysis of the converter requires consideration of the cooling system design, as this defines the electrical and thermal behavior of the system. Regarding the switches, conduction and switching loss analysis is the critical procedure in the design of the thermal network. Currently, loss analysis is typically conducted using lookup-table (LUT) methods[25], which are performed in a PLECS (Plexim GmbH) environment across various operating conditions, including power levels from 0 to 25 kW, output voltages ranging from 50 to 600 V, and junction temperatures from −10 to 180 °C. These simulations generated five 3D LUTs to characterize losses for SPS, EPS, and DPS modulations with minimum BFP and peak current schemes.

The design of the cooling system is essential for the thermal network. In this design, the Cauer RC thermal network is employed, as shown in Figure 7. Each half-bridge is equipped with an individual heatsink. Therefore, the steady-state junction temperature of the switches is found as Ref. [17]:

$$T_j = P_{\text{loss}}\left(R_{\text{jc}} + R_{\text{ch}}\right) + 2P_{\text{loss}}R_{\text{ha}} + T_a \tag{4}$$

where T_j and P_{loss} are the junction temperature and power loss of a single switching device, respectively. R_{jc}, R_{ch} and R_{ha} represent the thermal resistances. T_a is the ambient temperature.

Regarding the thermal network, the values of junction-to-case thermal impedance (Z_{jc}) can be derived from the datasheets[26,27], which are shown in Table 3. The thermal interface material resistance R_{ch} is evaluated at a value of 0.0482 K/W, which depends on the specific device dimensions and materials. In this analysis, the DAB converter exhibits different loss performances under all the modulation techniques analyzed above. To ensure the thermal safety of the switching devices under the worst-case scenarios, various heatsink-to-ambient thermal resistances R_{ha} are designed specifically for SPS, EPS, and DPS. According to the LUTs, the maximum loss of switching devices at the 120 °C junction temperature is used as a reference for designing R_{ha} under an ambient temperature of 40 °C. Using Eq. (4), the required Rha values are calculated. The Rha results and the selected heatsink-to-ambient thermal capacitance value are summarized in Table 4.

3.3 Thermal performance comparison

Figure 8 illustrates the current and junction temperature of switches S1 and S3 on the primary side under an operating point of 500 V output voltage, 20 kW output power, and 25 °C ambient temperature. From the current waveforms, it can be observed that EPS and DPS with the minimum BFP scheme achieve zero backflow power at the expense of significantly increased peak current, resulting in much higher current stress on the switches. In the DPS minimum BFP case, S1 even loses ZVS, which leads to additional switching losses. Therefore, both EPS and DPS under the minimum BFP scheme exhibit higher average junction tempera-

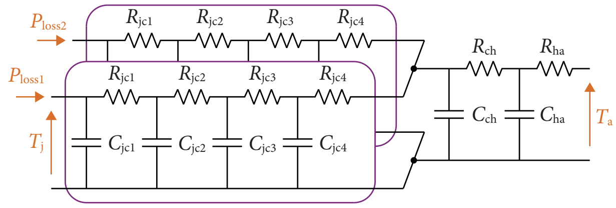


Figure 7 Cauer thermal network for one half-bridge. Junction-to-case thermal impedance are modeled as a four-layer RC network[26–27]. P_{loss1} and P_{loss2} represent the losses for two switches. C_{jc}, C_{ch} and C_{ha} represent the thermal capacitances of the junction-to-case, case-to-heatsink, and heatsink-to-ambient, respectively. R_{jc}, R_{ch} and R_{ha} represent the thermal resistances of the junction-to-case, case-to-heatsink, and heatsink-to-ambient, respectively.

Table 2 Main working parameters

Description	Symbol	Value	Unit
Input voltage	V_{dc}	800	V
Maximum output voltage	V_{omax}	500	V
Maximum power per DAB	P_{max1}	25.0	kW
Total power	P_{max}	250	kW
Switching frequency	f	50	kHz
Inductance value	L	57.2	μH
Transformer ratio	$n : 1$	2 : 1	/
Module number	N	10	/

Table 3 Thermal parameters from junction to case

Side	Z_{jc}	Cauer thermal model				Unit
Primary	R_{jc}	38.5	111	62.8	47.6	mK/W
	C_{jc}	2.41	12.0	46.5	50.4	mJ/K
Secondary	R_{jc}	13.8	28.5	135	164	mK/W
	C_{jc}	0.59	2.87	6.69	55.6	mJ/K

Table 4 Thermal parameters from heatsink to ambient

Symbol	SPS	EPS		DPS		Unit
		minBFP	min I_{Lp}	minBFP	min I_{Lp}	
R_{ha}	393	70.5	382	233	466	mK/W
C_{ha}	5.35	5.35	5.35	5.35	5.35	mJ/K

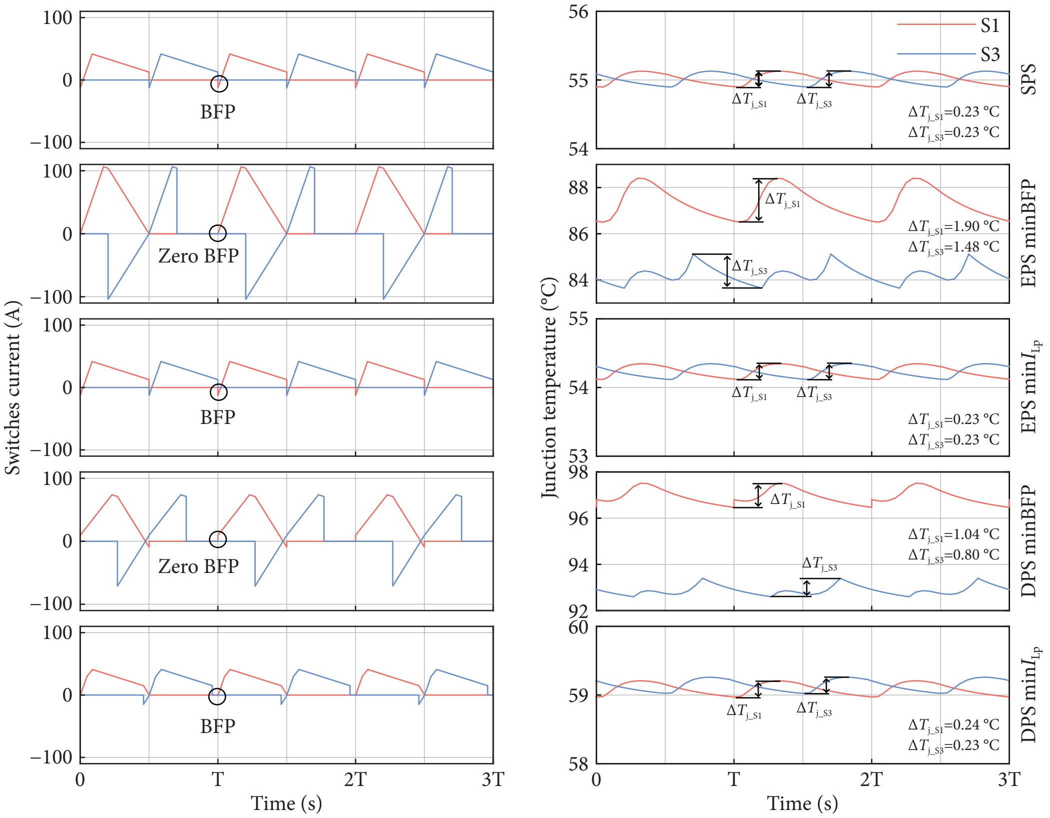


Figure 8 Current (left) and junction temperature (right) waveform of S1 and S3 in one DAB module with different modulation techniques and optimized schemes. The operating condition is 500 V output voltage, 20 kW output power, and 25 °C ambient temperature.

tures and larger temperature swings within each period. Moreover, due to the presence of the inner phase shift, the current waveforms of S1 and S3 are different, which leads to unequal device losses and consequently an imbalanced temperature distribution in the same module.

According to the theoretical analysis in Figure 4, when the voltage conversion ratio $k < 1$, the EPS with the minimum peak current scheme comes to the same operating mode as SPS and therefore shows identical current waveforms. In general, the minimum peak current scheme exhibits a much lower current stress than the minimum BFP scheme, although they introduce a certain amount of backflow power. From the device-level perspective, this scheme leads to a lower average junction temperature and a more balanced thermal distribution between S1 and S3, which is beneficial for improving the device lifetime.

3.4 Thermal performance comparison

Under an ambient temperature of 25 °C, Figure 9 illustrates the junction temperature performance of a single DAB converter operating under 0–25 kW and 300–500 V conditions based on the designed thermal model. The maximum current is limited to 62.5 A, with any excess disregarded. For SPS, the absence of an inner phase shift results in identical junction temperature behavior for S_1–S_4 and Q_1–Q_4. The junction temperature gradient varies significantly with power. In the case of EPS, the inner phase shift ratio is applied to the primary side, generating circulating current with the pairs of switches (S_1 and S_3, S_2 and S_4) that result in different current waveforms and losses. Consequently, S_1–S_2 and S_3-S_4 should exhibit distinct junction temperature profiles. For the EPS with the minimum BFP scheme, the devices show a higher proportion of elevated temperatures, particularly under high-voltage conditions. Conversely, EPS with the minimum peak current scheme exhibits a similar thermal behavior to that of SPS, as analyzed in Figure 4. In the DPS, the inner phase shift ratio is applied to both the primary and secondary sides, causing distinct junction temperature patterns across all four legs of the DAB converter.

According to the analysis in Figure 6, the minimum BFP scheme leads to increased peak current stress on the switches. This higher current stress significantly elevates the junction temperature, as shown in Figure 9, which has a negative impact on the switch lifetime. On the other hand, the minimum peak current scheme maintains a lower junction temperature by mitigating the current stress, particularly under low-to-medium power conditions, which results in superior thermal performance and potentially enhances the system reliability.

4 Mission profiles and power sharing strategies

4.1 Mission profile generation

To evaluate the reliability of the modular DAB converter in practical charging applications, a one-year mission profile based on the real charging data from 25 EVs has been generated, as shown in Figure 10 (data source: https://www.fastnedcharging.com/en/brands-overview). The profile is created in a randomized way and considers arrival and departure times from the city center scenario discussed in Ref. [28] and the initial state of charge from Ref. [29]. Every day accounts for approximately 12 charging events on average. Additionally, the ambient temperature profile is generated by considering historical data, including mean average, mean maximum, and mean minimum temperatures ranging from 1991–2020 in the city of Bologna (the same city examined in Refs. [28–29]). Mission profile data are generated with a temporal reso-

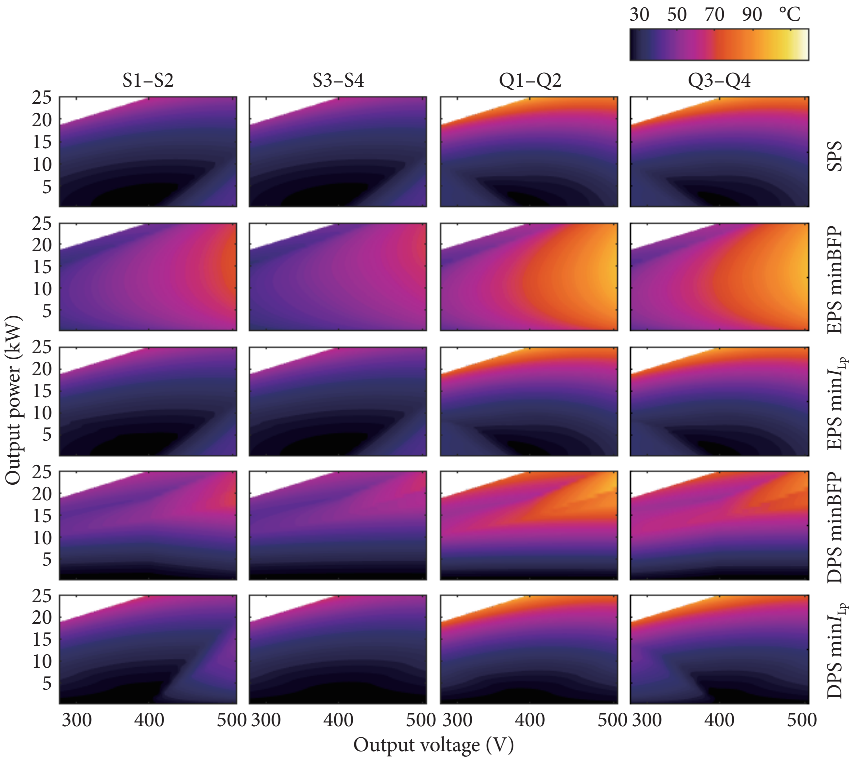


Figure 9 Junction temperature color map of switching devices with the function of output power and voltage under 25 °C ambient temperature.

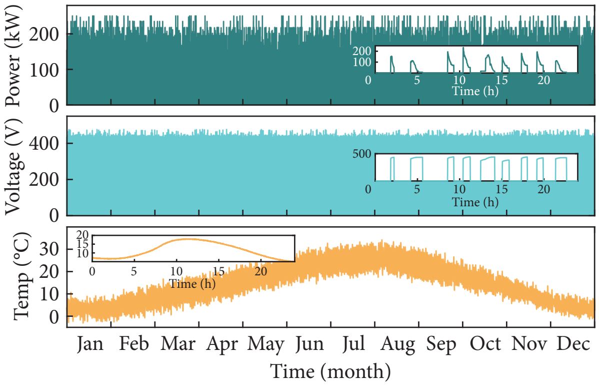


Figure 10 One-year mission profile output power (top), output voltage (middle), and ambient temperature in Bologna (bottom). Zoom frames show one-day time span.

lution of 1 minute.

As illustrated by the one-day load profiles in Figure 10, the charging power profile exhibits significant fluctuations throughout the day, while the charging voltage varies approximately 400 V. The ambient temperature ranges from approximately –4 to 34 °C.

4.2 Power sharing strategies

For the modular DAB converters illustrated in Figure 1, various power-sharing strategies are suited to different applications when addressing the dynamic high-voltage and high-power demands of a year-long mission profile. These strategies have varying impacts on the efficiency and reliability of the system. To comprehensively evaluate the reliability performance of SPS, EPS, and DPS with minimum BFP and peak current schemes, a comparative analysis was conducted under three types of PSS, including even sharing, efficiency-oriented module shedding, and shedding with rotation[11,12]. To identify the load switching points for various modulations and schemes, the junction temperature performance of a single DAB module assumed to operate at 400 V is analyzed using the thermal data shown in Figure 9; thus, the losses are calculated based on the LUTs. From the loss evaluation, the efficiency performance of the modular configuration is derived, which determines the reference switching points for module shedding. The detailed explanation is as follows:

- PSS T1: The load is evenly shared among the 10 DAB modules regardless of the power level; thus, all the modules share the same average powers and active times.
- PSS T2: The load is split and sequentially allocated among the DAB modules following efficiency-oriented module shedding based on the performance of each modulation technique and optimization scheme. The varying power loss characteristics cause different power allocation results.
- PSS T3: Power division equivalent to **PSS T2**. DAB modules are rotated sequentially at a certain frequency[11].

To further introduce these three types of PSS, Figure 11 provides a visual representation of the relationship between power and the number of active DAB modules (N_a) under SPS. The N_a at a given load P can be expressed as

$$N_a = \begin{cases} N, & \text{PSS T1} \\ \left\lceil \sqrt{\frac{1}{4}+\frac{P^2}{P_\eta^2}} - \frac{1}{2} \right\rceil, & \text{PSS T2} \end{cases} \tag{5}$$

where P_η is the power level where a single DAB achieves the peak

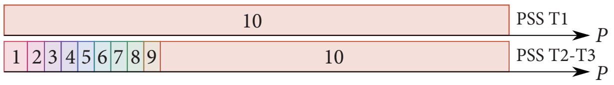


Figure 11 Comparison between even sharing (top) and efficiency-oriented module-shedding (bottom) PSSs under SPS modulation technique. Numbers indicate how many DAB modules are active for a given value of power *P*.

efficiency and $N_a \leqslant N$[12]. As shown in Figure 11, for PSS T1, all 10 modules operate simultaneously under any power requirements. Regarding PSS T2 and T3, as the power range changes, the number of activated DAB modules also varies, and it engages all modules from approximately 30% of $P_{\max}$. On the other hand, different power distribution results occur in the EPS and DPS, and further details are shown in Figure 12.

Figure 12 illustrates the power distribution among 10 modules in the case of different PSSs being applied to the SPS, EPS, and DPS with minimum BFP and peak current schemes, where PSS T1 is used for all modulations. The DAB modules are rotated at every charging event. t_{on} represents the percentage of active time for each module over one year. The average power during active periods is indicated with a dashed line. As shown in this figure, under PSS T2, power is allocated mostly in low-order modules, and high-order modules present a particularly low level of utilization, even less than 1% with the minimum BFP of EPS, which results in a sequential decrease in their active time. Thanks to the rotation in PSS T3, power allocation and active time assume an almost perfect balance among the modules. Comparing the two optimization schemes, although under PSS T2 that is without rotation, the minimum peak current scheme inherently achieves a more equal distribution of power among modules.

5 Lifetime and reliability evaluation

Based on the power allocation of individual modules illustrated in Figure 12 and the previously developed thermal model, the junction temperature profiles of the devices can be derived. However, the dynamics of the mission profile result in irregular temperature fluctuations. To address this, the rainflow counting method is utilized to transform the irregular thermal profiles into regular thermal loading cycles, which enables the extraction of the critical parameters for device lifetime estimation, including the mean junction temperature (T_{jm}), the temperature swing (ΔT_{j}), and the cycle period (t_{on})[20].

For switching devices, bond-wire lift-off failure is a key factor influencing device reliability, which is directly correlated with thermal behavior. Therefore, the Bayerer's lifetime model[30] is employed. It establishes the relationship between the number of cycles to failure (N_{f}) and the thermal parameters, specifically the minimum junction temperature (T_{jmin}) and ΔT_{j}, and is expressed as

$$N_{\mathrm{f}} = A \Delta T_{\mathrm{j}}^{-\beta_1} \mathrm{e}^{\frac{\beta_2}{T_{\mathrm{jmin}}+273}} t_{\mathrm{on}}^{\beta_3} I^{\beta_4} V^{\beta_5} D^{\beta_6} \tag{6}$$

where I, V, and D are the current per bond wire, blocking voltage, and bond wire diameter, respectively, and all the temperatures are in °C. A and $\beta_1 - \beta_6$ are technology fact and model parame-

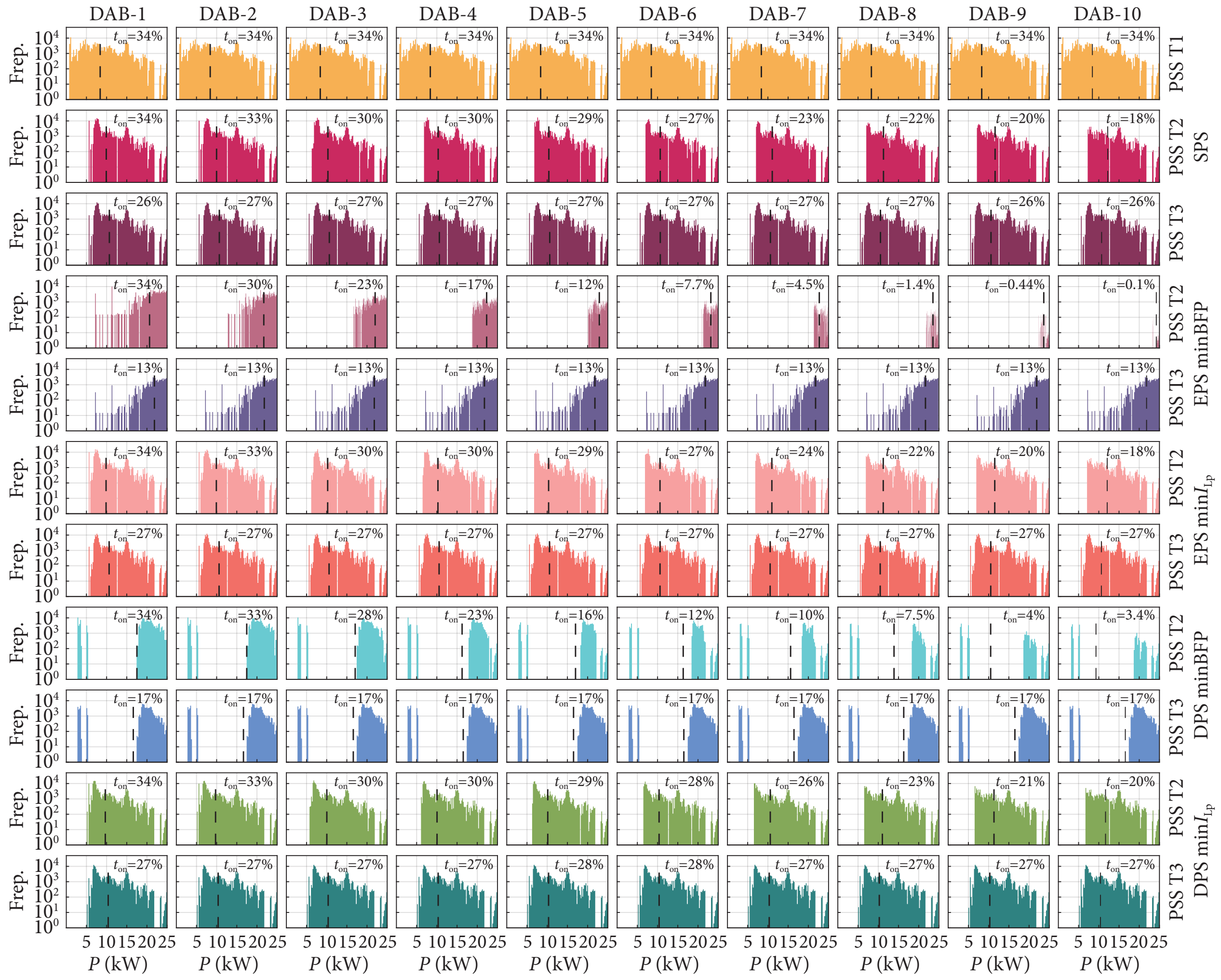


Figure 12 **Histogram of the power allocation strategies of even sharing, efficiency-oriented module shedding, and module shedding with rotation per event under SPS, EPS, and DPS with minimum BFP and peak current schemes. Dashed lines indicate the position of average power and t_{on} is the active time in percentage.**

ters, which can be obtained in Ref. [30].

Normally, the lifetime of the switching device is expressed by considering the life consumption, which is calculated via Miner's rule[19], accumulating the damage contributions from each thermal cycle. This approach enables the prediction of the device's lifetime, providing a robust basis for assessing system reliability.

In practical reliability analysis, due to the manufacturing tolerances, the technology factor and model parameters A and $\beta_1-\beta_6$ in Eq. (6) can deviate from their ideal values, and other electrical parameters can also differ from ideal conditions because of device and measurement errors. To address this, the Monte Carlo simulation method is commonly employed, utilizing the statistical probability of failure to represent the reliability of devices and systems[20]. In this approach, the parameters in Eq. (6) are sampled from a normal distribution with 100,000 data points, assuming a $\pm 5\%$ variation and a 99% confidence level. The lifetime consumption and corresponding lifetimes for these samples are then calculated and fitted using a Weibull distribution[21].

As shown in Figure 13, if any single switching device fails, the unit module cannot maintain operation at its rated power. Therefore, the converter-level reliability is assessed using a series reliability block diagram (RBD) with 8 components that accounts for the interdependence of component-level reliability. Similarly, to assume that there is no derating or redundant operation of the system, the system-level reliability is determined by aggregating the reliability of individual converters arranged in a series RBD. The system-level reliability expression is derived as

$$F_{\mathrm{sys}}(x)=1-\prod_{j=1}^{10}\left\{\prod_{i=1}^{8}\left[1-F_{i,j}(x)\right]\right\} \tag{7}$$

where $F(x)$ and $F_{\mathrm{sys}}(x)$ represent the unreliability function of the Weibull distribution of components and system, respectively.

To comprehensively evaluate the reliability performance of the modular DAB converter under the previously discussed PSSs, modulation techniques, and optimization schemes, two case studies are considered:

- Case study 1: In this case, the reliability performance of SPS, EPS, and DPS with minimum BFP and peak current schemes are analyzed. All three types of PSS introduced in Section 4.2 are included. The rotation frequency of PSS T3 is per event.
- Case study 2: The trade-off between system reliability and rotating frequency in PSS T3 is analyzed in this case study. In addition to rotating the modules per event, five additional rotation frequencies are considered: per month, per day, per hour, every 10 min, and per minute.

5.1 Case study 1

With reference to the mission profile introduced in Section 4.1, the three modulation techniques with minimum BFP and peak current schemes under different types of PSSs have been numerically simulated for all 10 DAB modules in the PLECS (Plexim GmbH) environment. To illustrate the variation in lifetime performance among the parallel-connected DAB converters, Table 5 shows the standard deviation of 10 DAB modules' B1 lifetime under different modulations and PSS types. The system B1 lifetime results, which are expressed in years with a 1% fault probability, are shown in Table 6.

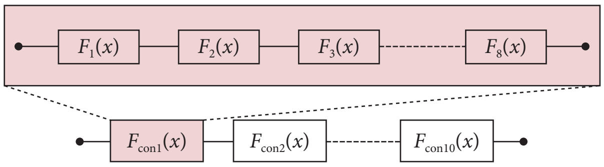


Figure 13 Series reliability block diagram of the 10-DAB system. Each DAB module contains 8 switching devices.

From Figure 12, it is evident that under PSS T1, the power is uniformly distributed across the 10 DAB converters, leading to identical reliability performance of each module, as shown in Table 5, where the standard deviation of PSS T1 is 0. As shown in Figure 12, the converter approximately operates in the full power range, particularly from 0 to 20 kW. Coupled with the thermal performance in Figure 9, the EPS with the minimum BFP scheme exhibits the highest junction temperatures, whereas SPS, EPS and DPS with the minimum peak current scheme have lower and comparable thermal performance. Further analysis reveals that under DPS with the minimum peak current scheme, switching devices S3, S4, Q1, and Q2 show a broader range of lower thermal behavior, particularly in the low-to-medium power range, which explains the superior reliability performance achieved by DPS with the minimum peak current.

Under PSS T2, module shedding results in uneven power distribution among the DAB converters from a long-term perspective, creating significant variability in their reliability performance. As shown in Table 5, the standard deviation of the B1 lifetime reaches as high as 74.2 years under EPS with the minimum BFP. SPS and DPS with the minimum BFP have standard deviations of 31.9 and 23.8 years, respectively. To illustrate the temperature imbalance caused by module shedding, Figure 14 presents the corresponding rainflow counting results over one year for the first and tenth DAB modules under EPS with the minimum BFP. It is evident that under PSS T2, the lower-order modules are always activated first. As a result, the first module experiences more complex thermal behavior, as illustrated in Figure 14, driven by a higher total number of thermal cycles, an increased number of cycles of large temperature fluctuations and average junction temperatures. In both EPS and DPS with the minimum BFP scheme, the average operating power shifts toward a higher level, more than 15 kW, leading to significantly higher thermal behavior. As the performance of the heavily loaded modules determines the reliability of the system, the B1 lifetimes of EPS and DPS with minimum BFP are only 3.97 and 6.32 years, respectively.

Under PSS T3, the rotating power distribution strategy balances the load among the 10 DABs, as evidenced by the significantly lower B1 lifetime standard deviations (i.e., < 1 year) compared with those of PSS T2, which can improve the system reliability. As shown in Table 6, the system reliability of SPS improves to 29.6 years, representing an approximate 1.4-year increase compared to PSS T2. For EPS and DPS, the rotating strategy brings marginal reliability improvements, with the B1 lifetime increasing by less than 1 year.

Therefore, in the case of only considering the reliability of the switching device, PSS T1 exhibits the best reliability performance among the three types of PSSs. However, in practical applications, module shedding is widely adopted in modular configurations due to the advantages of high efficiency[11]. From a comprehensive

Table 5 Standard deviation of 10 modules' B1 lifetime

Description	SPS	EPS		DPS		Unit
		minBFP	minI_{Lp}	minBFP	minI_{Lp}	
PSS T1	0	0	0	0	0	Year
PSS T2	31.9	74.2	5.47	23.8	4.61	Year
PSS T3	0.65	0.23	1.05	0.36	1.12	Year

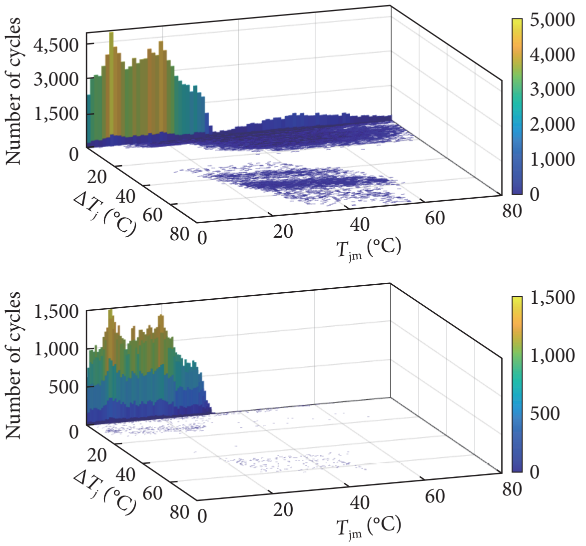


Figure 14 Rainflow counting results of the thermal loadings of the switches on the secondary side in the first (top) and tenth (bottom) DAB converter. The EPS with minimum BFP scheme is considered.

perspective, using PSS T3 can help mitigate the reliability degradation introduced by PSS T2 while still maintaining high efficiency. Furthermore, the DPS with the minimum peak current scheme enhances the lifetime of switches by effectively reducing the current stress.

5.2 Case study 2

Based on the above analysis, the rotating module shedding PSS demonstrates advantages in both efficiency and reliability. However, the rotation frequency needs to be determined since it plays a critical role in affecting the system reliability. In this case study, PSS T2 represents the non-rotating situation, with a rotation frequency of zero. In addition to the PSS T3 with per event rotation, five additional rotation frequencies are considered: per month, per day, per hour, every 10 minutes, and per minute.

To illustrate the thermal behavior of the DAB converter under different rotation frequencies, the rainflow counting results of experienced thermal cycles under a certain temperature fluctuation amplitude ΔT_j for the switching devices in the first DAB module under DPS with the minimum peak current scheme are shown in Figure 15. For PSS T2, the total thermal cycles are 175,341. With rotation implemented at frequencies of one month, one day, one event, one hour, and 10 minutes, the thermal stress is more evenly distributed among modules. This results in a notable reduction in the number of cycles in the small junction temperature swing range, with the total number of cycles reduced to approximately 174,000. In contrast, the one-minute rotation case exhibits a different trend, where the faster transitions between active and idle states cause more complex temperature fluctuations, leading to an increased number of low-amplitude thermal cycles and a higher total cycle count of 180,734.

A complete analysis of all modulation techniques under different rotation frequencies is summarized in Table 7, while Figure 16 further presents the trends in B1 lifetime with the rotation frequency changing. It is observed that once PSS T3 occurs with a frequency of one month, the system reliability can be improved compared with PSS T2. Generally, as the rotation frequency increases, the B1 lifetime continues to rise to an optimal lifetime. For SPS, the highest B1 lifetime is achieved at a 10-minute rotation frequency. For EPS with minimum BFP and minimum peak current, the peak reliability occurs with daily and per-event rotation, respectively. For the minimum BFP and peak current under DPS, the maximum lifetimes are reached with monthly and hourly rotation, respectively. However, as the rotation frequency increases beyond the optimal situation, a decrease in system lifetime is observed. In particular, under the one-minute rotation PSS, the lifetime drops below that of PSS T2 in some cases. Therefore, although the temperature fluctuation amplitudes decrease at high rotation frequencies, the significantly higher number of thermal cycles, along with the more complex and rapid thermal transients, can increase the probability of failure.

6 Analysis and discussion

6.1 Analysis of the potential cost

According to the reliability results presented in this work, it is also meaningful to analyze the potential cost associated with both losses and maintenance[31]. As shown in the junction temperature map of Figure 9, which inherently reflects the loss behavior under different operating points, modulations and optimized schemes. It can be observed that EPS and DPS with the minimum BFP scheme exhibit significantly higher junction temperatures, particularly in the high-power and high-voltage region. This indicates higher losses and therefore a higher operational cost associated with energy losses. In contrast, SPS, EPS and DPS with minimum peak current achieve much lower junction temperatures, implying lower losses and reduced loss-related cost.

The maintenance cost is strongly related to the reliability results, which is the main work in this paper. Based on the results in Table 6 and Table 7, DPS with minimum peak current achieves the longest lifetime, implying the lowest maintenance cost. Table 5 shows that PSS T2 causes a large power imbalance among modules, forcing the low-order modules to operate longer and hence suffer earlier aging, which increases maintenance cost. In contrast, PSS T1, where all modules are operating together, distributes the thermal and electrical stress more evenly, resulting in higher reliability and therefore lower maintenance cost. For PSS T3, a higher rotation frequency increases thermal fluctuations and therefore decreases reliability, which also elevates maintenance cost.

In summary, for modulation techniques, the loss-related cost

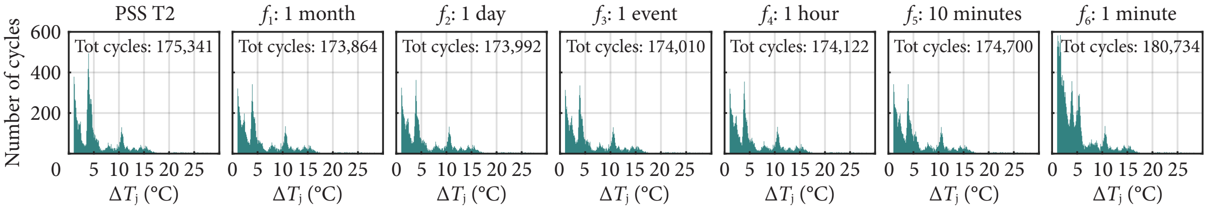


Figure 15 Rainflow counting results of experienced thermal cycles under the certain temperature fluctuation amplitude ΔT_j for PSS T2, PSS T3 with the rotation frequency of 1 month, 1 day, 1 event, 1 hour, 10 minutes, and 1 minute. Only cases with $\Delta T_j > 1$ °C are shown here. The "tot cycles" is the total number of thermal cycles.

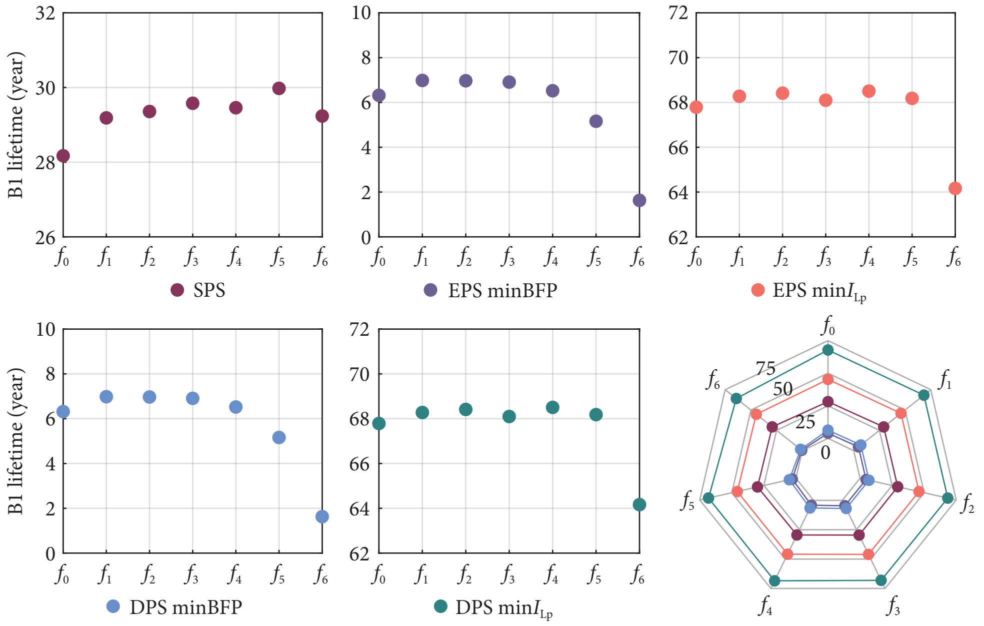


Figure 16 System-level B1 lifetime with the function of rotation frequency. f_0–f_6 represent the rotation frequency of none rotation, per month, per day, per event, per hour, 10 minutes, and 1 minute, respectively.

and maintenance-related cost exhibit consistent trends. The minimum peak current optimized scheme for EPS and DPS tends to provide both lower losses and higher reliability, making it an effective method for reducing the overall system cost.

For power sharing strategies, the situation is more complex. The literature indicates that PSS T1 provides lower efficiency, while our reliability analysis shows that PSS T1 has the best lifetime performance. Conversely, PSS T2 and PSS T3 achieve higher efficiency but suffer from reduced reliability. This trade-off between operational loss and maintenance cost requires further investigation.

6.2 Directions for future reliability enhancement

Based on the reliability results, several insights can be drawn regarding potential methods for extending the lifetime of modular DAB converters. First, among the three modulation methods, DPS exhibits the highest reliability due to its additional degrees of freedom, which cause more flexibility in reducing the inductor current. In particular, the ability of DPS to effectively suppress the peak current has been shown to play a dominant role in reducing the junction temperature and improving the overall device lifetime. These results indicate that increasing the number of control degrees of freedom is a promising direction for broadening the operating region in which the current stress can be minimized.

Table 6 System-level B1 lifetime under different power sharing strategies

Description	SPS	EPS		DPS		Unit
		minBFP	minI_{Lp}	minBFP	minI_{Lp}	
PSS T1	39.7	6.35	47.1	27.3	71.2	Year
PSS T2	28.2	3.97	45.3	6.32	67.8	Year
PSS T3	29.6	4.57	46.0	6.91	68.1	Year

In the modular configuration, the rotating PSS has demonstrated a clear advantage in equalizing the thermal behavior across the modules. The results confirm that a more uniform module temperature distribution is correlated with improved reliability. This emphasizes that thermal balancing is an effective reliability enhancement strategy.

Therefore, there are several directions that are particularly promising for future lifetime extension:

- Expanding the ZVS range and minimizing the current stress under multi-degree-of-freedom modulation.

Triple phase shift, four- or five-degree of freedom modulations hold the potential to widen the ZVS region and reduce RMS and peak current stresses, which are critical factors driving device reliability.

- Achieving thermal balancing not only across modules but also between devices.

As shown in Figure 9, the temperature imbalance occurs on the different legs, especially in EPS and DPS. Techniques such as active thermal control can be used to redistribute the loss to balance the thermal performance.

- Developing coordinated modulation and power-sharing strategies.

The results show that both modulation and PSS can impact

Table 7 System-level B1 lifetime of all modulation techniques under different rotation frequencies

Description	PSS T2	PSS T3						Unit
		1 month	1 day	1 event	1 h	10 min	1 min	
SPS	28.17	29.19	29.36	29.58	29.46	29.98	29.24	Year
EPS minBFP	3.973	4.641	4.664	4.574	4.154	2.856	< 1	Year
EPS minI_{Lp}	45.26	45.98	45.93	45.99	45.84	45.74	44.74	Year
DPS minBFP	6.317	6.981	6.968	6.908	6.523	5.161	1.627	Year
DPS minI_{Lp}	67.79	68.28	68.41	68.10	68.51	68.18	64.16	Year

device current stress and temperature. Co-optimization of these two components can further enhance the system reliability.

7 Conclusions

In this paper, a comprehensive reliability evaluation of a modular DAB converter under SPS, EPS, and DPS with minimum BFP and peak current is performed, along with power sharing strategies such as even sharing and module shedding with and without rotation in the application of EV chargers. The key findings can be summarized as follows:

- The EPS and DPS with the minimum peak current scheme enhance the lifetime of the switches by reducing the current stress, especially at low-to-medium power levels. The minimum BFP scheme can improve the transmission power quality but increase the current stress and thermal on switching devices. SPS performs well, especially in high-power conditions, and has the potential to reduce both the backflow power and peak current.
- The module shedding with rotation balances the thermal distribution of all modules, improving the reliability compared to the module shedding without rotation while maintaining a higher efficiency than that of even sharing.
- Overall, the rotation frequencies from one month to one hour can retain comparable reliability performance. Frequent rotation (e.g., per minute) increases thermal cycling and reduces the system lifetime despite low temperature swings.

In summary, these results provide valuable insights for designing robust and reliable high-power EV charging systems. By selecting the DPS with minimum peak current under rotating shedding in an approximately one-hour rotation frequency, the converter design can achieve the best balance between efficiency, thermal performance, and system reliability.

Appendix

Based on the Lagrange multiplier algorithm introduced in Section 2, the optimal solutions for EPS and DPS with minimum BFP and peak current schemes are summarized in this Appendix. The results are categorized according to different power ranges and voltage conversion ratios. In addition, the working modes shown in Figures 2 and 3 are also listed in the Tables A1 to A4.

Table A1 Optimization results of EPS with minimum BFP

P_{in}	k	D_1	d	Mode
$[P_{\text{lim1}}, 1]$	/	$\frac{(4+4k)\,d+1}{2k+4}$	$[d_{\text{lim1}}, 0.25]$	1
$[P_{\text{lim2}}, P_{\text{lim1}}]$	/	$\frac{0.25-d}{0.5k}$	$[d_{\text{lim1}}, d_{\text{lim2}}]$	1
$[0, P_{\text{lim2}}]$	/	$\frac{0.25-d}{0.5k}$	$[d_{\text{lim2}}, 0.25]$	2

Table A2 Optimization results of EPS with minimum peak current

P_{in}	k	D_1	d	Mode
$[P_{\text{lim1}}, 1]$	$k \geqslant 1$	$\frac{(4k-4)\,d+1}{2k}$	$[0, 0.25]$	1
$[0, P_{\text{lim1}}]$	$1 < k < 2$	0.5	$[0, 0.25]$	1
$[0, P_{\text{lim1}}]$	$k \geqslant 2$	$d = 0.5$	$[0, 0.25]$	1
$[0,1]$	$k < 1$	0.5	$[0, 0.25]$	1

Table A3 Optimization results of DPS with minimum BFP

P_{in}	k	D_1	d	Mode
$[P_{\text{lim1}}, 1]$	$k \geqslant 1$	$\frac{1}{2}-\left(\frac{1}{4}-d\right)(k+1)$	$[d_{\text{lim1}}, 0.25]$	1
$[P_{\text{lim4}}, P_{\text{lim1}}]$	$k \geqslant 1$	$\frac{-B \pm \sqrt{B^2-4AC}}{2A}^{\dagger}$	$[0.5-D_1, 0.25]$	1
$[P_{\text{lim2}}, 1]$	$k < 1$	$\frac{1}{2}-\left(\frac{1}{4}-d\right)(k+1)$	$[d_{\text{lim2}}, 0.25]$	1
$[P_{\text{lim3}}, P_{\text{lim2}}]$	$k < 1$	$\frac{1-2d}{k+1}$	$[d_{\text{lim2}}, 0.25]$	1
$[P_{\text{lim4}}, P_{\text{lim3}}]$	$k < 1$	$\frac{-B + \sqrt{B^2-4AC}}{2A}^{\dagger}$	$[0.5-D_1,\ 0.25]$	1
$[0, P_{\text{lim4}}]$	/	d	$[0,\ 0.25]$	2

†$A=-8k$, $B=4k^2d+4d-k^2+6k-1$, $C=16kd^2-8kd$

Table A4 Optimization results of DPS with minimum peak current

P_{in}	k	D_1	d	Mode
$[P_{\text{lim1}}, 1]$	$k \geqslant 1$	$(k-1)\,d-\frac{1}{4}k+\frac{3}{4}$	$[d_{\text{lim1}}, 0.25]$	1
$[0, P_{\text{lim1}}]$	$k \geqslant 1$	$\frac{k+1}{k-1}d$	$[0, d_{\text{lim1}}]$	2
$[P_{\text{lim2}}, 1]$	$k < 1$	$\frac{3k-1}{4k}+\frac{1-k}{k}d$	$[d_{\text{lim2}}, 0.25]$	1
$[0, P_{\text{lim2}}]$	$k < 1$	$\frac{1+k}{1-k}d$	$[0, d_{\text{lim2}}]$	2

A EPS with minimum BFP

The solutions for EPS with minimum BFP are listed in Table A1. P_{lim1} and P_{lim2} represent the power limits of each case, while d_{lim1} and d_{lim2} are the limits of the outer phase shift value in a certain power range. The results are independent of the k requirements.

$$\begin{cases} P_{\text{lim1}} = \dfrac{2k+2}{k^2+2k+2} \\ P_{\text{lim2}} = \dfrac{2k+2}{(2+k)^2} \end{cases} \tag{A1}$$

$$\begin{cases} d_{\text{lim1}} = \dfrac{1}{2\,(k^2+2k+2)} \\ d_{\text{lim2}} = \dfrac{1}{2\,(k+2)} \end{cases} \tag{A2}$$

B EPS with minimum peak current

Table A2 presents the optimal phase shift combinations for EPS with minimum peak current. In this scheme, only mode 1 is needed, and d remains within the standard range of [0, 0.25] without any additional constraints.

$$P_{\text{lim1}} = \frac{2k-2}{k^2} \tag{A3}$$

C DPS with minimum BFP

Due to the flexible control characteristics of DPS, more cases of power conditions are considered, as shown in Table A3. When the converter operates in mode 2, the optimal solutions are independent of k.

$$\begin{cases} P_{\text{lim1}} = \dfrac{(k+1)\,(k+5)\,(k^2+2k-1)}{(k^2+4k+1)^2} \\ P_{\text{lim2}} = \dfrac{-8k^2+16k+24}{8(k+1)^2+16} \\ P_{\text{lim3}} = \dfrac{-3(k+1)^2+2\,(k+3)\,(k+1)-2}{(k+1)^2} \\ P_{\text{lim4}} = \dfrac{1}{2} \end{cases} \tag{A4}$$

$$\begin{cases} d_{\mathrm{lim}1} = \dfrac{k^2+4k-1}{4k^2+16k+4} \\ d_{\mathrm{lim}2} = \dfrac{k^2+3}{4\left(k^2+2k+3\right)} \end{cases} \tag{A5}$$

D. DPS with minimum peak current

The optimal solutions for DPS with minimum peak current are summarized in Table A4. Similar to the minimum BFP scheme, all cases can be achieved in mode 1 and mode 2.

$$\begin{cases} P_{\mathrm{lim}1} = \dfrac{k^2+2k-3}{2k^2} \\ P_{\mathrm{lim}2} = -\dfrac{3}{2}k^2+k+\dfrac{1}{2} \end{cases} \tag{A6}$$

$$\begin{cases} d_{\mathrm{lim}1} = \dfrac{k-1}{4k} \\ d_{\mathrm{lim}2} = \dfrac{1-k}{4} \end{cases} \tag{A7}$$

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Additional information

Declaration of competing interest

The authors have no competing interests to declare that are relevant to the content of this article.

References

[1] IEA (2025). Global EV outlook 2025. International Energy Agency (IEA). Available at https://www.iea.org/reports/global-ev-outlook-2025

[2] Drobnic, K., Grandi, G., Hammami, M., Mandrioli, R., Ricco, M., Viatkin, A., Vujacic, M. (2019). An output ripple-free fast charger for electric vehicles based on grid-tied modular three-phase interleaved converters. *IEEE Transactions on Industry Applications*, 55: 6102–6114.

[3] Geng, J., Mandrioli, R., Sangwongwanich, A., Ricco, M. (2025). Impacts of reliability-oriented phase shedding in modular DAB EV charging. In: Proceedings of the 2025 IEEE/AIAA Transportation Electrification Conference and Electric Aircraft Technologies Symposium (ITEC+EATS), Anaheim, CA, USA.

[4] de Doncker, R. W. A. A., Divan, D. M., Kheraluwala, M. H. (1991). A three-phase soft-switched high-power-density DC/DC converter for high-power applications. *IEEE Transactions on Industry Applications*, 27: 63–73.

[5] Zhao, B., Yu, Q., Sun, W. (2012). Extended-phase-shift control of isolated bidirectional DC–DC converter for power distribution in microgrid. *IEEE Transactions on Power Electronics*, 27: 4667–4680.

[6] Mandrioli, R., Ricco, M., Grandi, G., Pereira, T. A., Liserre, M. (2022). DAB-based common-mode injection in three-phase four-wire inverters. In: Proceedings of the 2022 IEEE 16th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG), Birmingham, UK.

[7] Keshmiri, N., Pradhan, R., Hassan, M. I., Emadi, A. (2022). An optimized GaN-based DAB converter for more electric aircraft. In: Proceedings of the IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium.

[8] Mudiyanselage, G. A., Keshmiri, N., Emadi, A. (2023). Comparative analysis of single phase shift control and optimized extended phase shift control of dual active bridge converters for wide voltage range applications. In: Proceedings of the IECON 2023- 49th Annual Conference of the IEEE Industrial Electronics Society, Singapore.

[9] Shi, H., Wen, H., Chen, J., Hu, Y., Jiang, L., Chen, G., Ma, J. (2018). Minimum-backflow-power scheme of DAB-based solid-state transformer with extended-phase-shift control. *IEEE Transactions on Industry Applications*, 54: 3483–3496.

[10] Polat, H., Hosseinabadi, F., Chakraborty, S., Geury, T., El Baghdadi, M., Hegazy, O. (2023). Assessing the impact of EV charging and discharging profiles on T-type active front end charger lifetime. In: Proceedings of the IECON 2023- 49th Annual Conference of the IEEE Industrial Electronics Society, Singapore.

[11] Alharbi, M. A., Alcaide, A. M., Dahidah, M., Montero-Robina, P., Ethni, S., Pickert, V., Leon, J. I. (2023). Rotating phase shedding for interleaved DC–DC converter-based EVs fast DC chargers. *IEEE Transactions on Power Electronics*, 38: 1901–1909.

[12] Kolar, J. W., Krismer, F., Lobsiger, Y., Muhlethaler, J., Nussbaumer, T., & Minibock, J. (2012). Extreme efficiency power electronics. In: Proceedings of the 2012 7th International Conference on Integrated Power Electronics Systems (CIPS), Nuremberg, Germany.

[13] Son, G., Huang, Z., Li, Q. (2022). Light load efficiency improvement for two-channel paralleled soft-switching three-phase inverter using phase shedding control. *IEEE Transactions on Power Electronics*, 37: 10200–10212.

[14] Zhou, X., Donati, M., Amoroso, L., Lee, F. C. (2000). Improved light-load efficiency for synchronous rectifier voltage regulator module. *IEEE Transactions on Power Electronics*, 15: 826–834.

[15] Xiao, Z., Yao, Z., Deng, F., Zhang, L., Tang, Y. (2024). Seamless rotational phase shedding for multiphase DC–DC converters. *IEEE Transactions on Power Electronics*, 39: 4996–5001.

[16] Yedukondalu, G., Samanta, S. (2023). Effective phase utilization and efficiency improvement of high power interleaved DC–DC converter using modified rotating phase shedding control. *Computers and Electrical Engineering*, 110: 108837.

[17] Geng, J., Mandrioli, R., Sangwongwanich, A., Ricco, M. (2025). Impacts of SPS, DPS, and EPS modulations on the reliability of modular DAB EV chargers. In: Proceedings of the 2025 IEEE 19th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Antalya, Turkiye.

[18] He, J., Sangwongwanich, A., Yang, Y., Iannuzzo, F. (2021). Lifetime evaluation of three-level inverters for 1500-V photovoltaic systems. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9: 4285–4298.

[19] Chakraborty, S., Hasan, M. M., Paul, M., Tran, D. D., Geury, T., Davari, P., Blaabjerg, F., El Baghdadi, M., Hegazy, O. (2022). Real-life mission profile-oriented lifetime estimation of a SiC interleaved bidirectional HV DC/DC converter for electric vehicle drivetrains. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 10: 5142–5167.

[20] Sangwongwanich, A., Yang, Y., Sera, D., Blaabjerg, F. (2018). Life-

time evaluation of grid-connected PV inverters considering panel degradation rates and installation sites. *IEEE Transactions on Power Electronics*, 33: 1225–1236.

[21] Karunarathna, J., Madawala, U., Baguley, C., Blaabjerg, F., Sandelic, M. (2021). Reliability analysis of fast electric vehicle charging systems. In: Proceedings of the 2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia), Singapore.

[22] Reigosa, P. D., Wang, H., Yang, Y., Blaabjerg, F. (2016). Prediction of bond wire fatigue of IGBTs in a PV inverter under a long-term operation. *IEEE Transactions on Power Electronics*, 31: 7171–7182.

[23] Pittala, L. K., Barbone, R., Mandrioli, R., Cirimele, V., Ricco, M., Grandi, G. (2023). Insights on DAB converter with auxiliary inductors. In: Proceedings of the 2023 International Conference on Clean Electrical Power (ICCEP), Terrasini, Italy.

[24] Cuoghi, S., Pittala, L. K., Mandrioli, R., Cirimele, V., Ricco, M., Grandi, G. (2024). Model-based adaptive control of modular DAB converter for EV chargers. *IET Power Electronics*, 17: 2669–2685.

[25] Novak, M., Sangwongwanich, A., Blaabjerg, F. (2021). Monte Carlo-based reliability estimation methods for power devices in power electronics systems. *IEEE Open Journal of Power Electronics*, 2: 523–534.

[26] Wolfspeed (2025). E3M0032120J2: Silicon carbide power MOSFET E-series automotive N-channel enhancement mode. Available at https://assets.wolfspeed.com/uploads/2024/01/Wolfspeed_E3M0032120J2_data_sheet.pdf

[27] Wolfspeed (2025). E4M0015075J2: Silicon carbide power MOSFET E-series automotive N-channel enhancement mode. Available at https://assets.wolfspeed.com/uploads/2024/04/Wolfspeed_E4M0015075J2_data_sheet.pdf

[28] Franco, F., Ricco, M., Cirimele, V., Apicella, V., Carambia, B., Grandi, G. (2023). Electric vehicle charging hub power forecasting: A statistical and machine learning based approach. *Energies*, 16: 2076.

[29] Lo Franco, F., Cirimele, V., Ricco, M., Monteiro, V., Afonso, J. L., Grandi, G. (2022). Smart charging for electric car-sharing fleets based on charging duration forecasting and planning. *Sustainability*, 14: 12077.

[30] Bayerer, R., Herrmann, T., Licht, T., Lutz, J., & Feller, M. (2008). Model for power cycling lifetime of IGBT modules-various factors influencing lifetime. In: Proceedings of the 5th international conference on integrated power electronics systems, Nuremberg, Germany.

[31] Grazian, F., Ceccarelli, L., Mandrioli, R., Sangwongwanich, A., Ricco, M. (2025). Circular economy R-strategies for reliability-oriented modular DAB EV charging with phase shedding. In: Proceedings of the IECON 2025 – 51st Annual Conference of the IEEE Industrial Electronics Society, Madrid, Spain.