

Alma Mater Studiorum Università di Bologna  
Archivio istituzionale della ricerca

Thickness-dependent dielectric breakdown in thick amorphous SiO<sub>2</sub> capacitors

This is the final peer-reviewed author's accepted manuscript (postprint) of the following publication:

*Published Version:*

Giuliano F., Reggiani S., Gnani E., Gnudi A., Rossetti M., Depetro R. (2022). Thickness-dependent dielectric breakdown in thick amorphous SiO<sub>2</sub> capacitors. SOLID-STATE ELECTRONICS, 194, 1-5 [10.1016/j.sse.2022.108363].

*Availability:*

This version is available at: <https://hdl.handle.net/11585/895709> since: 2022-10-10

*Published:*

DOI: <http://doi.org/10.1016/j.sse.2022.108363>

*Terms of use:*

Some rights reserved. The terms and conditions for the reuse of this version of the manuscript are specified in the publishing policy. For all terms of use and more information see the publisher's website.

This item was downloaded from IRIS Università di Bologna (<https://cris.unibo.it/>).  
When citing, please refer to the published version.

(Article begins on next page)

# Thickness-dependent dielectric breakdown in thick amorphous SiO<sub>2</sub> capacitors

Federico Giuliano<sup>a,\*</sup>, Susanna Reggiani<sup>a</sup>, Elena Gnani<sup>a</sup>, Antonio Gnudi<sup>a</sup>, Mattia Rossetti<sup>b</sup>, Riccardo Depetro<sup>b</sup>

<sup>a</sup>ARCES and DEI, University of Bologna, Bologna, Italy

<sup>b</sup>Smart Power R/D, STMicroelectronics, Cornaredo, Italy

---

## Abstract

High-voltage dielectric breakdown of thick amorphous silicon dioxide capacitors for galvanic insulation is experimentally investigated and analyzed through numerical simulations carried out with a commercial TCAD tool. Silicon oxide metal-insulator-metal capacitors are used as back-end inter-level dielectric layers in integrated circuits. The large biases such devices must sustain and the material intrinsic defectivity give rise to a leakage current which is responsible of degradation and failure. Therefore, the understanding of the degradation mechanisms of the insulator is an essential prerequisite for its safe operation. For this reason, high-voltage dielectric breakdown measurements have been performed under DC-stress conditions on thick metal-insulator-metal structures with different oxide thickness and, in order to gain insight on the role of defects on breakdown, numerical simulations have been compared to experiments.

**Keywords:** Silicon oxide, Insulators, Reliability, TEOS

---

## 1. Introduction

Metal-insulator-metal (MIM) capacitors embedded in the back-end inter-level dielectric layers are used for analog and RF applications [1, 2, 3]. To this purpose, silicon dioxide (SiO<sub>2</sub>) is the best insulator candidate because of its near-ideal properties. However, the device degradation and failure are limited by the charge buildup in pre-existing defect sites of the oxide layer. This is mostly related to the plasma-enhanced chemical vapor deposition (PE-CVD) process adopted for the deposition of tetraethyl orthosilicate (TEOS) for back-end galvanic insulation and to the specific properties of the structures made through several deposition steps due to their thicknesses in the micrometer range [4, 5, 6]. Due to the very high biases these structures must sustain, charge injection at the contacts leads to a leakage current that limits the device performance and reliability [7], together with charge build-up in the bulk of the oxide [8].

As far as the physical mechanisms responsible for the breakdown are concerned, many studies have been carried out for very thin oxides, such as gate oxide structures in CMOS technologies, in the past. It is widely accepted that breakdown in thin oxides is due to the formation of percolation paths connecting cathode and anode caused by the generation of defects in the bulk oxide [9]. Thus, the breakdown field typically increases with the film thickness [10]. Viceversa, in thicker oxides it has been shown that impact ionization plays a relevant role in the definition of the breakdown. This is confirmed by some works

on devices with oxide thickness in the range of 10 – 100 nm[11, 12], but much less is known about even thicker oxides, such as those used for galvanic insulation applications. Since stacked dielectrics have long been used in commercial products, the reliability of the technology is empirically well established, but very few works are based on a self-consistent theoretical framework [6].

The main motivation of this work is to accurately describe the breakdown mechanisms in thick oxides through a TCAD-based modeling approach which can be useful for the development and optimization of capacitances in integrated high-voltage systems.

## 2. Test structures and experiments

Fig. 1 shows a cross section of the high-voltage MIM capacitor used in this work. The electrodes are in tantalum nitride (Ta<sub>2</sub>N<sub>3</sub>). The high voltage is applied to the circular top metal electrode (diameter  $d \approx 150 \mu\text{m}$ ), while the bottom metal electrode is grounded. TEOS material is used as intermetal dielectric. The ring contact ensures protection of the device from external disturbances and acts as grounded lateral boundary condition. The distance between the ring contact and the top metal is at least 10 times the oxide thickness and has been kept constant in every measure performed.

Voltage-ramp measurements have been carried out under DC stress conditions. The DC voltage stress was performed by applying a stair-case voltage ramp at a constant rate until the breakdown condition was reached. The stair-case rampage is applied to avoid the displacement current. Capacitors with different oxide thicknesses ( $t_{\text{OX}}$ ) have been investigated. In order to apply the same stress

---

\*Corresponding author

Email address: federico.giuliano2@unibo.it (Federico Giuliano)

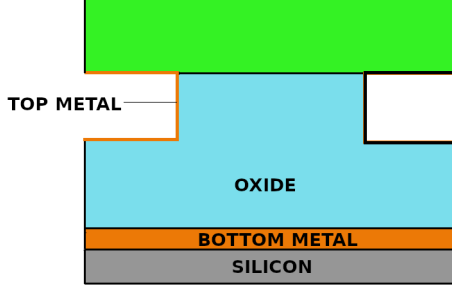


Figure 1: Schematic view of the TEOS capacitor.

conditions to all the samples, different voltage-ramp rates ( $V_{\text{rate}}$ ) have been used for each device in order to have the same oxide-field rate, defined as  $E_{\text{rate}} = |V_{\text{rate}}|/t_{\text{OX}}$ . As far as DC ramps are concerned, the top metal acts as a cathode while the bottom metal acts as anode. The oxide field ramp rate used for all samples is  $E_{\text{rate}} = 0.073 \text{ MV cm}^{-1} \text{ s}^{-1}$ . Five  $t_{\text{OX}}$  in the range between  $0.6 \mu\text{m}$  and  $15 \mu\text{m}$  have been investigated. All measurements have been carried out at room temperature, namely  $T = 25^\circ\text{C}$ . The nominal thickness of the devices under study, the corresponding voltage-ramp and the oxide-field rates are reported in Table 1.

Table 1: Nominal oxide thickness, voltage ramp rates and oxide field ramp rates applied to the MIM structures used in experiments.

$t_{\text{OX}}$ ( $\mu\text{m}$ )	$ V_{\text{rate}} $ (V/s)
0.6	4.4
0.9	6.6
7.0	51
10.0	73
15.0	110

Fig. 2 shows the current density  $J$  as a function of the oxide electric field  $E_{\text{OX}} = |V|/t_{\text{OX}}$ , with  $V$  the voltage applied at the top electrode. Measurements were performed up to the breakdown for the devices with thickness  $0.6 \mu\text{m}$  and  $0.9 \mu\text{m}$ . The J-E characteristics show a similar trend. At low fields, up to about  $E_{\text{OX}} = 6 \text{ MV/cm}$ , the relevant increase of the current is due to charge injection at contacts [8]. At intermediate fields, namely  $6 \text{ MV/cm} < E_{\text{OX}} < 8 \text{ MV/cm}$ , the current saturation indicates that the charge trapping is the predominant physical effect in this region, as the injected charges are trapped in oxide defects and cannot contribute to the current, while the electric field at the cathode is reduced limiting the charge tunneling effect [8]. At higher fields ( $F_{\text{OX}} > 8 \text{ MV/cm}$ ) the current increases again up to the breakdown: impact ionization plays a relevant role in this portion of the characteristics as shown in the following section.

The breakdown of the thicker oxides was investigated by hard-breakdown measurements by applying the same

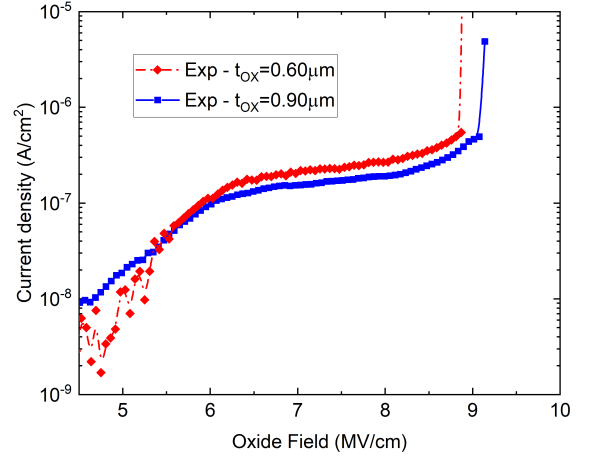


Figure 2: Measurements of the current density as a function of the oxide field up to the breakdown for the devices with thickness  $0.6 \mu\text{m}$  and  $0.9 \mu\text{m}$ .

ramp-rate up to breakdown. Fig. 3 shows the breakdown field as a function of the film thickness for each device under study. A weak dependence is observed. The breakdown field slightly increases with  $t_{\text{OX}}$  for the thinner oxides, while it decreases for longer  $t_{\text{OX}}$ , following a dependence which could be ascribed to the impact ionization as explained in [6].

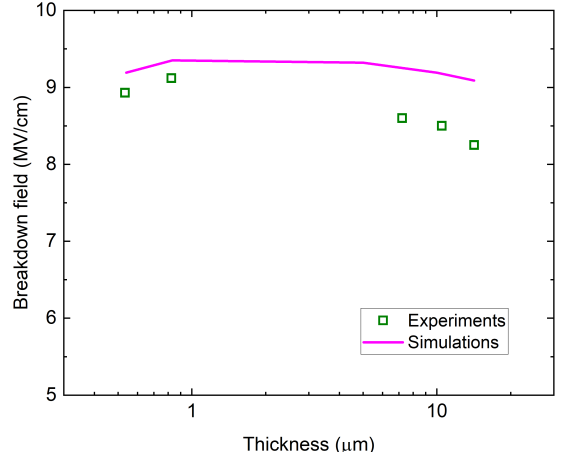


Figure 3: Breakdown field as a function of the oxide thickness for samples with thicknesses up to  $15 \mu\text{m}$ . Experiments: open symbols. Simulations: solid line.

### 3. Modeling and simulations

Conduction in  $\text{SiO}_2$  has been modeled by using the drift-diffusion (DD) transport equation with suitable physical parameters. Among them, the energy structure for the conduction and valence bands, the presence of distributed defects in the band gap and the tunneling injection at the contacts have been accurately addressed [8, 13, 14]. Two uniform distributions of traps have been explicitly defined

by fixing their energy dependence, density and capture cross-section [8]. Trapping and de-trapping mechanisms have been taken into account by using a first-order detailed balance equation for each trap as available in the TCAD tool [15]; the trap equations are solved consistently along with Poisson and electron and hole transport equations. A cylindrical symmetry has been assumed in order to predict the realistic 3D circular structure.

As far as the high-field transport is concerned, the effect of avalanche due to impact ionization cannot be neglected in order to have a complete picture of the relevant physical mechanisms [16]. For this reason, the impact-ionization generation has been taken into account in our simulation setup by activating the Okuto-Crowell model [17]. Fig. 4 shows the ionization coefficient for electrons compared with the experimental data reported in [16]. Slight differences are observed between the experimental data and the calibrated Okuto TCAD model, especially at high electric fields. However, it should be pointed out that TEOS oxides tend to show different electrical properties with respect to thermally grown  $\text{SiO}_2$ , such as different Schottky barriers [18], thus affecting also the impact ionization mechanism. No specific indication was found for the impact-ionization coefficient of holes, as avalanche is mostly due to electrons in  $\text{SiO}_2$ . The same ionization coefficient is thus used also for holes.

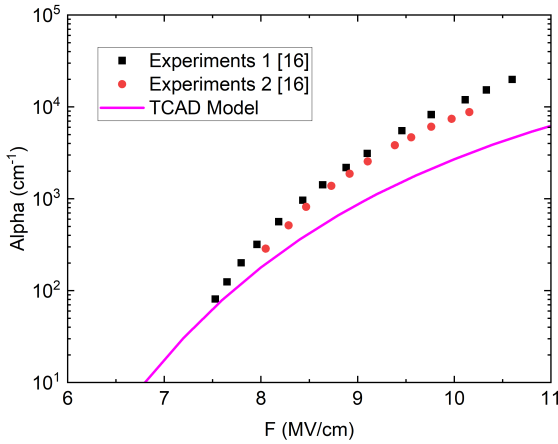


Figure 4: Electron avalanche coefficient as a function of the electric field at room temperature. Symbols: experimental data in [16]. Solid line: calibrated TCAD model at room temperature.

Fig. 5 shows the TCAD results of the current density versus the oxide field at  $T = 25^\circ\text{C}$ . Experiments are qualitatively reproduced: the current level in the intermediate-field portion of the characteristics, the breakdown field and its slight dependence on the oxide thickness are correctly captured by simulations, indicating that the most relevant physical mechanisms have been taken into account and properly modeled.

The predicted breakdown fields are reported in Fig. 3: even if a slight overestimation is found with respect to the experimental data, the overall dependence on the oxide

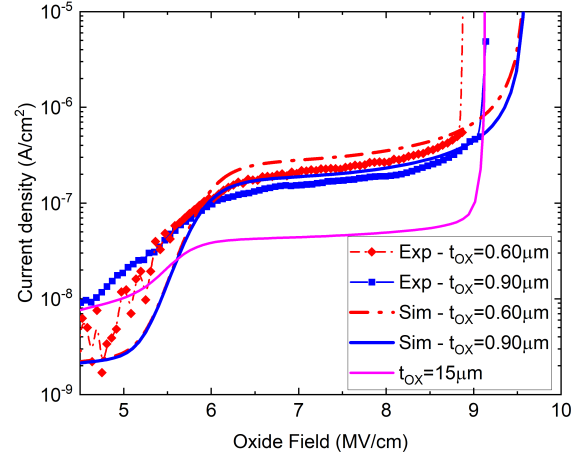


Figure 5: Current density as a function of the oxide field up to the breakdown for different oxide thickness. Symbols and lines: experiments. Lines: Simulations at  $t_{\text{ox}} = 0.6\mu\text{m}$ ,  $t_{\text{ox}} = 0.9\mu\text{m}$  and  $t_{\text{ox}} = 15\mu\text{m}$ .

thickness is fairly captured by simulations in a wide range of thicknesses, indicating that impact ionization plays a relevant role in the breakdown of such devices.

In order to gain further insight on the mechanisms responsible of the breakdown, the electric field across the devices with thicknesses  $0.9\mu\text{m}$  and  $15\mu\text{m}$  has been extracted and is reported in Fig. 6(A-C) (dimensions not in scale) at the biases corresponding to the onset of the avalanche breakdown. Firstly, it should be noted that the electric field distribution of the thinner oxide (Fig. 6A) notably differs from that of the thicker oxide (Fig. 6C). The thinner oxide approximately behaves like a one-dimensional parallel-plate capacitor, with the electric field being smaller near the cathode, becoming greater moving towards the anode, reaching its maximum value in its proximity and rapidly laterally decreasing far from the top metal corner. The maximum field sustained by the thinner oxide at the onset of the avalanche breakdown is about  $E = 11\text{MV/cm}$  when an external nominal electric field  $E_{\text{ox}} = 9.4\text{MV/cm}$  is applied. The impact-ionization generation shows its maximum value at the corresponding maximum electric field (not shown). Avalanche is thus initiated by electrons flowing in the high field at the anode. The thicker oxide is characterized by having two electric field peaks: the first one is in the same position as the one of the thinner oxide, i.e., in the proximity of the anode (Fig. 6C), while the second one is close to the top metal corner, with the high-electric field profile extending over a wide region of the device. The cutlines in the longitudinal direction at the top side of the capacitance show that the second peak gives rise to a significant impact-ionization generation, leading to a large amount of current density 6(B-D).

As a consequence, the thickness dependence of the breakdown field is substantially modulated by the electric field profile in the proximity of the corner, the extension of

which is strongly dependent on the oxide thickness, which acts as a scaling parameter.

## 4. Conclusions

TCAD calculations have been proven to be a useful tool for the study of breakdown in back-end thick oxides characterized under DC-stress conditions. Simulations suggest that the impact-ionization generation is the dominant mechanism of the breakdown in capacitances with thicknesses from  $1\mu\text{m}$  to  $15\mu\text{m}$ . The effect of the 2D geometry has been analyzed nicely explaining the measured characteristics.

## References

- [1] C. C. Hung, A. S. Oates, H. C. Lin, P. Chang, J.L. Wang, C.C. Huang, and Y.W. Yau, *New understanding of Metal-Insulator-Metal (MIM) capacitor degradation behavior*, IEEE 45th Annual International Reliability Physics Symposium, Phoenix, AZ, USA, pp. 630-631, April 15-19, 2007. DOI: 10.1109/RELPHY.2007.369985.
- [2] P. Mahalingam, D. Guiling and S. Lee, *Manufacturing challenges and method of fabrication of on-chip capacitive digital isolators*, IEEE International Symposium on Semiconductor Manufacturing, Santa Clara, CA, USA, pp. 1-4, October 15-17, 2007. DOI: 10.1109/ISSM.2007.4446870.
- [3] R. Higgins and J. McPherson, *TDDDB Evaluations and Modeling of Very High-Voltage (10 KV) Capacitors*, IEEE 47th Annual International Reliability Physics Symposium, Montreal, QC, Canada, pp. 432-436, April 26-30, 2009. DOI: 10.1109/IRPS.2009.5173292.
- [4] J.W. McPherson, R.B. Khamankar, and A. Shanware, *Complementary model for intrinsic time-dependent dielectric breakdown in  $\text{SiO}_2$  dielectrics*, Journal of Applied Physics, Vol. 88, pp. 5351-5360, 2000. DOI: 10.1063/1.1318369.
- [5] J. W. McPherson, *On why dielectric breakdown strength reduces with dielectric thickness*, IEEE International Reliability Physics Symposium (IRPS), 2016, pp. 3A-3-1-3A-3-8. DOI: 10.1109/IRPS.2016.7574512.
- [6] S. Shin, Y.P. Chen, W. Ahn, H. Guo, B. Williams, J. West, T. Bonifield, D. Varghese, S. Krishnan, and M.A. Alam, *High Voltage Time-Dependent Dielectric Breakdown in Stacked Intermetal Dielectric*, IEEE 56th Annual International Reliability Physics Symposium, Burlingame, CA, USA, pp. P-GD.9-1-P-GD.9-5, March 11-15, 2018. DOI: 10.1109/IRPS.2018.8353669.
- [7] E.F. Runnion, S.M. Gladstone, R.S. Scott, D.J. Dumin, L. Lie, and J.C. Mitros, *Thickness Dependence of Stress-Induced Leakage Currents in Silicon Oxide*, IEEE Transactions On Electron Devices, Vol. 44, No. 6, pp. 993-1001, June 1997. DOI: 10.1109/16.585556.
- [8] F. Giuliano, S. Reggiani, E. Gnani, A. Gnudi, M. Rossetti, R. Depetro, G. Croce, *Novel TCAD Approach for the Investigation of Charge Transport in Thick Amorphous  $\text{SiO}_2$  Insulators*, IEEE Transactions on Electron Devices, Vol. 68, No. 11, pp. 5438-5447, 2021. DOI: 10.1109/TED.2021.3100309.
- [9] R. Degraeve, J. L. Ogier, R. Bellens, P. J. Roussel, G. Groeseneken and H. E. Maes, *A new model for the field dependence of intrinsic and extrinsic time-dependent dielectric breakdown*, IEEE Transactions on Electron Devices, Vol. 45, No. 2, pp. 472-481, 1998. DOI: 10.1109/16.658683.
- [10] K. Okada, K. Narita, M. Kamei, S. Ohno, Y. Ito and S. Suzuki, *Generalized model of dielectric breakdown for thick and thin  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$  films combining percolation model and constant- $\delta E$  model*, IEEE International Reliability Physics Symposium (IRPS), 2017, pp. 5B-2.1-5B-2.5. DOI: 10.1109/IRPS.2017.7936324.
- [11] D.N. Chen and Y.C. Cheng, *A new model for dielectric-breakdown phenomenon in silicon dioxide films*, Journal of Applied Physics 61, pp. 1592-1601, 1987. DOI: 10.1063/1.338096.
- [12] D.J. Di Maria, D. Arnold, E. Cartier, *Impact ionization, trap creation, degradation, and breakdown in silicon dioxide films on silicon*, Journal of Applied Physics 73, pp. 3367-3385, 1993. DOI: 10.1063/1.352936.
- [13] P. C. Arnett, *Transient conduction in insulators at high fields*, Journal of Applied Physics 46, pp. 5236-5243, 1975. DOI: 10.1063/1.321592.
- [14] J.F. Verwey, E.A. Amerasekera and J. Bisschop, *The physics of  $\text{SiO}_2$  layers*, Reports on Progress in Physics, Vol. 53, No. 10, pp. 1297-1331, 1990.
- [15] Synopsys Inc., Sentaurus Device User Guide S-2021.06, 2021.
- [16] D. Arnold, E. Cartier, and D. J. DiMaria, *Theory of high-field electron transport and impact ionization in silicon dioxide*, Physical Review B, Vol. 49, No. 15, pp. 10278-10297, Apr. 1994. DOI: 10.1103/PhysRevB.49.10278.
- [17] Y. Okuto, C.R. Crowell, *Threshold energy effect on avalanche breakdown voltage in semiconductor junctions*, Solid-State Electronics, Vol. 18, Issue 2, pp. 161-168, 1975. DOI: 10.1016/0038-1101(75)90099-4.
- [18] M. Sometani, R. Hasunuma, M. Ogino, H. Kuribayashi, Y. Sugahara and K. Yamabe, *Suppression of Leakage Current of Deposited  $\text{SiO}_2$  with Bandgap Increasing by High Temperature Annealing*, ECS Transactions, Vol. 19 (2), pp. 403-413, 2009. DOI: 10.1149/1.3122105.

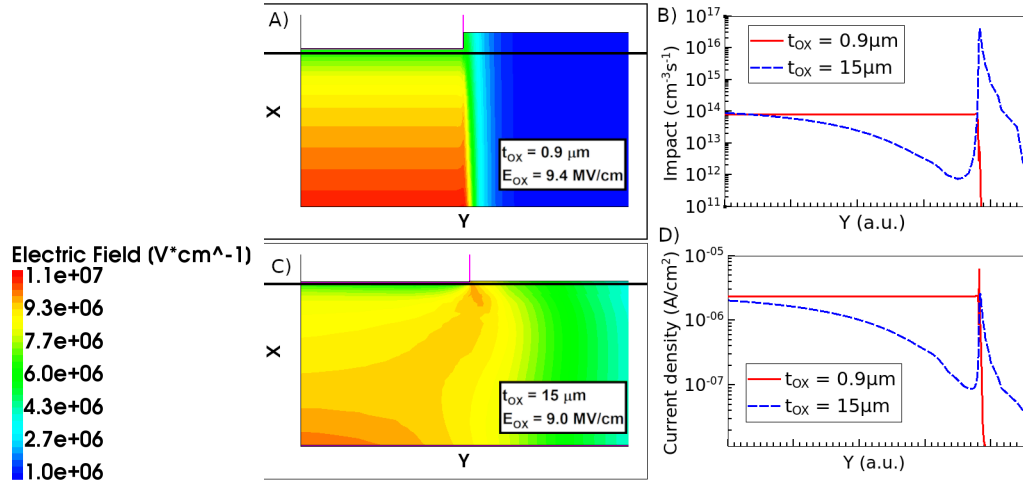


Figure 6: Electric field within the oxide layer for two thicknesses and cutlines of the impact-ionization generation rate and the current density along the Y axis (black lines in the leftmost figures).

A. Electric field distribution for  $t_{OX} = 0.9 \mu\text{m}$  at  $E_{OX} = 9.4 \text{ MV/cm}$  (onset of avalanche breakdown).

B. Impact-ionization generation rate along the Y coordinate in proximity of the top metal contact.

C. Electric field distribution for  $t_{OX} = 15 \mu\text{m}$  at  $E_{OX} = 9.0 \text{ MV/cm}$  (onset of avalanche breakdown).

D. Current density along the Y coordinate in proximity of the top metal contact.

X and Y axes have arbitrary units. The same scale is used on every X axis, while different scales have been used for the Y axes due to the different thicknesses. The distances from the two cutlines to the respective top metal contacts are the same. For the schematic of the structure, see Fig. 1.