Power-Efficient UHF Rectification for Long-Distance Wireless Power Transfer in Sensor Nodes

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Gabriele Marasca
ARCES
University of Bologna
Cesena, Italy
gabriele.marasca2@unibo.it

Rudi Paolo Paganelli
IEIIT
National Research Council
Bologna, Italy
rudipaolo.paganelli@cnr.it

Aldo Romani
ARCES
University of Bologna
Cesena, Italy
aldo.romani@unibo.it

***Abstract*—In the last decade, the development and the implementation of smart and ubiquitous sensors in various fields of interest has opened several issues about the life cycle of these devices and the disposal or replacement of their batteries. One potential solution can be found in wireless power transfer and in radio-frequency (RF) Energy Harvesting, which enables devices to be powered up to several meters from a RF source. This study proposes the optimization of an UHF rectifier operating at 868 MHz, and investigates the effects of the main parasitic elements of its implementation, like printed circuit board (PCB) metal traces and the package of lumped elements. Furthermore, an optimization method for matching network design, composed of two specific harmonic balance simulations, is described: in the first one, ideal matching network components are used in order to improve simulation time; in the second, S-parameters provided by manufacturers are used. Finally, a PCB prototype is characterized, producing 4.56 µW of rectified power, with 36.3% RF-to-DC conversion efficiency and 278 mV in optimum load conditions, with a -19 dBm harmonic input signal at 868 MHz. An estimate of output power over distance is reported in order to evaluate the maximum operative distance of potential commercial devices, like micro-power management integrated circuits.**

***Keywords*—energy harvesting, wireless power transfer, rectifier**

I. Introduction

In recent years, there has been a significant increase in the utilization of Internet of Things (IoT) devices, particularly smart sensors, reflecting an exponential growth trend. The recent surge in the use of these devices has led to scientific discussions about their lifecycle and maintenance. Energy Harvesting (EH) is a promising solution to address these concerns by eliminating the reliance on batteries to power such systems.

In this scenario, radio-frequency (RF) EH and wireless power transfer (WPT) play a key role in obtaining simple and cost-effective wirelessly-powered devices. Antennas are easily implemented on the same substrates and technology of conventional printed circuit boards (PCBs) hosting system electronics, with no need to purchase expensive or exotic energy harvesting transducers. The non-idealities of the components used in RF-to-DC converters produce in general relevant losses [1]. Indeed, practical implementations face relevant challenges due to the use of real diodes and the need to account for substrate losses, as well as for parasitics of passive components, which makes it unfeasible to achieve ideal results. It is important to note that efficiency decreases as the received RF power decreases due to the intrinsic non-linearity of rectification, which is a particularly relevant point in real-world scenarios where available powers may be quite low, e.g. at distances of several meters from the power source, the received power can be comparable to or below a few microwatts. Various methodologies have been proposed in existing literature to address these challenges and mitigate losses to enhance efficiency, including the enhancement of substrates to reduce losses in distributed matching networks in one [2], or more [3] bands of interests and also for wide bandwidth rectification for EH purposes [4]. An alternative to mitigate the losses introduced by the implementation of the matching network, is to avoid it by using a high-impedance antenna for direct impedance matching [5], which, however, implies a loss of a degree of freedom in the design. Although their potential, these approaches lead to increased production costs, due to the use of expensive substrates or the creation of custom antennas designed for a specific system.

The aim of this study is to present an approach based on the use of commercial off-the-shelf (COTS) lumped components to model and implement both matching networks and rectifier using output power and overall efficiency, including input impedance matching [3], [4], as the parameter to be optimized. The circuit is designed to interface with a generic 50 Ω impedance antenna. The use of lumped

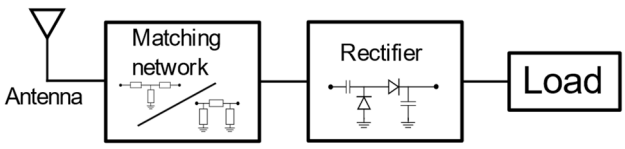

Fig. 1. Block diagram of the system presented in this work. The load represents any current-sinking device connected to the output of the rectifier.

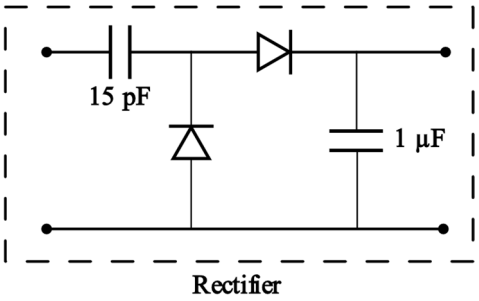

Fig. 2. Schematic of the voltage doubler rectifier. The DC-current component developed on the antiphase conducting diodes can only flow in the loop involving the output load (not shown in the figure).

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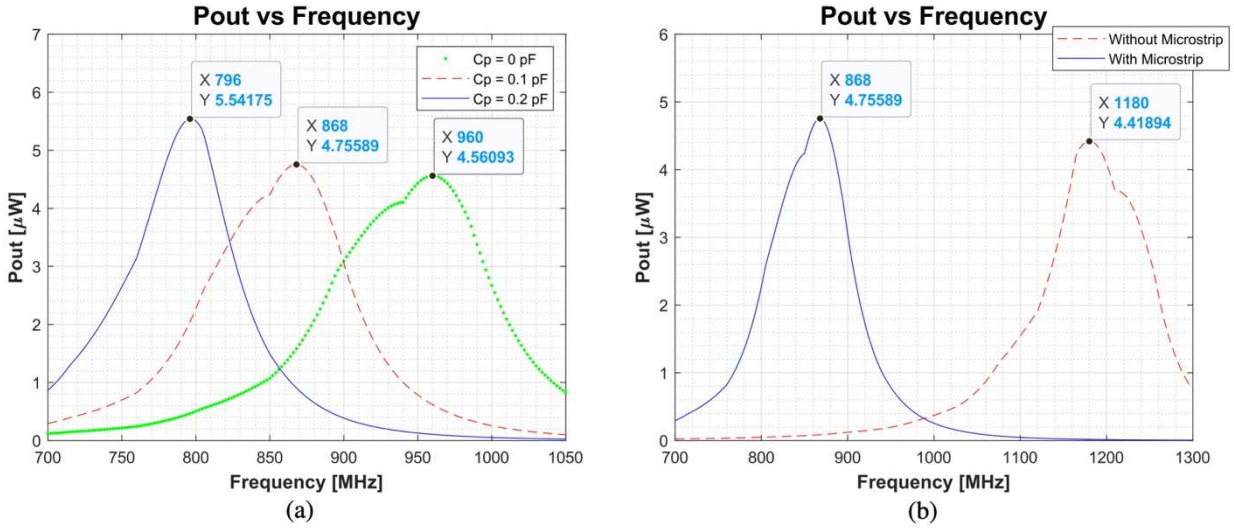

Fig. 3. Simulation results of output power (P_{out}) over frequency with an antenna delivering a power of -19 dBm, and a T matching network with three inductors (12 nH for the first one in series, 11 nH for the shunt inductor, and 22 nH for the last one in series): (a) with different hypothetic values of package capacitance (C_P) for the SMS7630-040LF diode; (b) with and without microstrip elements used to account for PCB metal traces.

components requires to consider during the design phase component tolerances and parasitic effects introduced by component packages. This paper pays special attention to modelling the effects of parasitics at different levels, like the packages of components and the effects introduced by metal lines on the PCB. Furthermore, design achieves state-of-the-art performances in reference conditions corresponding to extremely low received power in the order of a few microwatts.

Table I compares various studies, focusing on power conversion efficiency (PCE) and output voltage (V_{out}) values, measured at specific levels of available power (P_{av}) at the antenna output port. The table also includes information on the frequency and substrate used. It is important to note that all studies utilize a voltage doubler as a rectifier except for [6] and [7]. However, they represent various implementations of matching networks, including matching networks with distributed elements [6], [8], high impedance antennas without matching networks [5], lumped elements [3], and both distributed and lumped elements [7], [9]. As shown in Table I, the prototype produced using the design method discussed in this work provides state of the art values for both efficiency and output voltage for the input power considered.

TABLE I. STATE OF ART

Ref.	P_{av}	PCE	V_{out}	Frequency	Substrate
[2]	-19 dBm	28%*	~260 mV*	868 MHz	Rogers RO4350B
[3]	-20 dBm	28%*	N.A.	915 MHz	RT/duroid 5880
[5]	-20 dBm	43%	~200 mV*	845 MHz*	Polyimide
[6]	-20 dBm	19%*	~130 mV*	868 MHz	FR4
[7]	-20 dBm	15%*	N.A.	850 MHz	PET
[8]	-20 dBm	32%	186 mV	888.7 MHz	Rogers RO4350
[9]	-19 dBm	29%*	~200 mV*	915 MHz	Rogers 4003C
This work	-19 dBm	36.3%	278 mV	868 MHz	FR4

* values inferred from plots included in the works

II. SYSTEM DESIGN

Powering a battery-less ultra-low power system is a challenging task due to the limited power available and to the low voltages obtained at the receiver side, which can typically be in the range of a few hundred millivolts at distances of several meters from the source. Since a DC/DC will be still required at the output of the rectifier, which requires a minimum activation voltage to cold start and to operate, and since in power-constrained scenarios it is still necessary to maintain a fair PCE of the rectifier, we decided to use a voltage doubler rectifier, which may still result in a possibly lower efficiency with respect to a single diode configuration, but provides a higher output voltage, as typically required by power management circuits interfacing with the load, i.e. the sensor node. Cockcroft-Walton voltage multipliers may provide higher output voltages, although they are associated with increased power losses due to the effects on every stage of the intrinsic threshold voltage of rectifier diodes as shown in [10]. Therefore, in this work, two stages were deemed a reasonable trade-off.

Fig. 1 depicts the typical configuration, where a matching network interfaces the UHF antenna to the rectifier circuit, which drives a load. Providing an optimum matching, which is a linear concept, to an intrinsically non-linear rectifier is a non-trivial problem. For the matching network, we considered both T and π configurations during the optimization process to determine which one provides the highest PCE. The load in Fig.1 represents a generic current-sinking device, e.g. measurement instrumentation, or a micro-power management circuit to supply a sensor node, etc.

III. MATCHING NETWORK OPTIMIZATION

A rectifier is a highly non-linear component, which makes it impossible to identify a matching network suitable for every usage scenario and power level. Therefore, in this work, we assume, for the purpose of optimization, a working frequency of 868 MHz and an input power of -19 dBm (12.589 µW). For each configuration, we determined the optimal value for the load resistance.

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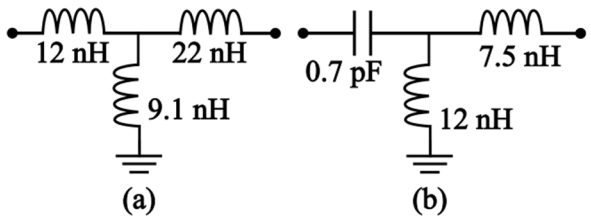

Fig. 4. The proposed matching networks and the identified values of the passive components: (a) inductive matching network; (b) mixed capacitive-inductive matching network.

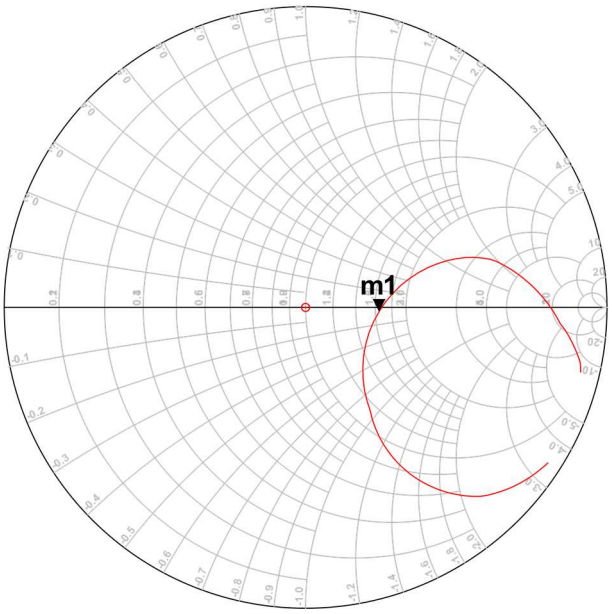

Fig.5. Impedance of the system implementing the matching network shown in Fig. 4(b), equal to 82.2 -j2.4 Ω at the marker m1, pointed in 868 MHz. This simulation is obtained with the S2P files of the components and all the considered parasitics, sweeping frequency from 750 MHz to 1 GHz.

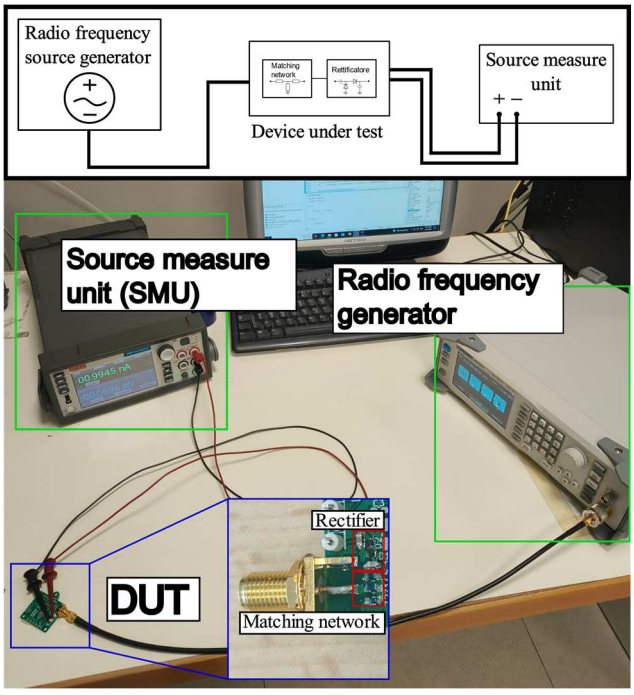

Fig.6. Experimental setup and zoom on device under test.

It is possible to create a model using various simulations, like Large Signal S-Parameter (LSSP) [3] and Harmonic Balance (HB) [2]; in this work the HB method was used, which is seen to ensure accurate results. Furthermore, the optimization parameter used to design the matching network was the output power. This helps to consider all the peculiarities of the circuit jointly, and to find the best compromise between them, like the antenna matching, the losses on the parasitics, and the conversion efficiency on the diodes by choosing the equivalent load resistance.

In this work, the voltage doubler is implemented using SMS7630-040LF low-barrier Schottky diodes [11], with a series capacitance of 15 pF and a shunt capacitance of 1 µF, as shown in Fig. 2. To design an appropriate matching network, an accurate estimation of the parasitic components is essential. This includes consideration of the package of the diodes, the components of the matching network, and the effects of metal traces on the PCB, as shown in [12]. For the lumped components, we used the S-parameters for capacitors and inductors, and the Spice models for diodes, as provided by their manufacturers. In order to minimize parasitics we opted for the SOD-882 package; however, literature reports different capacitance values associated with the diode packages. As shown in Fig. 3(a), this variability has a significant impact on the operating frequency of the system, raising some concerns on sensitivity and reproducibility of the circuit. Indeed, even a difference of 0.1 pF in the model capacitances of diode package has a strong effect on the system in terms of frequency shift because of the high-quality factor of the node (Q_n) of the proposed impedance T-matching network: Q_n is defined as the ratio of the imaginary over the real part of the impedance seen at the node and is an indicator both of the network sensitivity and of the achievable matching band. Then, to take into account all the parasitic contributions, we decided to model the effects of the metal traces with microstrip elements. Although the length of such microstrips can be considered negligible at the considered frequencies, they still better refine the parasitic contributions introduced by the PCB on those critical RF nodes. Fig. 3(b) shows the effect on the frequency response of the system generated by the decision of not including microstrip elements between components.

The optimization phase was performed with two main simulation activities: in the first one, the matching network components were considered ideal. By sweeping parameters with sufficiently fine steps, all values of the matching network components were varied to obtain an optimal matching network, i.e., maximizing the output power, measured over the optimum value of load resistance, found by a further sweeping of this parameter. In this part, package parasitics were ignored, aiming at faster simulations. In this initial phase, it is crucial to consider the tolerances associated with the components and the network sensitivities. If the system is overly selective due to unfeasible high-step impedance transformations, tolerances can cause the system to deviate from the frequency band of interest. In the second simulation, the ideal components identified in the previous simulation were replaced by the S-parameters of COTS components provided by the manufacturers to account for parasitic effects. This step is mandatory, because the system requires further tuning due to the parasitic elements, and also because available commercial components with reduced tolerances have to be used. It is preferable to use the S-parameters for the fixed series capacitor of the voltage doubler from the first

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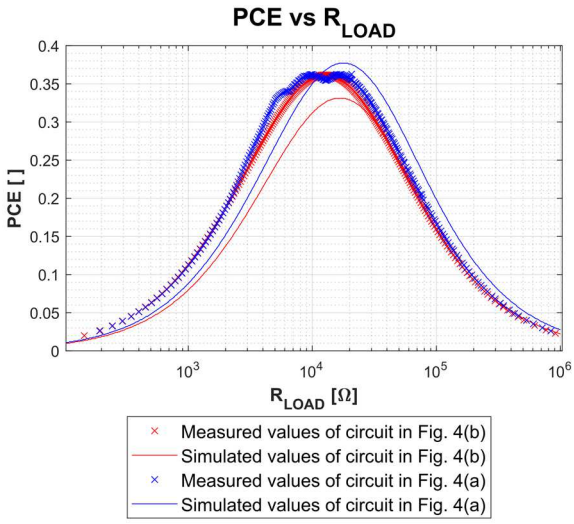

Fig.7. Simulated and measured values of PCE over R_{LOAD} for circuit with matching network in Fig. 4(b) in red and 4(a) in blue.

phase. This allows its parasitic elements to be properly taken into account, thus reducing the tuning required in the second phase.

The above optimization method allows the identification of various matching networks, with a particular focus on T matching networks, respectively with three inductors, and a series capacitance with two inductors, as shown in Fig. 4(a) and Fig. 4(b). Fig. 5 shows the Smith chart showing the degree of matching provided by the configuration in Fig. 4(a).

IV. Experimental Results

To validate the model, two PCB prototypes (FR4 substrate, 1.6 mm overall board thickness, 35 µm copper thickness) were assembled and characterized with the previous matching networks, with the experimental setup is shown in Fig. 6. For characterization purposes, a RF signal generator was used to generate a sinusoidal tone with fixed power and frequency. The attenuation introduced by the cable used to connect the generator to the device under test (DUT) was experimentally measured to be 1.5 dB. This attenuation was compensated when setting the output power of the RF generator. To measure the output power, a Source Measure Unit (SMU) was used. The SMU acts as a variable load that can set the output voltage and at the same time measure the current at the load side. It is then easy to determine the static power transfer characteristics as a function of load conditions. However, it is possible to translate the above load conditions into equivalent load resistances associated to every measurement. In fact, a SMU does not use a fixed load resistance in the measurement process. Therefore, the reported data refers to the optimum load resistance value for the operating frequency of 868 MHz, as identified in the maximum power point by the HB simulation with constant input power of -19 dBm and sweeping load resistance value. This optimum resistance value is confirmed by the experimental data obtained, shown in Fig. 7. With this configuration, two characterizations were made to evaluate PCE: the output power measured by sweeping frequency with a constant value of input power of -19 dBm, and a sweep in input power at a constant frequency of 868 MHz.

Fig. 8 reports simulated and measured output power levels. Data refer to load resistances of 17 kΩ and 15 kΩ for the circuits implementing the matching networks reported in Fig. 4(a) and Fig. 4(b), respectively.

The first characterization, as shown in Fig. 8(a), achieves up to 4.64 µW at 864 MHz, with a bandwidth of 77 MHz (from 820 MHz to 897 MHz), with a rectified power of 4.56 µW at 868 MHz for the DUT with the matching network of Fig. 4(a). The same figure also reports the characterization of the DUT with the matching network of Fig. 4(b), which achieves up to 4.5 µW at 868 MHz, with a bandwidth of 93 MHz (from 809 MHz to 902 MHz).

The second characterization, as shown in Fig. 8(b), reports the efficiency and the output voltage measured for both circuits, with a focus on –19 dBm. PCE increase with P_{av} for various dBm over the target, showing the diode's conversion efficiency increasing, while input matching gracefully deteriorates, giving still overall better PCE, but not the optimal one that occours for P_{av} of -19 dBm. At this power level, the prototype implementing the matching network illustrated in Fig. 4(a) achieves an efficiency of 36.26% and a V_{out} of 278 mV. At the same power, the prototype with the matching network shown in Fig. 4(b) achieves 35.98% with a V_{out} of 260 mV. A comparison of the achieved performance with other relevant works is reported in Table I.

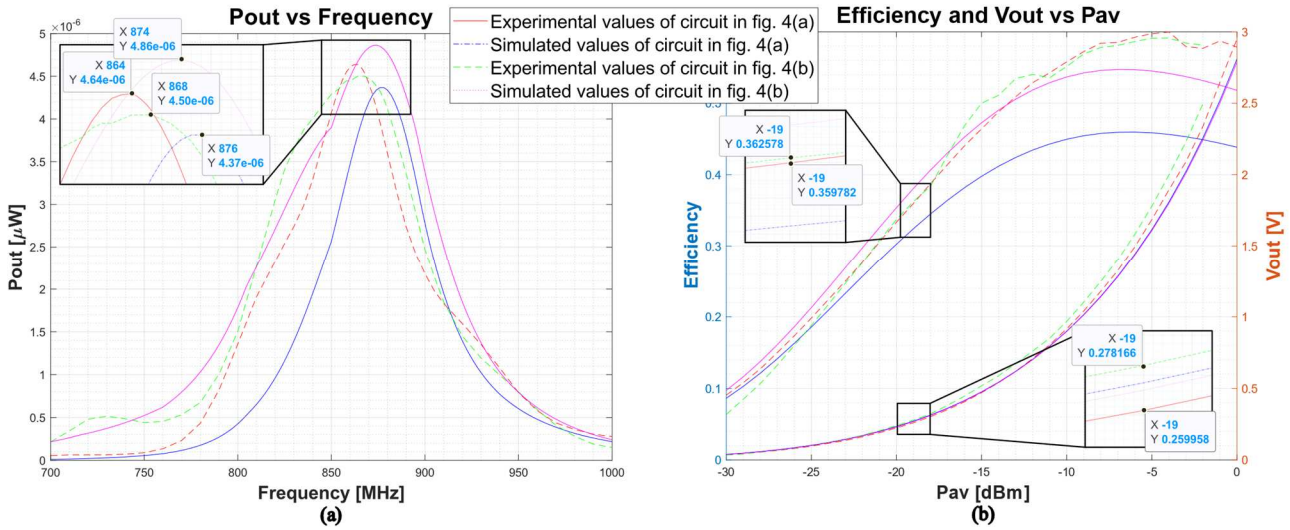

Fig. 8. Simulated and measured values of: (a) rectifier otuput power for frequencies ranging from 700 to 1000 MHz for the matching networks of Fig. 4; (b) power conversion efficiency and output voltage V_{out} for input power levels ranging from –30 dBm to 0 dBm. Zoomed views of zones of interest are shown.

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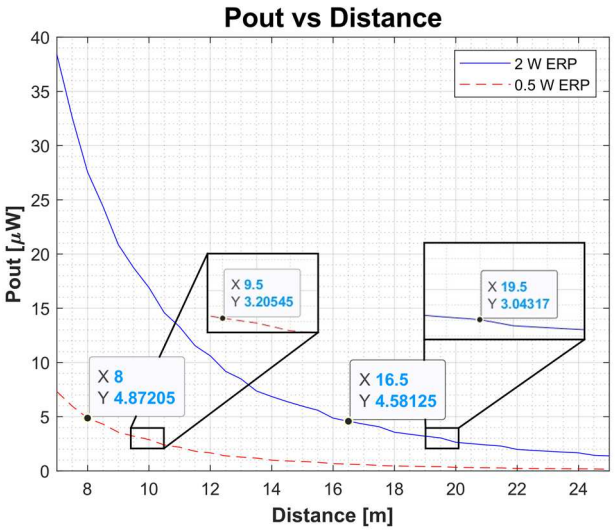

Fig. 9. Simulated rectifier output power as a function of distance for different values of effective radiated power (ERP).

In order to evaluate reproducibility of results, three additional prototypes of the circuit with the matching network shown in Fig. 4(a) were characterized. For the frequency of interest of 868 MHz, the highest rectified power is the one reported above, while the lowest is equal to 4.18 μW, with the corresponding efficiencies ranging from 36.3% to 33.2%. However, a rectified power of 4.71 μW was also measured at 850 MHz, corresponding to an efficiency of 37.8%.

V. Discussion

With this work, a cost-effective power-efficient rectifier is proposed. In the adopted approach, particular attention was paid to some relevant aspects. Firstly, it is necessary to consider the tolerance of the components, which can be mitigated by using low-tolerance COTS. Secondly, the use of microstrip elements to model PCB copper traces has lower intrinsic accuracy with respect to an electromagnetic simulation. However, the adopted approach provided fast simulation times, allowing the design of a lumped component matching network achieving high efficiency at ultra-low power. Lumped elements allow for a significant reduction in circuit dimensions compared to a distributed UHF design.

Based on the measured results, it appears feasible to power a sensor system with this RF energy harvesting front-end, by using a DC/DC converter. In fact, recent ultra-low power DC/DC converters like [13], can perform cold start with just a few μW with a voltage below 300 mV, and emulate the optimum load. Compatible values can be achieved by the rectifier presented in this work at the considered input power of -19 dBm, with COTS and on a lossy FR4 substrate. Furthermore, the estimated output power of the rectifier over distance can be estimated according to (1), as explained in [2] and shown in Fig. 9, using simulated data for Friis equation and previously measured data for $\eta_{RF\text{-}DC}$ from -30 to 0 dBm:

$$P_{out} = P_{TX} G_{TX} G_{RX} \left(\frac{\lambda}{4\pi D}\right)^2 \eta_{RF-DC} \qquad (1)$$

where P_{TX} is the transmitter power, G_{TX} is and G_{RX} are, respectively, the gain of the transmitting and receiving antennas, λ is the wavelength, D is the distance from the source and the receiver, and $\eta_{RF\text{-}DC}$ is defined according to (2):

$$\eta_{RF-DC} = \frac{V_{out} \cdot I_{out}}{P_{av}} , \qquad (2)$$

where V_{out} and I_{out} are, respectively, the voltage and current at the output port of rectifier, and P_{av} is the available power at the output port of the antenna. In the band of interest (865-868 MHz), in some channels $P_{TX}\,G_{TX}$ can be set to 2 W of Effective Radiated Power (ERP) in Europe, i.e. for radio Frequency identification (RFID) systems, or generally to 0.5 W ERP. Both cases are reported in Fig. 9 where, for G_{RX}, an omni-directional antenna with a peak gain of 3.6 dBi [14] was considered for the simulation. A value of P_{av} of -19 dBm was considered, which corresponds to distances of 16.5 m and 8m respectively from a 2 W ERP and a 0.5 W source. Furthermore, with a 2 W ERP transmitted power, the power required to cold start for a micro-power management integrated circuit [13], can be collected at a distance of 19.5 m, and at 9.5 m with 0.5 W ERP.

VI. Conclusions

The described design approach allowed to optimize the matching network and achieve efficiencies in line with the state of art on standard FR4 substrates. The rectifier is designed to operate in the 865-868 MHz band, because of the generally higher allowed power, which offers favorable conditions for increased distance of effective wireless power transfer. At the reference input power of -19 dBm, an output power in the order of 4.56 μW was measured at 868 MHz, along with a voltage of 278 mV on an optimum load. As discussed in Section V this is sufficient to cold start recent power management integrated circuits at several meters of distance from UHF sources compliant with regulation for the ISM (Industrial, Scientific, and Medical) band. Possible applications include wirelessly powered and battery-less sensors and dataloggers, activated on-demand. In this power-constrained scenario, energy-efficient back-scattering communications may also be implemented at node level, to achieve compatibility with RFID protocols, e.g. EPC GEN2, and add advanced functionalities for industrial applications like asset tracking and environmental monitoring.

References

[1] R. J. Gutmann and J. M. Borrego, "Power Combining in an Array of Microwave Power Rectifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 27, no. 12, pp. 958–968, Dec. 1979, doi: 10.1109/TMTT.1979.1129774.

[2] M. Pizzotti *et al.*, "A Long-Distance RF-Powered Sensor Node with Adaptive Power Management for IoT Applications," *Sensors*, vol. 17, no. 8, Art. no. 8, Aug. 2017, doi: 10.3390/s17081732.

[3] C. Song *et al.*, "A Novel Six-Band Dual CP Rectenna Using Improved Impedance Matching Technique for Ambient RF Energy Harvesting," *IEEE Trans. Antennas Propag.*, vol. 64, no. 7, pp. 3160–3171, Jul. 2016, doi: 10.1109/TAP.2016.2565697.

[4] W. Liu, K. Huang, T. Wang, J. Hou, and Z. Zhang, "A Compact High-Efficiency RF Rectifier With Widen Bandwidth," *IEEE Microw. Wirel. Compon. Lett.*, vol. 32, no. 1, pp. 84–87, Jan. 2022, doi: 10.1109/LMWC.2021.3115106.

[5] M. Wagih, A. S. Weddell, and S. Beeby, "High-Efficiency Sub-1 GHz Flexible Compact Rectenna based on Parametric Antenna-Rectifier Co-Design," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, Aug. 2020, pp. 1066–1069. doi: 10.1109/IMS30576.2020.9223796.

[6] S. D. Assimonis, S.-N. Daskalakis, and A. Bletsas, "Efficient RF harvesting for low-power input with low-cost lossy substrate rectenna grid," in *2014 IEEE RFID Technology and Applications Conference (RFID-TA)*, Sep. 2014, pp. 1–6. doi: 10.1109/RFID-TA.2014.6934190.

[7] A. Collado and A. Georgiadis, "Conformal Hybrid Solar and Electromagnetic (EM) Energy Harvesting Rectenna," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 60, no. 8, pp. 2225–2234, Aug. 2013, doi: 10.1109/TCSI.2013.2239154.

[8] J. Argote-Aguilar *et al.*, “Low-input-power Sub-GHz RF Energy Harvester for Powering Ultra-low-power Devices,” in *2023 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC)*, Nov. 2023, pp. 1–4. doi: 10.1109/INMMIC57329.2023.10321785.
[9] A. Nadeem *et al.*, “UHF IoT Humidity and Temperature Sensor for Smart Agriculture Applications Powered from an Energy Harvesting System,” in *2022 IEEE International Conference on Internet of Things and Intelligence Systems (IoTaIS)*, Nov. 2022, pp. 186–190. doi: 10.1109/IoTaIS56727.2022.9975982.
[10] A. Costanzo *et al.*, “Energy Autonomous UWB Localization,” *IEEE J. Radio Freq. Identif.*, vol. 1, no. 3, pp. 228–244, Sep. 2017, doi: 10.1109/JRFID.2018.2792538.
[11] Skyworks, “Surface-Mount Mixer and Detector Schottky Diodes,” 200041AG datasheet, Mar. 2021.
[12] Skyworks, Appl. Note APN1014, Apr. 2014.
[13] e-peas, “Highly Versatile, Regulated Single-Output, Buck-Boost Ambient Energy Manager For AC/DC Sources”, AEM30330 datasheet, Jan. 2021 [Revised Feb. 2024].
[14] TE Connectivity, ANT-868-CW-RCS-xxx datasheet, Jan. 2015.

This is the accepted manuscript of: G. Marasca, R. P. Paganelli and A. Romani, "Power-Efficient UHF Rectification for Long-Distance Wireless Power Transfer in Sensor Nodes," 2024 IEEE Sensors Applications Symposium (SAS), Naples, Italy, 2024, pp. 1-6, doi: 10.1109/SAS60918.2024.10636357