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# Role of interface/border traps on the threshold voltage instability of SiC power transistors

V. Volosov<sup>1</sup>, S. Cascino<sup>2</sup>, M. Saggio<sup>2</sup>, A. Imbruglia<sup>2</sup>, F. Di Giovanni<sup>2</sup>, C. Fiegna<sup>1</sup>, E. Sangiorgi<sup>1</sup>, A.N. Tallarico<sup>1</sup>

<sup>1</sup>ARCES-DEI, University of Bologna, Campus of Cesena, 47521, Cesena, Italy

<sup>2</sup>STMicroelectronics, SRL, Stradale Primosole 50, 95121, Catania, Italy

Corresponding author: vladislav.volosov2@unibo.it

## Abstract

In this paper the role of interface/border defects on the threshold voltage drift ( $\Delta V_{TH}$ ) of SiC power MOSFETs has been investigated by means of slow and fast positive bias temperature instability (PBTI), hysteresis and conductance tests. Results have shown an opposite temperature (T) dependency based on the level of the applied gate bias ( $V_G$ ) and on the adopted stress technique. With  $V_G > 30$  V and a slow-PBTI procedure, the creation of new oxide defects and/or the charge trapping in deep states occurs, showing a positive T-dependency. On the contrary, with a lower  $V_G$  and a fast-PBTI test, the  $\Delta V_{TH}$  shows a negative T-dependency, associated to dominant role of pre-existing interface and/or border traps.

## Keywords

SiC MOSFET, threshold voltage instability, hysteresis, interface/border traps, conductance, TCAD simulation.

## Introduction

Silicon carbide (SiC) technology features several advantages with respect to its Silicon (Si) competitor, e.g., higher operating voltages, safer operating temperatures and higher switching frequencies. This set of features gives rise to power devices with a better trade-off between performance and robustness, ensuring their widespread application in power electronics [1].

However, from reliability stand point, it is not as stable as Si counterpart. Numerous papers have reported that SiC devices exhibit higher threshold voltage ( $V_{TH}$ ) instability and faster  $V_{TH}$  recovery effects than Si-based devices [2-4], mainly ascribed to SiC/SiO<sub>2</sub> interface defects [5].

In [6], the  $\Delta V_{TH}$  under gate bias stress has been ascribed to two separate trapping mechanisms: i) near-interface (also referred as border) oxide charge trapping due to tunneling mechanisms from SiC semiconductor [7]; ii) charge trapping in intrinsic defects at the SiO<sub>2</sub>/SiC interface.

In [8], the adoption of slow test procedures has shown that the change in  $V_{TH}$  can be associated to capture/release of charge carriers to/from border traps, reporting, however, a significant  $V_{TH}$  recovery when a fast measurement is adopted. In addition, the  $V_{TH}$  shift decreases by increasing the temperature (T), indicating that electron emission from traps is temperature activated. Accordingly, a T-dependent

$V_{TH}$  recovery, i.e. faster by increasing T, has been reported also in [9].

Finally, the role of the border traps on the  $V_{TH}$  instability/hysteresis has been modeled in [10] and [11] by adopting a two-stage and a four-stage non-radiative multi-phonon model, respectively.

Overall, the adoption of a proper test procedure to evaluate the  $V_{TH}$  instability and the characterization/modeling of interface/border defects is of paramount importance to fully exploit the potential of SiC-based technology.

In this work, the  $\Delta V_{TH}$  induced by different PBTI test procedures (slow and fast) has been investigated, highlighting two opposite temperature dependencies. Moreover, interface defects have been characterized by means of conductance method and their effect has been modeled by TCAD simulator, qualitatively reproducing the  $V_{TH}$  hysteresis.

## Results and Discussion

SiC power MOSFETs fabricated by STMicroelectronics for automotive applications [12], with a class voltage of 650 V and a typical  $V_{TH}$  of 3.2 V, have been adopted for this investigation.

First, slow PBTI tests were conducted according to JEDEC JEP184 standard [13], which consists in a measure-stress-measure technique, adopting a conditioning procedure to stabilize the  $V_{TH}$  readout, thus ensuring the same charging state of the interface traps during the characterization phases. With this approach, a full  $I_D$ - $V_G$  measurements are carried out, hence the interface trap density ( $\Delta D_{it}$ ) can be calculated from subthreshold slope [14] as follows:

$$\Delta D_{it} = \frac{C_{ox}}{\ln(10) \cdot q \cdot k \cdot T} \cdot (S_i - S_0) \quad (1)$$

where  $C_{ox}$ ,  $q$ ,  $k$ ,  $T$  and  $S$  are the gate oxide capacitance per unit of area, the elementary charge, the Boltzmann's constant, the temperature and the sub-threshold swing ( $1/slope$ ), respectively.

The  $\Delta V_{TH}$  at different temperatures in the case of  $V_G = 20$  V and 35 V, measured by means of slow PBTI test is reported in Fig. 1. In both cases, it is mainly ascribed to charge trapping in the oxide, since, as reported in Fig. 2, the interface trap density, calculated from subthreshold slope (1), is negligible during the stress. Once excluded the role of  $D_{it}$ , the oxide trap density can be calculated as follows:

$$\Delta N_{ox} = \frac{C_{ox} \cdot \Delta V_{TH}}{q} \quad (2)$$

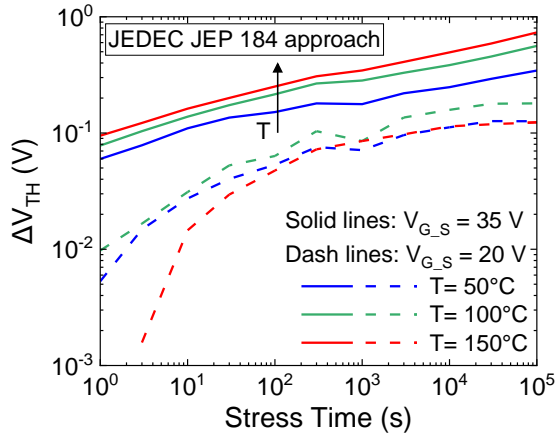


Fig. 1:  $\Delta V_{TH}$  during the stress time as a function of different temperatures and  $V_{G,S}$ , monitored by slow-PBTI technique.

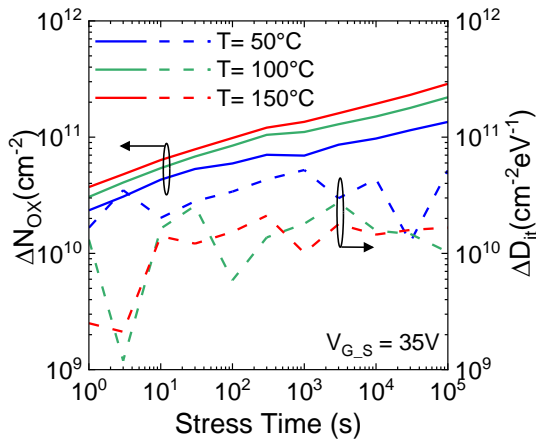


Fig. 2:  $\Delta N_{OX}$  (Solid lines) and  $\Delta D_{it}$  (Dash lines) calculated from  $\Delta V_{TH}$  and subthreshold slope, respectively, in the case of slow-PBTI test.  $D_{it}$  refers only to slow interface states.

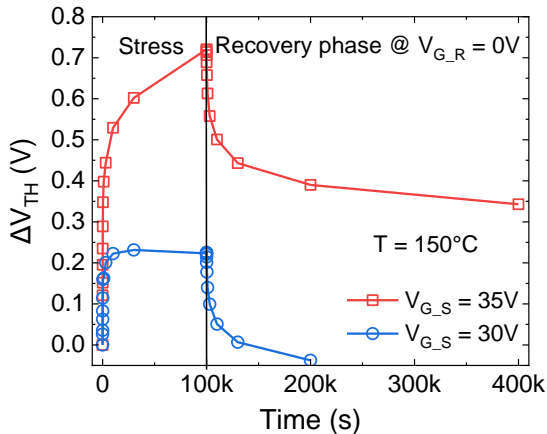


Fig. 3:  $\Delta V_{TH}$  during the stress and recovery time as a function of different  $V_G$ , monitored by slow-PBTI technique. Recovery condition:  $V_G = 0V$ ,  $T = 150^\circ C$ .

By observing Fig. 1, a clear and positive temperature trend is reported only in the case of  $V_G = 35 V$ . By applying such a high  $V_G$ , the creation of new oxide defects or the charge trapping in deep states may occur, exhibiting the usual positive

temperature dependency observed also in the case of Si-based devices. This is strengthened by Fig. 3, where a permanent or slowly recoverable  $\Delta V_{TH}$  is observed after a stress at  $V_G = 35 V$ , despite a  $\sim 83$  hours long recovery at  $150^\circ C$ . Vice versa, when a lower  $V_G$  stress is applied ( $30 V$ ), the  $\Delta V_{TH}$  is completely recovered after few hours.

In order to investigate the fast charge trapping/de-trapping mechanisms associated to interface/border defects, the fast PBTI procedure has been performed. In this case, only a portion of the  $I_D$ - $V_G$  transfer-characteristic (from  $1 V$  to  $4 V$ ) is measured during the characterization phase and the  $V_{TH}$  readout takes just a few  $\mu s$ , limiting, as much as possible, fast recovery mechanisms.

Fig. 4 shows  $\Delta V_{TH}$  as a function of temperature in the case of  $V_G = 10 V$  and adopting the Fast PBTI test. The relatively low  $V_G$  was limited by instrument compliance (Keysight B1530A). From Fig. 4, it is possible to notice two aspects: i) although the applied  $V_G$  stress is lower than the one adopted in the case of slow PBTI (Fig. 1), the observed  $\Delta V_{TH}$  is larger. The latter is completely recoverable in a few seconds as reported in Fig. 5; ii) a negative temperature dependency shows up.

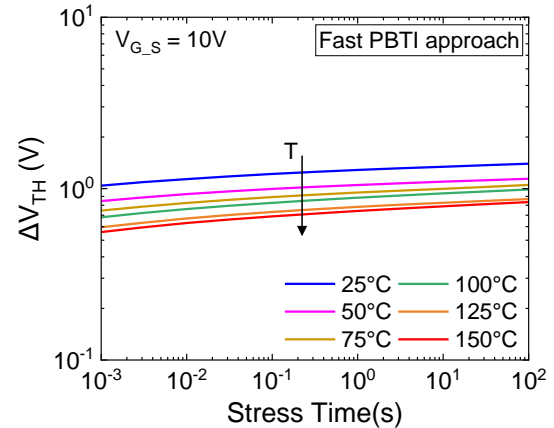


Fig. 4:  $\Delta V_{TH}$  during the stress time as a function of different temperatures, monitored by fast-PBTI technique. Contribution of fast interface/border traps is included.

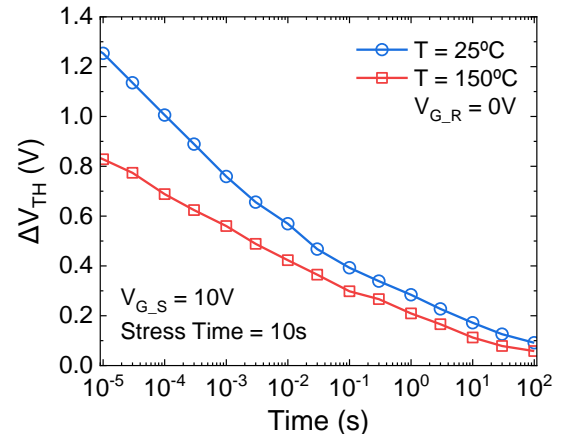


Fig. 5:  $\Delta V_{TH}$  during the recovery after  $10 s$  of stress with  $V_G = 10 V$  in the case of  $T = 25^\circ C$  and  $T = 150^\circ C$ .

By combining such aspects, a dominant role of charge trapping in pre-existing interface and/or border traps is suggested. On one hand, a faster characterization phase allows the evaluation of the  $\Delta V_{TH}$  induced by (fast) defects with short capture and emission time (from  $\mu\text{s}$  to  $\text{ms}$ ), thus obtaining a larger  $\Delta V_{TH}$ . On the other hand, the higher temperature induces a faster recovery mechanism, showing up a negative temperature dependency. A similar T-dependency has been reported in [9] and [10] for interface and border traps, respectively.

To confirm the presence of fast interface/border traps, hysteresis measurements have been carried out

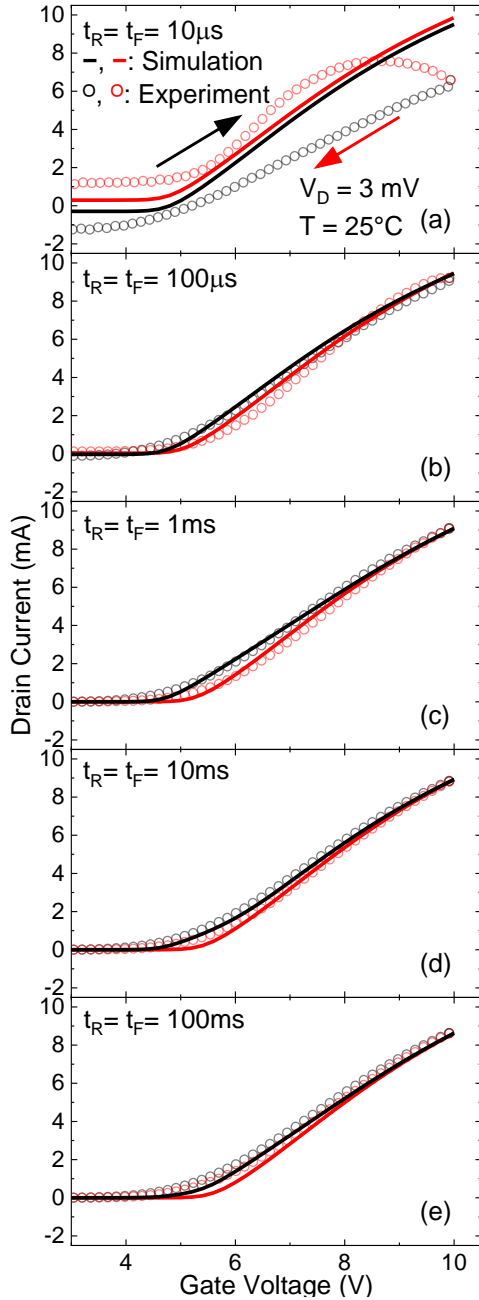


Fig. 6: Measured (symbols) and simulated (lines)  $I_D V_G$  characteristics with related  $V_{TH}$  hysteresis under different sweeping rates. From 0 V to 10 V in (a) 10  $\mu\text{s}$ , (b) 100  $\mu\text{s}$ , (c) 1 ms, (d) 10 ms, and (e) 100 ms.

at 25°C by adopting different sweeping rates. In particular,  $V_G$  was swept from 0 V to 10 V and back to 0 V with sweeping times ranging from 10  $\mu\text{s}$  to 100 ms, while  $V_D$  was kept constant.

The experimental  $I_D V_G$  and related hysteresis are reported in Fig. 6 (symbols). The  $V_{TH}$  hysteresis, although quite limited, confirms the presence of fast interface defects. It is worth noting that the negative  $V_{TH}$  hysteresis observed in the case of 10  $\mu\text{s}$  sweep time is an artifact of the measurement. In particular, since the drain voltage ( $V_D$ ) was limited due to current compliance of the instrument, the related current was affected by the displacement gate current of the large-area device.

The conductance method has been adopted to measure the interface trap density ( $D_{it}$ ). It is based on measuring the equivalent parallel conductance ( $G_p$ ) of a MOS structure, representing the loss mechanism due to interface trap capture and emission of carriers [14]. In particular, by considering traps with energy continuously distributed throughout the SiC bandgap,  $D_{it}$  can be calculated as follows:

$$D_{it} \approx \frac{2.5}{q} \left( \frac{G_p}{\omega} \right)_{\max} \quad (3)$$

The conductance ( $G_p/\omega$ ) measured as a function of frequency ( $\omega = 2\pi f$ ) is shown in Fig. 7 for different temperatures. The show up of two peaks (A and B) suggests the presence of defects with different features, including emission/capture times, activation energy ( $E_A$ ) and concentration. By performing conductance measurements with different  $V_G$  and T, the interface trap density  $D_{it}$  as a function of  $E_A$  ( $E_T - E_C$ ) has been calculated for the two defects and reported in Fig. 8 (symbols).

The relatively limited energy range of  $D_{it}$  may be ascribed to conductance method, since it yield  $D_{it}$  only in the portion of the bandgap scanned by the Fermi level in depletion and weak inversion conditions.

TCAD simulator [15] has been adopted to verify the electrostatic effect of such traps on the  $I_D V_G$  characteristics of the SiC power MOSFET.

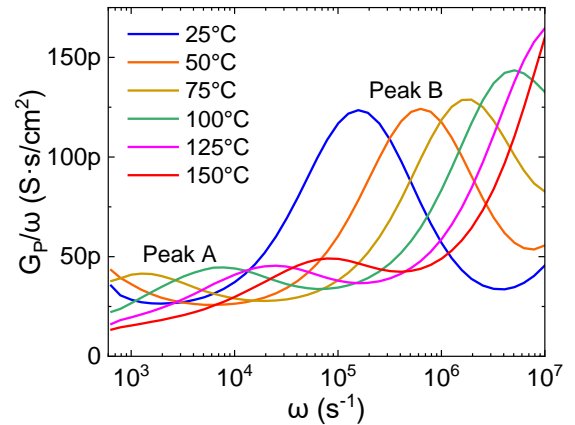


Fig. 7:  $G_p/\omega$  versus  $\omega$  as a function of different temperatures, measured using Conductance method.

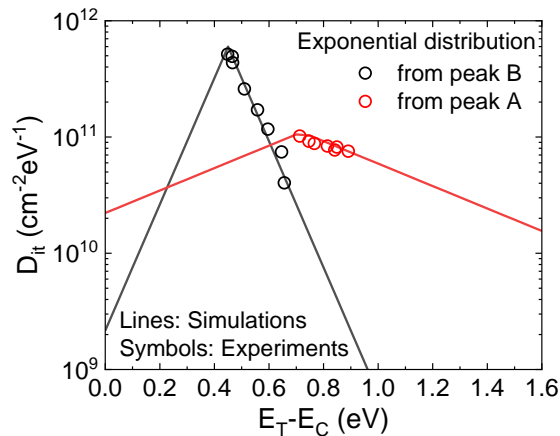


Fig. 8: Interface trap density as a function of energy position, calculated from conductance experiments (symbols) and adopted for in the simulations (lines).

Based on the experiments, two exponential trap distributions have been added at the SiC/SiO<sub>2</sub> interface as reported by lines in Fig. 8. Their adoption allows us to qualitatively reproduce the  $V_{TH}$  hysteresis observed during tests with different  $V_G$  sweep rates (lines, Fig. 6), confirming the important role of interface defects on the  $V_{TH}$  instability. However, it is worth noting that such distributions are not sufficient to reproduce the  $\Delta V_{TH}$  reported in Fig.4, as it is the result of interface, border and oxide traps. The last two are difficult, if not impossible, to characterize with conductance measurements.

### Conclusion

The role of interface/border defects on the  $V_{TH}$  instability has been investigated by means of slow-, fast-PBTI and hysteresis tests. Adopting the proper test procedure is of paramount importance, since the results can be completely different. A slow-PBTI procedure allows to mainly evaluate the effect of oxide charge trapping on the  $\Delta V_{TH}$ , which has a positive T-dependency. Vice versa, a negative T-dependency is observed when a fast-PBTI test is adopted, since the role of  $D_{it}$  and border traps becomes dominant. Finally,  $D_{it}$  has been characterized and their effect on the  $V_{TH}$  hysteresis has been qualitatively reproduced by means of TCAD simulator.

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