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Published Version:
Capasso, G., Zanuccoli, M., Tallarico, A.N., Fiegna, C. (2022). A novel approach to analyze the reliability of GaN power HEMTs operating in a DC-DC Buck converter. Piscataway, NJ : IEEE [10.1109/ESSDERC55479.2022.9947200].

Availability:
This version is available at: https://hdl.handle.net/11585/916829 since: 2023-02-22

Published:
DOI: http://doi.org/10.1109/ESSDERC55479.2022.9947200

G. Capasso et al. " A novel approach to analyze the reliability of GaN power HEMTs operating in a DC-DC Buck converter" in *IEEE 52nd European Solid-State Device Research Conference (ESSDERC),* September 2022, Milan, Italy, DOI: 10.1109/ESSDERC55479.2022.9947200.

A novel approach to analyze the reliability of GaN power HEMTs operating in a DC-DC Buck converter

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Abstract— **In this paper, we present a novel testbed based on a DC-DC synchronous Buck power converter, allowing the reliability analysis of GaN HEMT with p-type gate. In particular, it is possible to monitor the drift of the device parameters to highlight the main degradation mechanisms affecting GaN transistors in power electronic applications. Stress is applied when HEMTs operates within a practical 48/12V DC-DC converter featuring at 1 MHz switching frequency and 4A output current. The reported analysis has been carried in two different conditions, namely soft and hard stress, inducing a relatively low and high junction temperature, respectively. Results show that the high-side transistor of a DC-DC Buck converter is more prone to degradation, due to a larger threshold voltage and on-resistance drift. Moreover, based on the results of a validation analysis of the proposed characterization approach, the gate appears as the weaker transistor region causing device failure in the case of hard stress. Finally, a completely recoverable and a permanent V_{TH} and R_{ON} drift is observed in the case of soft and hard stress, respectively.**

Keywords—GaN power HEMTs, reliability analysis, R_{ON} degradation, V_{TH} drift

I. INTRODUCTION

Nowadays, several applications of power electronic, e.g. automotive end user industry, require more and more compact, efficient and high-power density DC-DC converters [1]. Gallium Nitride (GaN) technology, thanks to its low on-state resistance (R_{ON}), high switching speed, high breakdown voltage and comparable cost with respect to Silicon competitor, is gaining a primary role. However, to ensure a widespread adoption of GaN, a high level of reliability and robustness must be guaranteed. To date, GaN based high electron mobility transistors (HEMTs) are affected by degradation mechanisms which limit their reliability. For instance, these devices can be affected by current collapse increasing the dynamic R_{ON} or by threshold voltage (V_{TH}) instability, reducing the gate overdrive voltage. As a matter of fact, in order to identify the physical mechanisms responsible for degradation and to improve the device lifetime, GaN HEMTs long-term reliability is a relevant topic at research level [2]-[4].

V_{TH} instability has been reported and investigated by several works [5]-[7]. In [5], the important role of the characterization methods, which can significantly affect the V_{TH} measurement, has been discussed, both for pulsed and DC. In [6], it has been shown that the V_{TH} transients during positive gate bias stress are highly dependent on the current distribution in the gate stack of p-GaN HEMT. A link between gate current and V_{TH} shift during long-term positive bias temperature instability (PBTI) tests has been also observed in [7]. In addition to PBTI, the application of an off-state drain bias can induce positive V_{TH} shift in p-gate HEMTs [8].

Considerable effort has been devoted to monitor the dynamic R_{ON} under switching stress conditions (typical of a power converter application) [9][10]. Several methodologies and testbeds have been proposed to replicate switching conditions occurring in practical circuits [11]-[13]. In [11], the device response has been evaluated directly on-wafer, stressing the transistor through an off-state drain voltage sweep from 0 to 200V with 0.5 voltage step. Another technique consists of designing custom boards that are able to create current ringing, or voltage overshoot due to the inductor and quantify R_{ON} value [12]. In [13], a non-invasive drain current sensing and drain-source voltage sampling block has been added to a real circuit to continuously monitor R_{ON}. Many other papers study R_{ON} degradation under specific conditions, such as off-state voltage, drain current, junction temperature or on/off state time [14]-[16].

However, understanding the long-term reliability needs a more realistic context, in which current and voltage transients across device terminals are accurately reproduced. In addition, a deep investigation about the degradation mechanisms requires a full I-V characterization of the device under test. The ΔR_{ON} measured as a drain current/voltage variation at a pre-fixed condition can be caused by different factors such as V_{TH} or transconductance (g_m) shift, which in turn can be triggered by different physical phenomena [17].

To allow the I-V characterization of GaN HEMTs operating in practical power circuits, a custom measurement test board able to carry out an in-situ characterization is proposed in this work. This board allows to straightforwardly acquire the input, transfer and output I-V characteristics of GaN transistors operating in a DC-DC synchronous Buck converter.

In the frame of a validation analysis, the devices behaviour under soft and hard switching stress is monitored, highlighting the impact of the buck converter operation on the V_{TH}, R_{ON} and gate leakage of commercial GaN HEMTs.

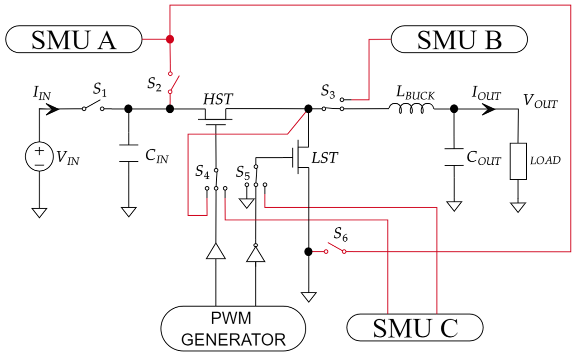

Fig. 1 - Simplified schematic of the setup adopted for the experimental in-situ characterization of the GaN HEMTs. The black wires and symbols denote the standard DC-DC synchronous Buck topology. The red portion of the network allows for the GaN I-V Characterization. Sj (j = 1..6) denotes the relays used for the hardware reconfiguration of the test circuit

II. SETUP DESCRIPTION

A simplified sketch of the novel setup adopted for this study is reported in Fig. 1. The circuit includes a standard type of synchronous Buck converter (in black) and the additional network (in red) to characterize the devices with a set of source measurement units (SMUs). In a synchronous Buck converter, the high-side transistor (HST) transfers energy to the output load, while the low-side transistor (LST) is the freewheeling diode that ensures current continuity on the inductor. The two transistors, HST and LST, are subjected to different electrical and thermal stresses. For this reason, both of them are characterized.

Stress to transistors is applied during power converter operation. After stress periods of pre-fixed duration, converter operation is stopped to allow transistors characterization by means of SMUs. Stress and characterization are alternatively repeated adopting a standard measure-stress-measure technique (Fig. 2). A hardware reconfiguration block based on electromechanical and solid-state relays enables the switching from Buck converter to characterization mode and viceversa. Such block as well as the characterization instruments are controlled by a National Instruments LabView virtual instrument. In addition, converter key-parameters, such as output voltage, input power and efficiency are continuously monitored during the stress. To estimate the junction temperature of the devices, a thermistor is mounted between the two GaN HEMTs. The performance deterioration of the converter circuit is linked to the device parameters degradation.

The monitoring of fast trapping and detrapping phenomena (<1s) is not possible because of the relatively long time required by the single device characterization (about 60s considering the soft shutdown of the converter and the subsequent device characterization). Therefore, the setup is aimed at studying the long-term reliability operating in a real-life application (DC-DC converter).

Commercial enhancement-mode p-type gate GaN-HEMTs featuring maximum drain-to-source voltage of 80V and maximum DC drain current of 6.8A are considered in this testbed validation.

The presence of a heatsink is required to avoid thermal stress to the transistors due to the significant junction to ambient thermal resistance of the small package.

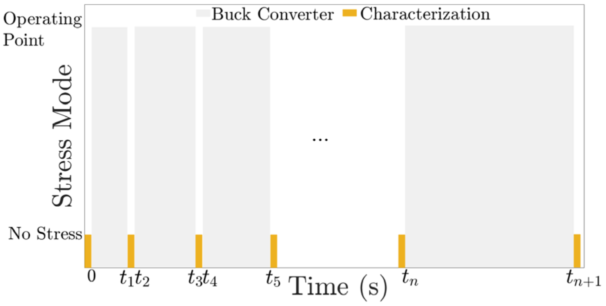

Fig. 2 – Illustration of the novel setup operation based on the measure-stress-measure technique. The stress phase is performed in the frame of power converter, whereas the measure one is carried out by SMUs.

III. RESULTS AND DISCUSSION

Experimental tests are performed by setting V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 4A (Fig.1) and switching frequency f_S = 1MHz. In electric and/or hybrid vehicles, this type of DC-DC converter plays a relevant role because of its simplicity and high efficiency [18]. The stress is carried out under two different thermal conditions, namely:

- Soft stress, where the heatsink is mounted to favour the heat transfer;
- Hard stress, where the transistors are exposed directly to the ambient in order to deliberately increase the junction temperatures of GaN.

The stress effect is monitored by extrapolating V_{TH}, R_{ON} and I_G from full I-V curves.

V_{TH} is extracted by constant-current Methods to avoid possible contributions coming from Δg_m. V_{TH} represents the value of the gate voltage V_G corresponding to drain current I_D = 3mA. Thanks to the full I_D-V_G characteristics, ΔR_{ON} is extracted at the same gate overdrive voltage (V_{GS} - V_{TH}) to evaluate the actual degradation, hence to avoid to include the contribution coming from ΔV_{TH} as in the case of online R_{ON} monitoring technique [13]. Finally, I_G is extracted from I_G-V_G characteristics.

Fig. 3 shows the V_{TH} drift during soft (top) and hard (bottom) stress for both HST and LST. First, it can be noted that, during soft stress (normal operation), the two transistors exhibit a different ΔV_{TH} dynamic. This is caused by the asymmetric stress condition applied to the two GaN HEMTs in a DC-DC converter. In particular, from electromagnetic printed-circuit-board simulations, power dissipation is estimated to be 1.6W and 0.5W for the HST and LST, respectively. Such difference induces a different junction temperature which is indirectly calculated (starting from the calculated power dissipation on transistors and thanks to the knowledge of thermal resistances provided by device and heatsink manufacturers) to be 60°C and 40°C for HST and LST, respectively. A similar ΔV_{TH} dynamic is reported also in [7] under PBTI stress at device level, ascribing its reduction, occurring at relatively long stress-time, to the gate leakage increase caused by the combined effect of positive gate bias and relatively high temperature. Indeed, by observing Fig. 4, it is possible to note that the HST gate leakage, in the case of soft stress, starts to increase when the related V_{TH} starts to decrease (1000 s). This is not observed in the case of LST.

By removing the heatsink (hard stress condition) the junction temperature of the HST exceeds the maximum junction

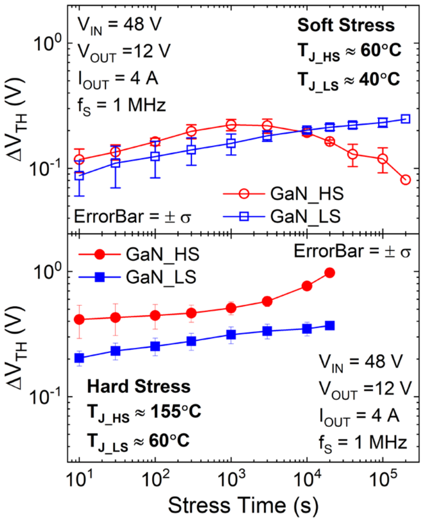

Fig. 3 – Threshold voltage degradation in the case of soft (top) and hard (bottom) stress; σ represents the standard deviation of the data.

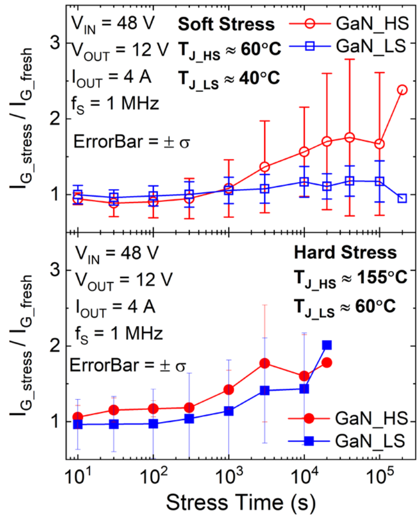

Fig. 4 – Gate leakage degradation in the case of soft (top) and hard (bottom) stress; σ represents the standard deviation of the data.

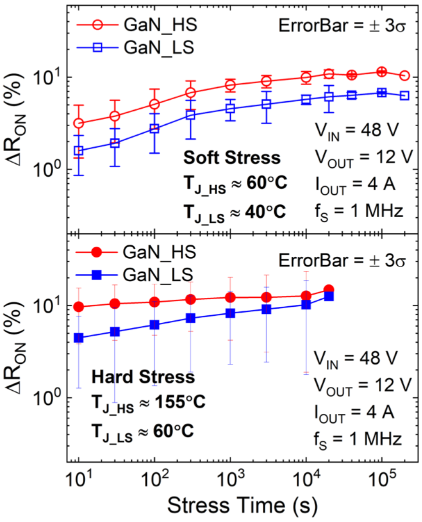

Fig. 5 – On-state resistance degradation in the case of soft (top) and hard (bottom) stress; σ represents the standard deviation of the data.

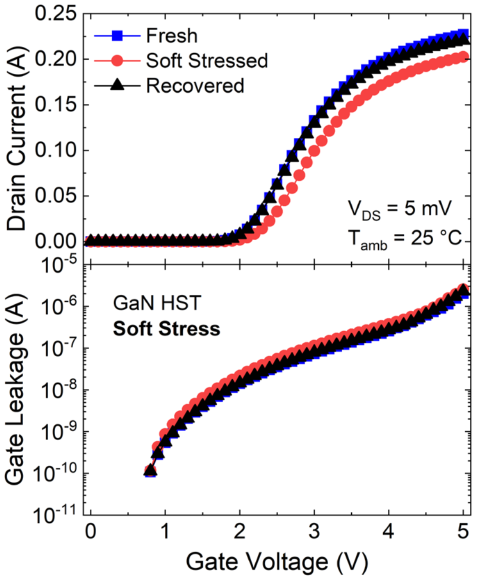

Fig. 6 – Transfer (top) and gate leakage (bottom) characteristics in the case of soft stress test.

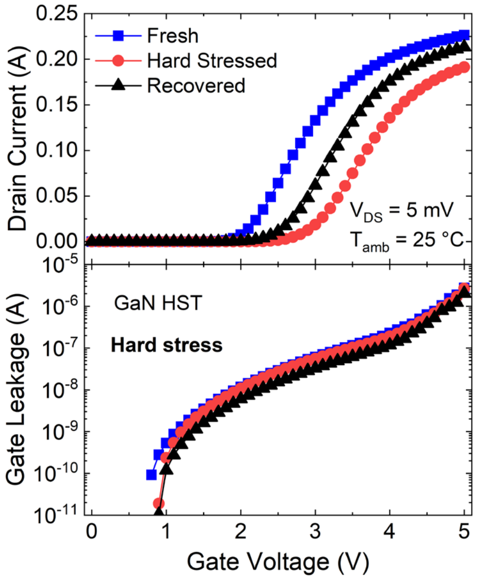

Fig. 7 – Transfer (top) and gate leakage (bottom) characteristics in the case of hard stress test.

temperature operating rating (150 °C). In this case a larger V_{TH} drift (up to 1 V) is observed, leading to device failure after ~ 25 ks. Also in this case, it is worth noting the larger degradation of the HST, which is the first to fail.

Concerning the ΔR_{ON} (Fig. 5), the soft stress (top) induces the same monotonous increase in both transistors up to around 10 ks, after which a saturation effect is observed. Also in this case, the HST exhibits a larger ΔR_{ON}, highlighting the extent of the level of criticality of HST in terms of reliability. In the case of hard stress (Fig. 5 bottom), ΔR_{ON} exhibits a different trend with respect to the soft stress test. In particular, the HST shows a 10% shift after only 10s, whereas the ΔR_{ON} of LST is characterized by a lower starting value and a higher slope, reaching approximately comparable drift at 20 ks, which is of the same magnitude of the hard stress case (HST).

Finally, a last characterization has been performed after 14 hours of recovery, showing that, parameters drifts (V_{TH} and R_{ON}) observed after soft stress are completely recoverable (Fig. 6), suggesting trapping mechanisms in pre-existing defects. A different picture is observed after the hard stress condition, where a permanent degradation persists after 90 hours, ascribed to the creation of new deep defects (Fig. 7).

Overall, from the reported testbed validation analysis, it is possible to recognize that a limited dispersion of the results obtained from experiments carried on different nominally-identical devices allows to identify repeatable degradation trends, such as: i) HST is more prone to degradation because of the larger stress intrinsically induced by the DC-DC Buck converter; ii) a significant V_{TH} shift, indicating gate degradation, occurs. It is markedly larger in the case of hard stress; iii) the noticeably differences in ΔV_{TH} and ΔR_{ON} after soft and hard stress, suggest that the premature device failure may be ascribed to gate breakdown.

IV. CONCLUSIONS

A DC-DC power converter aimed at experimentally characterizing in-situ the reliability of GaN HEMTs has been implemented. The test circuit allows to stress power transistors under realistic electrical and thermal conditions and to monitor different signatures (V_{TH}, R_{ON}, I_G, etc.) of their degradation, providing useful information for both GaN circuit designers and GaN technology manufacturers. The results of a validation analysis highlight that the developed testbed is able to identify the main degradation trends in the frame of realistic transistor operation. The obtained results show that: i) high-side transistor is more prone to degradation compared to low-side one; ii) the two transistors show a different ΔV_{TH} dynamic, suggesting that different degradation mechanisms are involved; iii) although the significant ΔR_{ON}, the gate seems to be the region responsible for device failure under hard stress condition, supported by large ΔV_{TH} and gate leakage drift.

ACKNOWLEDGMENT

Part of this work is funded by iRel40, a European co-funded innovation project that has been granted by the ECSEL Joint Undertaking (JU) under grant agreement No 876659. The funding of the project comes from the Horizon 2020 research programme and participating countries. National funding is provided by Germany, including the Free States of Saxony and Thuringia, Austria, Belgium, Finland, France, Italy, the Netherlands, Slovakia, Spain, Sweden, and Turkey.

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