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Design and Characterization of an Active Low-Pass Envelope Detector for Wake-Up Radio Receivers

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Abstract—This paper presents a design flow for an active low-pass (LP) Envelope Detector (ED) for Wake-Up Radio (WUR) receivers and provides insight on the well-known bitrate-sensitivity-current trade-off and on additional aspects which may be critical in Internet of Things (IoT) applications, such as maximum receivable input power and robustness against Continuous Wave (CW) interferers. The implemented LP ED, designed using the STMicroelectronics 90-nm BCD technology, receives 400-bit OOK-modulated packets with an 868-MHz carrier frequency and achieves -35.5-dBm sensitivity with a 2.7-nW power consumption. Finally, it receives input power levels up to 15 dBm and achieves 22-dB Signal-to-Interference Ratio (SIR) with a CW interferer with a 100-kHz frequency offset.

Keywords—Active Envelope Detector, maximum input power, Signal-to-Interference Ratio

I. INTRODUCTION

Low-power Wireless Sensor and Actuator Networks (WSANs) are an essential part of the Internet of Things (IoT) [1]. The Wake-Up Radio (WUR) is an enabling technology for WSANs since it allows asynchronous communication between the gateway and sensor nodes while reducing their overall power consumption [2]. A generic WUR is composed of an Analog Front-End (AFE) and a Baseband Logic (BBL). The purpose of the AFE is turning the input signal, which is usually OOK-modulated, into a stream of bits, whereas the BBL compares the received sequence with the actual address of the specific node and if the two match a Wake-Up pulse is issued. The incoming signal first passes through an external matching network and is then fed to the AFE. The first block within the AFE is an Envelope Detector (ED), i.e. a rectifier aimed at extracting the envelope of the input signal, which is typically followed by a block performing amplification at baseband. Finally, a decision circuit digitizes the extracted envelope by turning it into a bitstream.

Recently, rectification is often performed through passive diode chains, which are known to have better sensitivity performances thanks to the lack of flicker noise [3]–[5]. However, active implementations have also been chosen throughout the years for the following advantages [6]–[8]: i) smaller area thanks to the absence of a separated baseband amplifier, ii) a wider input power dynamic range, iii) a natively higher input resistance and lower input capacitance, thus making the design of an effective matching network easier, and iv) the availability, depending on the specific ED topology, of a threshold generated by the ED itself for the subsequent decision circuit.

This paper focuses on an active ED which can be implemented as a band-pass (BP) or a low-pass (LP) circuit. As a matter of fact, a first comparison between these two options is carried out in [8] but only results for a BP ED are

given. On the other hand, [9] presents results for a prototype in the STMicroelectronics 90-nm BCD technology implementing a LP ED but mostly covers the BBL. Conversely, this paper focuses on the design flow for the LP ED, also providing deeper insight on the well-known bitrate-sensitivity-current trade-off and on additional aspects which may be critical in IoT applications, such as maximum receivable input power and robustness against CW interferers. Moreover, this paper aims at completing the experimental characterization of the implemented LP ED covering the aforementioned critical aspects.

II. ACTIVE ENVELOPE DETECTOR

A. Demodulation mechanism

Active EDs perform both envelope extraction and the baseband amplification of the extracted envelope. They are usually biased with nanoAmps due to the very tight constraints on power consumption applied to WURs. This implies all MOSFETs in the ED operate in the subthreshold region, which in turn allows the exploitation of second order nonlinearities for envelope extraction.

The demodulation mechanism for active EDs is shown hereafter, using the proposed one, shown in Fig. 1, as an example. The input signal is OOK-modulated:

$$v_{RF}(t) = v_M(t) \cos(\omega t),$$

where $v_M(t)$ is the OOK envelope signal which is to be extracted. Since M_1 operates in subthreshold, its drain current is an exponential function of the input signal, which can be written as a Taylor series and truncated at the second order. Assuming all RF components to get filtered out at baseband, this yields [8]

$$I_{D1} = I_{bias} \left[1 + \frac{v_M^2(t)}{4n^2V_T^2} \right] \equiv I_{bias} + \Delta I(t). \quad (1)$$

$\Delta I(t)$ is an envelope dependent term which can be attributed to an effective low-frequency input voltage source $v_{IN}(t)$ replacing $v_{RF}(t)$:

$$v_{IN}(t) \equiv \frac{\Delta I(t)}{g_{m1}} = \frac{v_M^2(t)}{4nV_T}, \quad (2)$$

where the expression of the transconductance of M_1 in subthreshold $g_{m1} = I_{bias}/nV_T$ has been used [8].

B. AC response and design flow

The proposed ED features M_1 , which acts both as a rectifier and as a common gate amplifier within the signal band, and the feedback loop composed of follower M_2 and the RC filter, which prevents R from directly loading M_1 and allows the circuit to be self-biased. Assuming unity gain for the follower stage and the two poles to be well separated for

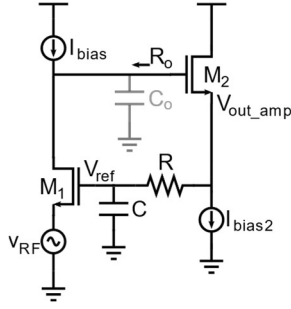


Fig. 1. Schematic of the proposed active ED, reused from [8].

simplicity, the small-signal response of the ED can be found using the open circuit time constant method:

$$\frac{v_{out_amp}}{v_{IN}}(s) = \frac{1 + sR^*C}{(1 + s\frac{R^*C}{g_{m1}R_o})(1 + sR_oC_o)} \quad (3)$$

where $R^* = R + R_{OUTFOLL}$, with $R_{OUTFOLL}$ the output resistance of M_2 , $R_o = r_{out1}$ is the output resistance at the drain of M_1 , where $r_{out1} = 1/\lambda I_{bias}$ and λ is the channel modulation coefficient. C_o accounts for all parasitics at the drain of M_1 [8]. The zero, $1/R^*C$, and the first pole, $g_{m1}R_o/R^*C$, are due to capacitance C and define the shape of the response (BP or LP, as will be clearer in Section II.D), whereas the second pole, $1/R_oC_o$, is due to parasitics and corresponds roughly to the bitrate of the ED. This model corresponds to the simulations shown in Fig. 2a.

The output amplitude V_{OUTM} can be calculated from (2) and (3) as

$$V_{OUTM} \propto \frac{g_{m1}R_o}{4nV_T} v_M^2.$$

As a result, the rectification gain can be written as

$$G_{RECT} \equiv \frac{V_{OUTM}}{v_M} = \frac{g_{m1}R_o v_M}{4nV_T} \propto v_M. \quad (4)$$

and is itself proportional to v_M because second order non-linearities are being leveraged. G_{RECT} also links the ED RMS output noise voltage $v_{RMS,out}$ to the ED RMS output noise voltage referred to the input $v_{RMSeq,in}$, as follows:

$$\frac{v_{RMS,out}^2}{G_{RECT}^2} = v_{RMSeq,in}^2. \quad (5)$$

Defining the input SNR as

$$SNR_{in} = \frac{v_M}{v_{RMSeq,in}}, \quad (6)$$

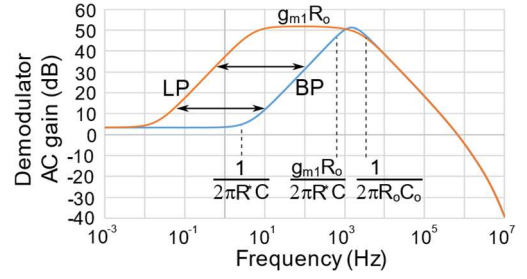
and solving the system composed of (4), (5) and (6) results in the estimated envelope amplitude

$$v_M = \sqrt{\frac{SNR_{in} \cdot v_{RMS,out} \cdot 4nV_T}{g_{m1}R_o}}. \quad (7)$$

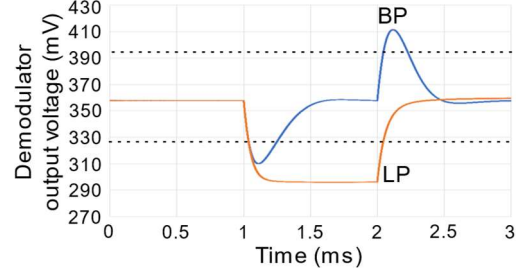
Voltage sensitivity $v_{M,min}$ can be estimated using (7) by setting the desired SNR_{in} and running an AC noise simulation to obtain the values for $g_{m1}R_o$ and $v_{RMS,out}$.

Finally, the integrated noise can be estimated assuming it completely white, resulting in

$$v_{RMS,out}^2 = \int_0^{BW} \frac{4k_B T \gamma}{g_m} df = \frac{4k_B T \gamma}{g_m} BW, \quad (8)$$



(a)



(b)

Fig. 2. a: simulated AC response for $C = 100$ nF (orange) and for $C = 500$ pF (blue). b: simulated transient response for $C = 100$ nF (orange) and for $C = 500$ pF (blue) to a '0-1-0' input OOK-modulated signal. The thresholds are also visible in dotted line. Pictures reused from [8].

where BW is the bitrate of the ED, which is mainly related to the second pole $1/R_oC_o$ with $R_o = 1/\lambda I_{bias}$.

AC response programmability can be achieved as in the following: the frequency of the second pole can be multiplied by a factor k by multiplying I_{bias} by k ; it is also possible to multiply the frequencies of the zero and the first pole by a factor k by dividing capacitance C by k .

C. Bitrate-sensitivity-current trade-off

An increase in the bitrate can be achieved at the cost of multiplying current I_{bias} by a factor k while dividing capacitance C by k accordingly. Under these conditions, g_{m1} gets multiplied by k as well. This results in $v_{RMS,out}$ (8) and $g_{m1}R_o$ staying the same, whereas the first pole $g_{m1}R_o/R^*C$ moves along with the second one keeping the same AC response shape (Fig. 2a). From (7), increasing the bitrate yields no significant changes in the voltage sensitivity ($v_{M,min}$) as illustrated in the upper part of Table I.

As shown in the lower part of Table I, sensitivity enhancement as well can be achieved at the cost of increasing current I_{bias} , but the bitrate has to be kept constant. To do so, C_o has to be increased accordingly through the addition of a parallel integrated capacitance. The same value for C is kept as well. This again causes a multiplication of g_{m1} without any changes in $g_{m1}R_o$, but $v_{RMS,out}$ gets divided by \sqrt{k} . Finally, this results in a division of the voltage sensitivity by $\sqrt[4]{k}$, yielding

$$v_{M,min} \propto \frac{1}{\sqrt[4]{I_{bias}}}$$

D. Comparison between active BP and LP ED

As mentioned in Section II.B, the AC response of an active ED can be BP or LP, depending on the position of the first pole. In particular, a lower R^*C time constant results in a LP response, setting the first pole at a frequency lower than the inverse of the packet length. Conversely, a BP response

TABLE I. BITRATE-SENSITIVITY-CURRENT TRADE-OFF

Bitrate increase: $I'_{bias} = k \cdot I_{bias}, C' = C/k, C'_o = C_o$					
Parameter	g_{m1}	$g_{m1}R_o$	BW	$v_{RMS,out}^2$	$v_{M,min}$
Mult. factor	$\cdot k$	$const$	$\cdot k$	$const$	$const$
Sensitivity enhancement: $I'_{bias} = k \cdot I_{bias}, C' = C, C'_o > C_o$					
Parameter	g_{m1}	$g_{m1}R_o$	BW	$v_{RMS,out}^2$	$v_{M,min}$
Mult. factor	$\cdot k$	$const$	$const$	$\cdot 1/k$	$\cdot 1/\sqrt{k}$

implies the first pole is high enough for the output signal to relax within one bit-time. Fig. 2a shows the frequency response v_{out_amp}/v_{IN} of an implementation of the proposed ED with $I_{bias} = 1$ nA, $I_{bias2} = 5$ nA and $V_{DD} = 1.2$ V. In orange is an example of LP frequency response for $C = 100$ nF, whereas in blue is an example of BP frequency response for $C = 500$ pF. The second pole, determining bitrate, is at the same frequency in the two cases, around 1 kHz, whereas the first pole is slightly lower than 1 kHz in the BP case and around 10 Hz in the LP case. This determines the time-domain response of v_{out_amp} shown in Fig. 2b, assuming a ‘0-1-0’ input OOK-modulated signal. In the BP case the ED output peaks at each transition in the input bit, whereas in the LP case the ED outputs a low-pass filtered version of the input signal envelope.

The two cases are very similar in terms of normalized sensitivity [8]. However, in the BP case flicker noise is filtered by the very AC response of the ED and C is likely small enough to be integrated. In the LP case a flicker noise-speed trade-off is set and C is likely way too big to be integrated. Minimizing flicker noise may require significantly enlarging M_1 and the MOSFET delivering I_{bias} , leading to an increase in C_o . On the other hand, Fig. 2b shows that a BP ED requires the subsequent stage to be a trigger with two thresholds. Moreover, Manchester coding is needed to prevent multiple errors due to noise in case of long sequences of equal consecutive bits. Conversely, a standard comparator with one threshold only can be employed if a LP response is chosen and the comparator can be fed a threshold voltage generated by the ED itself, thus making the whole system simpler.

III. LOW-PASS ACTIVE ED

An active LP ED has been implemented in the STMicroelectronics 90-nm BCD technology. It is biased with $I_{bias} = 1$ nA, $I_{bias2} = 1$ nA, $V_{DD} = 0.6$ V. $R = 75$ M Ω is integrated whereas $C = 500$ nF is external. A 1-kbit/s bitrate and an 868-MHz carrier frequency are targeted. Process and temperature robustness have been proven through 500-run transient Montecarlo simulations at three different temperatures. Applying a 5-mV input RF signal, the useful v_{out_amp} signal is nominally around 10 mV with $\sigma = 1.04$ mV, 8 mV with $\sigma = 0.7$ mV and 6 mV with $\sigma = 0.34$ mV at -20°C , 27°C and 85°C , respectively. All measurements reported hereafter have been carried out using an external coaxial impedance adapter with a 50-Ohm resistor in parallel to the input for a unity gain broadband matching network.

As anticipated in Section II.D, an ED with a LP response outputs a low-pass filtered version of the input signal envelope, shown in Fig. 2b. In order to perform Bit Error Rate (BER) measurements, the implemented ED is followed by a comparator which receives v_{out_amp} and V_{ref} (see Fig. 1) as inputs [9]. V_{ref} stays almost equal to its quiescent value throughout the reception of the whole packet, making it

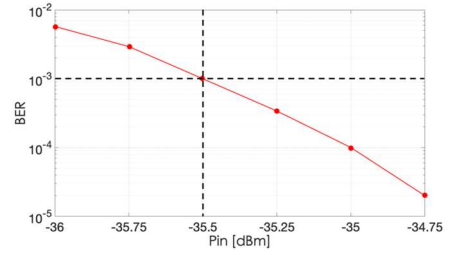


Fig. 3. Measured BER of the proposed ED.

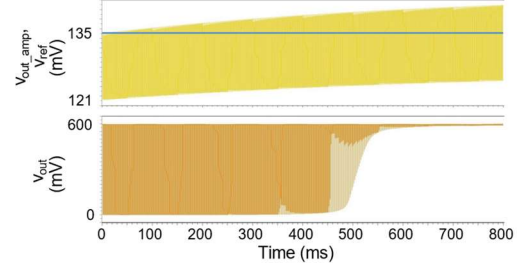
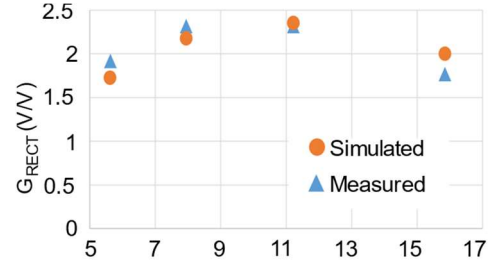
Fig. 4. Simulated transient response of v_{out_amp} (on top in yellow), V_{ref} (on top in blue) and comparator output v_{out} (at the bottom in orange) to an 800-bit ‘1-0-1-0’ packet at 1 kbit/s with a 7-mV input amplitude.

Fig. 5. Simulated and measured (in orange and blue, respectively) rectification gain of the proposed ED.

suitable to be used as a threshold by the subsequent comparator. Voltages V_{off1} and V_{off2} at the bulks of the input differential pair MOSFETs are leveraged to set an effective comparator threshold V_{THR} which lies between the two possible values v_{out_amp} can have. As a matter of fact, the effective offset of the comparator V_{off} , which sets its effective threshold, is ultimately determined by the difference between V_{off1} and V_{off2} as

$$V_{off} = \gamma \left(\sqrt{|2V_f|} - \sqrt{2V_f + (V_{off1} - V_{off2})} \right).$$

A. Sensitivity

The ED has a measured sensitivity, i.e. the input power corresponding to a 10^{-3} BER, of -35.5 dBm, whereas the model presented in Section II.B predicts around -37 dBm setting $SNR_{in} = 5$. Fig. 3 shows the measured BER as a function of input power around sensitivity.

B. Maximum packet length and minimum packet spacing

Actually, V_{ref} is not perfectly stuck to its quiescent value throughout the reception of the whole packet. Whenever a ‘1’ is received, v_{out_amp} lowers and compresses I_{bias2} . Therefore, some current flows from V_{ref} to v_{out_amp} , thus slightly discharging C with a rate which is related to the $R \cdot C$ time constant. Since v_{out_amp} is unipolar, i.e. it cannot have higher values than its quiescent value, there is no way for C to regain the lost charge. Moreover, since there is AC gain from V_{ref} to v_{out_amp} right after the first pole, the slight decrease

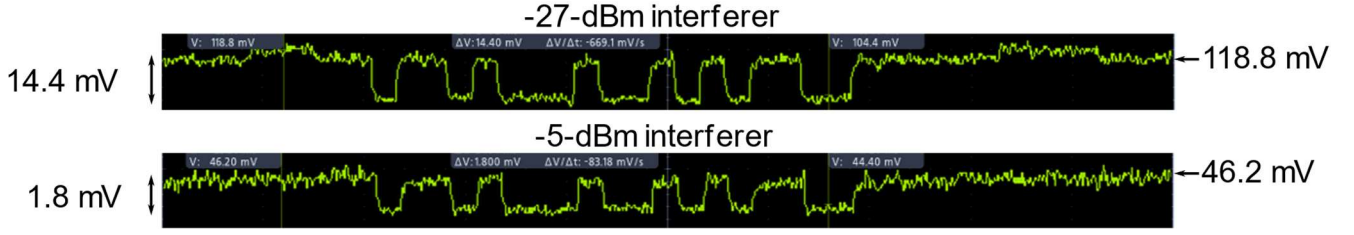


Fig. 6. ED output with a -27-dBm 868-MHz input signal and a -27-dBm 868.1-MHz interferer on top while a -5-dBm 868.1-MHz interferer at the bottom.

in V_{ref} translates into a much higher increase in v_{out_amp} . Therefore, after many received '1's the comparator is no longer able to correctly discriminate between '0' and '1', as shown in the example in Fig. 4. This sets a maximum number of receivable '1's, thus, assuming packets to include the same number of '1's as of '0's, a maximum packet length. Also, a minimum spacing between two subsequent packets needs to be set in order to let v_{out_amp} settle back to its quiescent value. In the presented implementation, the measured maximum receivable packet length and minimum packet spacing are around 400 bits and 100 ms, respectively.

C. Maximum receivable input power

Fig. 5 shows the simulated and measured (in orange and blue, respectively) rectification gain of the proposed ED. Gain compression is clearly visible and occurs due to the squeezing of generator I_{bias2} during the reception of a '1'. For the measured prototype, this allows the correct reception of input power levels up to +15 dBm (around 50 dBs over sensitivity).

D. Robustness against CW interferers

In the presence of a CW interferer, the incoming signal at the input of the ED is

$$v_{RF}(t) = v_M(t) \cos(\omega_1 t) + A \cos(\omega_2 t). \quad (9)$$

Substituting (9) into (1) yields

$$I_{D1} = I_{bias} \left[1 + \frac{v_M^2(t)}{4n^2V_T^2} + \frac{A^2}{4n^2V_T^2} + \frac{v_M(t)A}{2n^2V_T^2} \cos[(\omega_2 - \omega_1)t] \right].$$

An additional DC term proportional to the square of the interferer amplitude A is present, so the circuit responds to the appearance of a CW interferer as if a '1' was being received constantly. A third term is present but it lies out of band unless $\omega_2 - \omega_1$ is very small. Moreover, it only affects the output when a signal '1' is being received and its amplitude is proportional to A instead of A^2 , so it can be neglected.

Therefore, when a CW interferer is applied to the input of the ED the quiescent value of v_{out_amp} moves towards ground. If the amplitude of the interferer A is too big, the voltage across generator I_{bias2} becomes too small for the circuit to react to the reception of a signal '1'. For instance, Fig. 6 shows v_{out_amp} with an input -27-dBm 19-bit packet at 868 MHz: on top, a -27-dBm CW interferer at 868.1 MHz has been applied, resulting in a roughly 120-mV quiescent value for v_{out_amp} and leaving room for a roughly 15-mV drop in v_{out_amp} itself when a signal '1' is received; at the bottom, a -5-dBm CW interferer at 868.1 MHz has been applied, leading to a roughly 45-mV quiescent value for v_{out_amp} and only leaving room for a 2-mV drop. Actually, targeting a 10^{-3} BER, the implemented ED reaches a 22-dB Signal-to-Interferer

Ratio (SIR) with a 100-kHz frequency offset. Table II summarizes the performances of the proposed ED.

TABLE II. MEASURED RESULTS OF THE ACTIVE LP ED

Sensitivity at 27°C	-35.5 dBm
Supply voltage	0.6 V
Current consumption	4.5 nA
Maximum packet length	400 bits
Minimum packet spacing	100 ms
Maximum receivable input power	15 dBm
SIR with a CW interferer with a 100-kHz frequency offset	22 dB

CONCLUSIONS

This paper presents a design flow for an active ED, which can be implemented as a LP or a BP circuit. The bitrate-sensitivity-current trade-off has been analyzed along with critical aspects such as maximum receivable input power and robustness against CW interferers. A thorough experimental characterization of an active LP ED, designed using the STMicroelectronics 90-nm BCD technology, has been presented. The ED achieves -35.5-dBm sensitivity with 2.7-nW power consumption and receives 400-bit OOK-modulated packets with input power levels up to 15 dBm. Finally, it achieves 22-dB SIR with a CW interferer with a 100-kHz frequency offset.

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