High-Temperature Time-Dependent Gate Breakdown of p-GaN HEMTs

M. Millesimo *et al*. " High-Temperature Time-Dependent Gate Breakdown of p-GaN HEMTs" in *IEEE Transactions on Electron Devices,* Vol. 68, No. 11, November 2021, DOI: 10.1109/TED.2021.3111144.

High-Temperature Time-Dependent Gate Breakdown of p-GaN HEMTs

M. Millesimo, C. Fiegna, N. Posthuma, M. Borga, B. Bakeroot, S. Decoutere, A.N. Tallarico

***Abstract* —In this paper, we present an in-depth high temperature analysis of the long-term gate reliability in GaN-based power HEMTs with p-type gate. Three different isolation process options, aimed at improving the time-dependent gate breakdown (TDGB), are proposed and compared by means of constant voltage stress tests performed at different forward gate biases, temperatures and geometries. In particular, depending on the gate bias and temperature, the breakdown event may occur along the active gate area or through the isolation region. Results show different voltage dependency for such two different failure locations; therefore, two field-acceleration fitting models are needed for the estimation of lifetime.**

Furthermore, the gate time-to-failure (TTF) shows a non-monotonous temperature dependency at given gate bias. More specifically, a positive and a negative T-derivative are observed at relatively low and high temperatures, respectively, which are related to active gate area and isolation region failure, respectively.

***Index Terms*—Forward gate stress, isolation failure, lifetime models, p-GaN HEMT, gate reliability, temperature dependency, time-dependent gate breakdown.**

I. Introduction

THE increasing importance of power electronics in many application fields (such as hybrid/electric vehicles, aerospace, renewable energy systems, industrial automation, etc.) is leading to the need of even more performing, robust and efficient power transistors [1]- [3]. GaN-based high-electron-mobility transistors (HEMTs) promise to satisfy such requirements due to their capability of operating at high voltage and switching frequency with higher efficiency and comparable low costs of the well-established silicon-based technologies [4]- [5]. This is especially due to the impressive material properties of GaN, including wider bandgap, higher critical electric field, higher electron mobility, etc. when compared with Silicon [6]. What makes HEMTs so attractive is the two-dimensional electron gas (2DEG) that appears at the AlGaN/GaN interface and acts as a low-resistance conduction channel [7]. The 2DEG formation takes place also with no gate bias and, in the past years, different solutions have been adopted to enhance the normally-off operation which is preferred for safety and gate easy-controllability reasons [8]- [10]. The most stable solution consists of interposing a p-type (doped with magnesium, Mg) GaN layer between the gate metal and the AlGaN barrier [11]. In this way, the gate stack can be modelled as two back-to-back diodes [12], [13]: a Schottky metal/p-GaN diode and a PIN p-GaN/AlGaN/GaN diode. This allows the 2DEG depletion under the gate region shifting the threshold voltage towards positive values.

Considering the great interest in such technology, the time-dependent breakdown, in both ON-state and OFF-state conditions, are object of many studies [12]- [22]. In particular, a significant effort has been made to investigate the role of the gate stack design and fabrication processes on the time-dependent gate breakdown (TDGB), occurring under forward gate bias stress [12]- [17]. In [13] and [14], the role of the Mg concentration in the p-GaN layer on the TDGB has been discussed, showing that the lower the Mg concentration, the more robust the devices in terms of time-to-failure (TTF). Recently, Tallarico et al. [15] reported the role of the AlGaN barrier properties on the TDGB. In particular, lowering the aluminum content (Al%) and optimizing the thickness of the barrier layer at a given Al% leads to a longer lifetime of the gate stack. Furthermore, in [16] it has been demonstrated that a lateral etching of the gate metal, namely gate metal retraction (GMR), deposited on the p-GaN layer, improves the long-term reliability because of the suppression of the gate leakage along the gate edges, which leads to a premature breakdown. In addition, on such devices with the GMR, temperature-dependent breakdown mechanisms, occurring at different regions, have been found out, i.e. failure along the active gate area and through the isolation region at relatively low (< 80 °C) and high temperatures (>80°C), respectively. The phenomena have been identified by failure analysis on devices with different gate geometries. More specific, when the isolation failure occurs, the TTF values do not show gate length (L_G) and width (W_G) dependency. Differently, both L_G and W_G dependencies are observed in the case gate area related breakdown occurs.

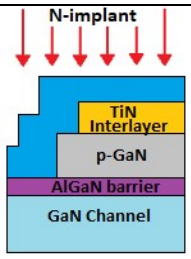
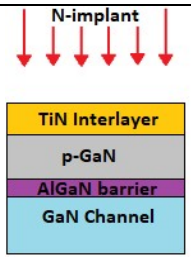
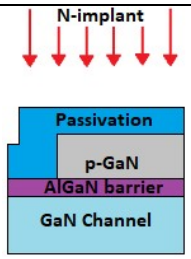
Concerning the TDGB, the debate on the choice of the field acceleration model (TTF vs V_G) adopted for the lifetime extrapolation is still ongoing. In [17], Moens et al. compared three different models: i) the "E-model" (TTF $\propto \exp(V_G)$); ii)

M. Millesimo, C. Fiegna and A. N. Tallarico are with the Advanced Research Center on Electronic System, Department of Electrical, Electronic, and Information Engineering, University of Bologna, 47522 Cesena, Italy (e-mail: maurizio.millesimo2@unibo.it; claudio.fiegna@unibo.it; a.tallarico@unibo.it)

N. Posthuma, M. Borga and S. Decoutere are with imec vzw, B-3001 Leuven, Belgium (e-mail: Matteo.Borga@imec.be; Niels.Posthuma@imec.be; Stefaan.Decoutere@imec.be).

Benoit Bakeroot is with CMST, imec and Ghent University, Ghent University, B-9052, Belgium (e-mail: Benoit.Bakeroot@imec.be)

TABLE I
PROCESS FLOW IN THE CASE OF THREE ISOLATION OPTIONS. NOTE THAT, FOR EACH VARIANT, PROCESS STEP 1 REPRESENT THE FIRST STEP AFTER p-GaN LAYER DEPOSITION.

Process step order	 **Reference**	 **Split 1**	 **Split 2**
1	TiN interlayer deposition	TiN interlayer deposition	SiN hard mask deposition
2	P-GaN patterning + gate metal retraction (TiN lateral etch)	AA patterning and N-implant	p-GaN and SiN hard mask patterning
3	Passivation (Al_2O_3 and SiO_2) deposition	P-GaN patterning + gate metal retraction (TiN lateral etch)	Passivation (Al_2O_3 and SiO_2) deposition
4	Active Area (AA) patterning and N-implant	Passivation (Al_2O_3 and SiO_2) deposition	AA patterning and N-implant
5	Passivation etching on top of TiN interlayer (gate region)	Passivation etching on top of TiN interlayer (gate region)	Passivation etching in the gate region ($SiN + Al_2O_3 + SiO_2$) up to pGaN layer
6	Gate metal stack deposition and patterning	Gate metal stack deposition and patterning	Gate metal stack deposition and patterning

"TTF ∝ $1/I_G$ "; iii) "TTF ∝ $\exp(1/I_G)$". The last two models, proposed in [12] and [13], respectively, are statistical based approaches, while the E-model is widely adopted for SiO_2 reliability studies [23].

In this paper, we investigate the TDGB at relatively high temperature (T=150 °C) of p-GaN HEMTs with the GMR process. In addition to [16], three different isolation process options are compared in terms of gate lifetime by means of extended constant voltage stress test on devices featuring various gate geometries.

II. Device Under Test and Process Variants

Lateral GaN-on-Si HEMTs with p-type gate fabricated by *imec* are considered in this study. The top layers (shown in Fig. 1a), grown on a super lattice buffer and a C-doped GaN back-barrier, consist of a uid GaN channel, an AlGaN barrier, a 80-nm-thick pGaN layer doped with magnesium, and a thin TiN metal interlayer which is laterally etched (GMR) (Fig. 1a), followed by a metal stack deposition. The access regions are passivated by a dielectric stack composed of a thin layer of Al_2O_3, followed by a thicker layer of SiO_2. Finally, devices are isolated by N-implantation (Fig. 1b). More details on the process steps can be found in [11].

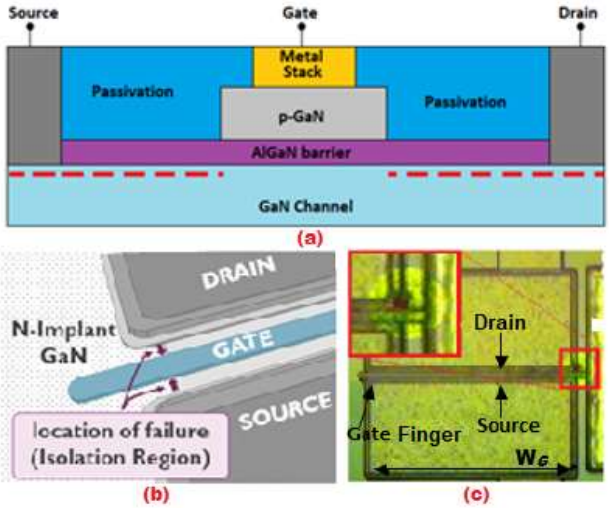


Fig. 1. (a) Final configuration of the device (not in scale), independently of the isolation process. (b) Representation of the isolation region (dotted area). (c) Optical microscopy image after the isolation region failure shown for the first time in [16].

Three different process integration schemes are used for the device isolation, aimed at the analysis of time-dependent gate breakdown at high temperatures (integration flow summarized in Table 1).

The device-under-tests (DUTs) feature a symmetric structure, realized for gate reliability studies, with equal gate–to-source and gate-to-drain distance (L_{GS} = L_{GD}) of 1.5μm. Different gate lengths (L_G) and widths (W_G) have been characterized to investigate the area and the edges dependence of the time-to-failure.

III. Time-Dependent Gate Breakdown

Time-Dependent gate breakdown analysis has been carried out by means of constant voltage stress (CVS) test at different gate biases and temperatures, on devices featuring different isolation processes and gate width and length. During the stress, a positive gate bias is applied while monitoring the current over the time up to breakdown. Drain, Source and Substrate contacts are forced to 0V. The time at which the gate current abruptly increases above a threshold value (1mA/mm in this work) is defined as TTF.

Fig. 2 shows the lifetime comparison of devices featuring the three process options and the same gate geometry (W_G=100μm and L_G=0.8μm). The TTF values are extrapolated from Weibull plots at different gate bias stress, while the test temperature is 150 °C and the failure rate (F) is 1%. A double V_G dependency is observed in the lifetime plot, suggesting different breakdown

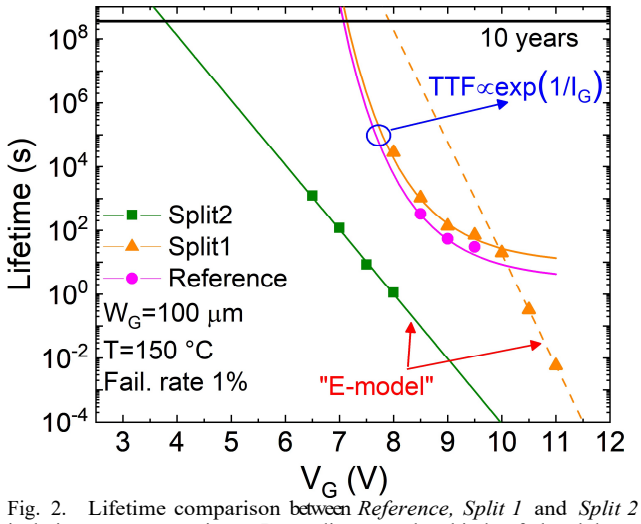


Fig. 2. Lifetime comparison between *Reference, Split 1* and *Split 2* isolation process options. Depending on the kind of breakdown mechanism, if area or isolation related, the TTF are fitted with the "E-model" or with the "TTF ∝ exp (1/I *Ginit*)" model, respectively. Failure criterion: 1% of failure at 150 °C extrapolated from the Weibull plots.

mechanisms. In particular, two different field acceleration (TTF vs V_G) fitting laws have been employed: as will be discussed in the subsections *III A* and *B*, a simple "E-model" provides a good fitting when the damage occurs along the active gate area, whereas, a "TTF ∝ exp((1/I$_G$)" is more suitable in the case of breakdown through the isolation region, i.e. the region where the gate finger intersects the N-implanted area (Fig. 1b).

Overall, from Fig. 2, it emerges that devices fabricated with the process *Split 2* show the lowest gate robustness, with a maximum applicable gate voltage for 10 years of lifetime of ~ 4V. Instead, devices featuring *Reference* and *Split 1* process show higher lifetime, i.e., they can withstand at least 7V on the gate guaranteeing a lifetime of 10 years at 150°C.

A. Gate Area and Edges Dependency

To understand the root causes of the different V_G dependency shown in Fig.2 and the related breakdown

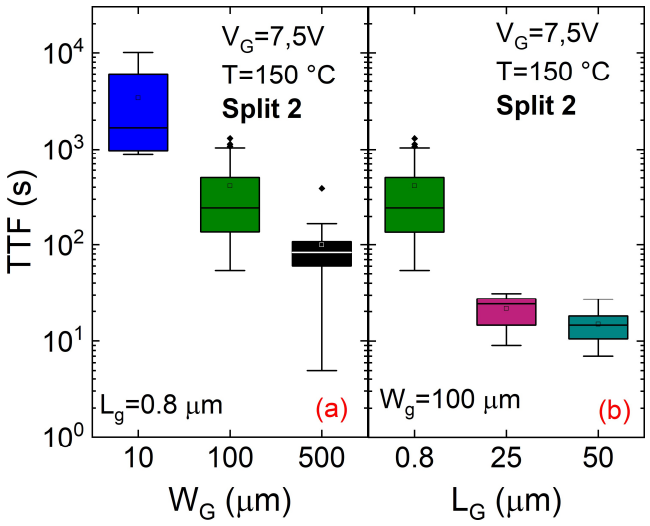


Fig. 3. (a) Gate width and (b) gate length dependency of the TTF at V_G=7.5 V and T=150 °C for devices fabricated with the process *Split 2*. About 16 devices per group have been stressed. TTF scales with both W_G and L_G.

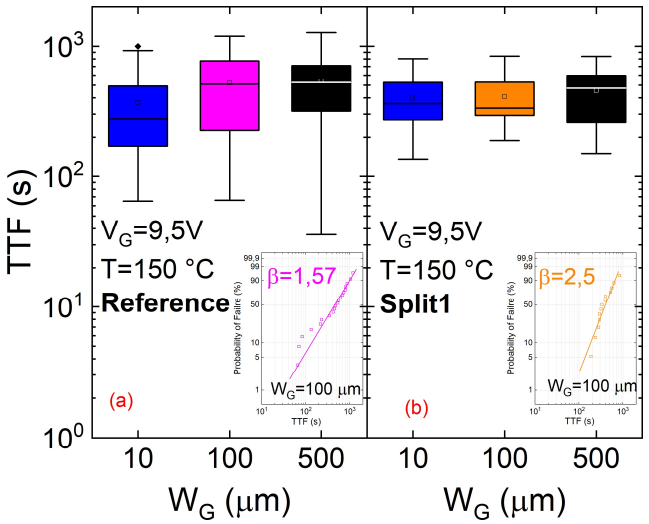


Fig. 4. Gate width dependency of the TTF at V_G=9.5 V and T=150 °C for devices fabricated with (a) Reference and (b) *Split 1* process option. In both cases, TTF does not scale with W_G. The insets show the Weibull plot of devices featuring W_G=100μm. Different TTF distribution (Weibull slope β) are observed.

mechanisms, gate area- and perimeter-dependent analyses have been performed on devices featuring different isolation options.

In Fig. 3, it is possible to notice that the TTF of the DUTs isolated with process *Split 2* shows both (a) gate width (W_G) and (b) gate length (L_G) dependency. The wider (longer) W_G (L_G), the lower TTF, meaning that a gate area-dependent breakdown mechanism occurs. Most probably, the deposition of the SiN hard mask layer directly on top of the p-GaN layer and its subsequent removal before the gate metal stack deposition, gives rise to highly defective Schottky junction, eventually leading to premature area-dependent gate failure (short lifetime).

In contrast, by observing Fig. 4, the TTF does not show neither gate area nor perimeter dependency in both *Reference* (a) and *Split 1* (b) processes, since it does not scale with W_G. The lack of area and perimeter dependency suggests that the breakdown is occurring at a more localized position, i.e., the region where the gate finger is intersecting with the isolation (see Fig. 1b), as observed in Fig. 1c through optical microscopy [16]. Despite the two process options show a similar mean TTF (Fig. 4), their distribution is different, as shown in the insets of Fig. 4 (a) and (b). In particular, the *Reference* process shows a worse distribution, leading to a lower Weibull slope (β=1.5 instead of 2.5 as for split 1), hence, to a shorter TTF extrapolated at F=1% (such behavior has been observed for all the gate voltages employed for the CVS tests). As a result, the maximum extrapolated applicable gate voltage is slightly smaller (see Fig. 2). Such difference might be ascribed to shallower and less uniform implant at the gate edge, and/or to possible damages of the passivation caused by the N-implant in the case of the *Reference* process. Differently, a uniform N-implant is expected

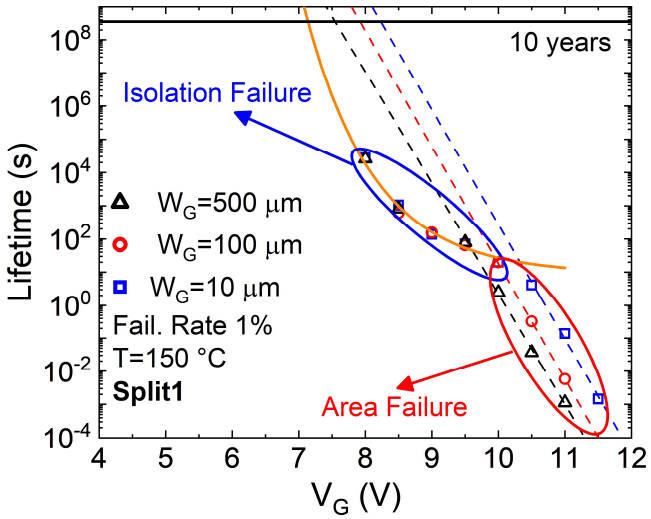


Fig. 5. Lifetime plot in the case of *Split 1* process on devices with three different gate width (W_G). Different V_G dependencies of the TTF, ascribed to different failure mechanisms, are observed. Failure criterion: 1% of failure at 150 °C extrapolated from the Weibull plots, with slope $\beta \approx 2.5$ (not shown).

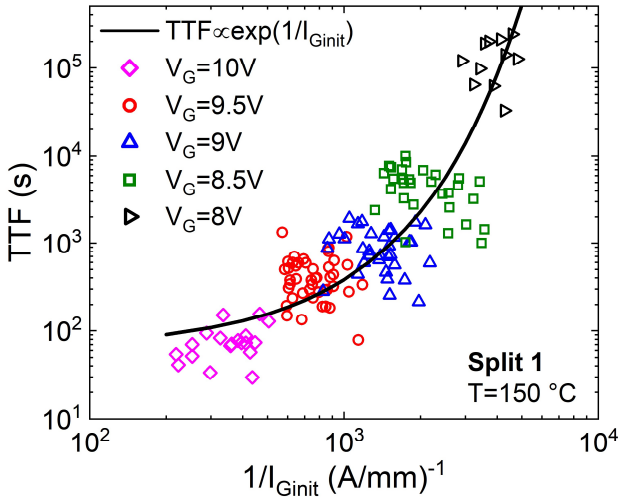


Fig. 6. Correlation between the inverse of the initial gate leakage current (I_{Ginit}), monitored at the beginning of CVS tests, and the time-to-failure, in the case of Split 1. An exponential relationship has been identified [13] by means of a statistical analysis at T= 150 °C.

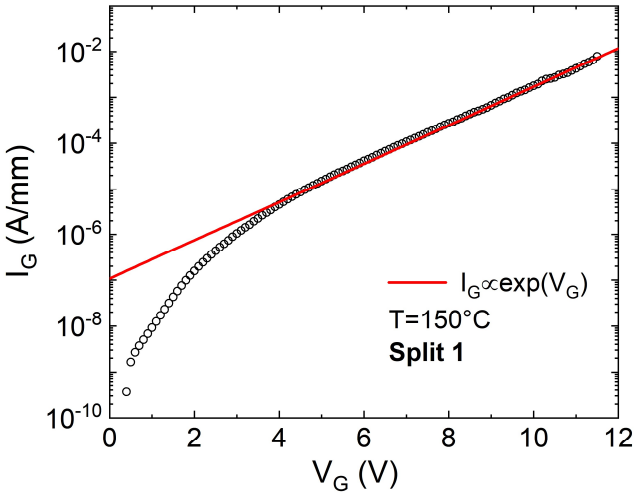


Fig. 7. Measured gate leakage characteristics (symbols) and fitting model (line) at T=150 °C in the case of Split 1. For $V_G \geq 4$V the gate current shows a purely exponential dependency.

for the *Split1* and the possible dielectric damage is completely avoided since it is deposited after the implantation.

Fig. 5 shows the lifetime plot for devices featuring different W_G (10 μm, 100 μm and 500 μm) in the case of isolation process *Split 1*. It can be noticed that TTF shows a double gate bias stress dependency, meaning that two failure mechanisms are competing. At relatively low V_G the isolation failure is the dominant one, since the extrapolated TTF values at F=1% for devices with different W_G are almost identical (Fig. 5, isolation failure). At relatively high gate voltages, area dependency is observed and as expected, the wider the gate area, the lower the V_G at which isolation breakdown shows up, e.g. 10.5 V and 10.0 V for DUTs with W_G=10 μm and 100 μm, respectively. This is due to higher failure probability along a wider gate area.

In the previous work [16], it was hypothesized that the exponential increase in TTF at V_G=8 V, over that at 8.5 V, was due to a possible switch of the failure mechanism. In this work, thanks to long-term CVS tests on device with different W_G, the lack of area dependency can be confirmed also at relatively low stress voltages, meaning that the isolation breakdown is still occurring. Therefore, as will be explained in the next subsection (*III B*), the E-model is not suitable to fit the relationship between TTF and V_G when the failure is related to the isolation region.

B. *Field Accelerated Fitting Models*

Two TTF vs V_G models have been employed to extrapolate both the area and isolation related lifetimes. For the first case a good fitting have been achieved with an "E-model" (or "V_G-model"), following the exponential relationship:

$$TTF \propto \exp(V_G). \quad (1)$$

The E-model is intrinsically developed for area-dependent breakdown since it is based on the percolation theory characterized by a probability of failure which increases with the gate area [24], thus, suitable in this case.

In the case of a more localized failure, such as the one occurring at the isolation region, a correlation between the time-to-failure and the correspondent initial gate leakage (I_{Ginit}), monitored at the beginning of the CVS tests, when the devices are still fresh, has been found. By observing Fig. 6, an exponential relationship between TTF and $1/I_{Ginit}$ is seen as reported in [13]:

$$TTF \propto \exp(1/I_{Ginit}); \quad (2)$$

although the gate leakage at relatively high V_G is dominated by an area component. Based on the strong correlation between TTF and I_{Ginit} we may argue that a fraction of the gate current, possibly featuring similar gate voltage dependency, contributes to the damage in the isolation region. Therefore, the higher the gate leakage, the higher the fraction of current triggering isolation breakdown, the shorter the TTF.

Afterwards, the relationship between the gate leakage and the gate voltage has been determined by analyzing the

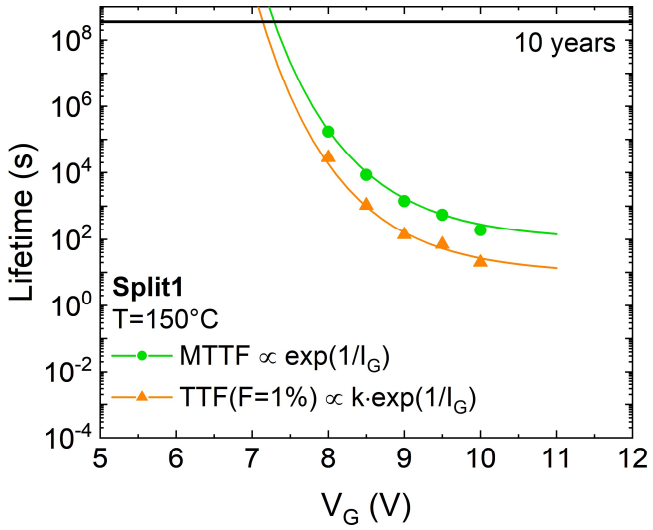


Fig. 8. Lifetime plot comparison in the case of the TTF extrapolate with F=1% (triangles) and the MTTF (circles). The process is the *Split 1* and the temperature is 150 °C. To better fit the TTF at F=1% the empirical model has been multiplied by a constant k<1.

characteristics reported in Fig. 7. For the DUTs, an exponential law has been adopted to reproduce I_G for relatively large V_G values. In particular, for $V_G > 4$ V, I_G can be modeled as follows:

$$I_G \propto \exp(V_G). \quad (3)$$

Finally, the empirical model can be derived by simply replacing Eq. (3) into Eq. (2). From Fig. 8, it is possible to notice the accurate fitting of the MTTF for V_G lower than 10 V, hence in the bias range dominated by the isolation breakdown. Then, in order to fit the TTF at F=1%, a multiplicative constant (k<1) was used.

C. Temperature Dependency

Fig. 9 shows the temperature dependency of the time-dependent gate breakdown at V_G= 9.5V on devices featuring three different gate widths (10μm, 100μm and 500 μm). A

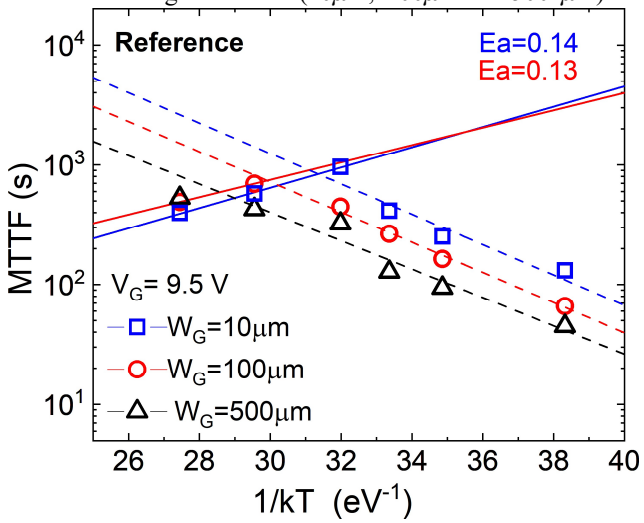


Fig. 9. Arrhenius plot at V_G=9.5 V showing the mean time-to-failure (MTTF) of devices featuring three different gate widths (W_G): 10μm , 100μm and 500 μm. The fitting dashed and solid lines are referred to the area failure and isolation region failure, respectively. The isolation process option is the Reference.

different T-dependency can be observed, depending on the failure mechanism.

At relatively low temperatures, an area-dependent TTF can be observed (TTF scales with W_G). In addition, TTF increases with the temperature, hence showing a positive T-dependency. The combination of such two evidences suggests and confirm the role of the impact ionization, in the high-field depletion region of the Schottky junction, on the gate failure [15, 25]. In particular, holes generated by impact ionization in such region are accelerated towards the AlGaN barrier, acquiring kinetic energy and possibly causing structural defects in the AlGaN barrier layer. Further details on the degradation mechanisms occurring at low temperatures can be found in [15].

On the contrary, at relatively high temperature a negative T-dependency and a lack of area-dependency can be observed. By increasing the temperature, the impact ionization mechanism is exponentially attenuated, reducing the probability of failure along the gate area. Consequently, the isolation failure shows up, featuring an activation energy of ~0.14 eV.

Finally, as expected, the temperature of transition between gate area and isolation failure is area dependent. The larger the gate area, the lower the transition temperature. By increasing the gate area, the probability of failure along it increases as well, therefore, a higher temperature is required to further reduce the root cause leading to area breakdown, i.e. impact ionization. More specifically, single finger devices featuring a gate width of 10 μm and 100 μm, and stressed with V_G=9.5V, are affected by area related failure at temperatures below 90 °C and 120 °C, respectively. In the case of devices with W_G=500 μm the isolation breakdown at V_G=9.5V has been observed only at T=150 °C.

IV. Conclusion

An in-depth analysis of the high-temperature time-dependent gate breakdown of p-GaN HEMTs has been proposed in this paper. Three isolation process splits, aimed at improving the gate breakdown occurring through the isolation region, have been compared by means of CVS tests on device featuring different gate areas. Results showed that, depending on the process and on the stress conditions, DUTs can be affected by irreversible breakdown occurring along the active gate area or through the isolation region.

The process Split 2, which consists in patterning the pGaN layer, depositing the passivation, carrying out the nitrogen implantation, removing the passivation and depositing the TiN metal, turned out to be less robust, showing an area related gate breakdown. Possibly, the deposition of the passivation directly on top of the pGaN and the subsequent etching prior to TiN metal deposition, introduces many surface defects making the Schottky junction highly defective.

In fact, by adopting a similar procedure, but depositing the TiN interlayer directly on top of the pGaN before passivation (Reference), a more robust gate region is attained. However, the adoption of higher gate voltages with respect to Split 2, gives rise to time-dependent isolation breakdown. The latter

can be slightly improved by adopting process Split 1, which consists of implanting directly through the TiN interlayer prior to patterning and passivation steps. Such a procedure ensures a uniform N-implant and avoids possible damage to passivation.

Concerning the shows up of the two different breakdown mechanisms (area and isolation related), the adoption of different acceleration laws has been suggested to model their voltage dependency. In particular, the TTF related to the gate area can be fitted with a simple "E-model", whereas an empirical approach is needed in the case of failure at the isolation region, emphasizing the detrimental role of the gate leakage.

Moreover, a temperature-dependent analysis has been carried out to extrapolate the activation energy of the degradation mechanism causing the isolation failure, i.e. ~0.14 eV. Finally, the isolation failure shows up at relatively high temperatures, with an area-dependent threshold temperature value. The wider the area, the higher the temperature at which the isolation breakdown occurs.

ACKNOWLEDGMENT

Part of this work is funded by iRel40. iRel40 is a European co-funded innovation project that has been granted by the ECSEL Joint Undertaking (JU) under grant agreement No 876659. The funding of the project comes from the Horizon 2020 research programme and participating countries. National funding is provided by Germany, including the Free States of Saxony and Thuringia, Austria, Belgium, Finland, France, Italy, the Netherlands, Slovakia, Spain, Sweden, and Turkey.

REFERENCES

[1] Bimal K. Bose,"Energy, Environment, Power Electronics, Renewable Energy Systems, and Smart Grid," in Power Electronics in Renewable Energy Systems and Smart Grid: Technology and Applications , IEEE, 2019, pp.1-83.

[2] B. Kroposki, C. Pink, R. DeBlasio, H. Thomas, M. Sim ões and P. K. Sen, "Benefits of Power Electronic Interfaces for Distributed Energy Systems," in IEEE Transactions on Energy Conversion, vol. 25, no. 3, pp. 901-908, Sept. 2010.

[3] T. P. Chow, "Wide bandgap semiconductor power devices for energy efficient systems," 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2015, pp. 402-405.

[4] L. Spaziani and L. Lu, "Silicon, GaN and SiC: There's room for all: An application space overview of device considerations," 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2018, pp. 8-11.

[5] N. Kaminski, "State of the art and the future of wide band-gap devices," 2009 13th European Conference on Power Electronics and Applications, 2009, pp. 1-9.

[6] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155-2163, May 2014, doi: 10.1109/TPEL.2013.2268900. J. Mill án, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2155-2163, May 2014.

[7] O. Ambacher et al.,"Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures" , Journal of Applied Physics 85 , 3222-3233 (1999).

[8] X. Huang, Z. Liu, F. C. Lee and Q. Li," Characterization and Enhancement of High-Voltage Cascode GaN Devices," in IEEE Transactions on Electron Devices, vol. 62, no. 2, pp. 270-277, Feb. 2015.

[9] C. Yang, J. Xiong, J. Wei, J. Wu, B. Zhang, X. Luo, "High performanceenhancement-mode AlGaN/GaN MIS HEMT with selective fluorinetreatment", Adv Condens Matter Phys 2015:267680, 2015.

[10] D. Marcon, M. Van Hove, B. De Jaeger, N. Posthuma, D. Wellekens, S. You, X. Kang, Tian-Li Wu, M. Willems, S. Stoffels, and S. Decoutere "Direct comparison of GaN-based e-mode architectures (recessed MISHEMT and p-GaN HEMTs) processed on 200mm GaN-on-Si with Au-free technology", Proc. SPIE 9363, Gallium Nitride Materials and Devices X, 936311, 2015.

[11] N. E. Posthuma et al., "An industry-ready 200 mm p-GaN E-mode GaN- on-Si power technology," 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2018, pp. 284-287.

[12] M. Ťapajna, O. Hilt, E. Bahat-Treidel, J. Würfl and J. Kuzmík, "Gate Reliability Investigation in Normally-Off p-Type-GaN Cap/AlGaN/GaN HEMTs Under Forward Bias Stress," in IEEE Electron Device Letters, vol. 37, no. 4, pp. 385-388, April 2016.

[13] A.N. Tallarico, S. Stoffels, P. Magnone, N. Posthuma, E. Sangiorgi, S. Decoutere, C. Fiegna, Investigation of the p-GaN gate breakdown in forward-biased GaN-based power HEMTs, IEEE Electron Device Lett 38 (1) (2017) 99–102, https://doi.org/10. 1109/LED.2016.2631640.

[14] S. Stoffels et al., "Failure mode for p-GaN gates under forward gate stress with varying Mg concentration," 2017 IEEE International Reliability Physics Symposium (IRPS), 2017, pp. 4B-4.1-4B-4.9.

[15] A.N. Tallarico, N.E. Posthuma, B. Bakeroot, S. Decoutere, E. Sangiorgi, C. Fiegna, "Role of the AlGaN barrier on the long-term gate reliability of power HEMTs with p-GaN gate", Microelectronics Reliability, Vol. 114, 2020.

[16] A. N. Tallarico et al., "Gate Reliability of p-GaN HEMT With Gate Metal Retraction," in IEEE Transactions on Electron Devices, vol. 66, no. 11, pp. 4829-4835, Nov. 2019.

[17] P. Moens, A. Stockman, A physical-statistical approach to AlGaN/GaN HEMT reliability, Proc. IEEE Int. Rel. Phys. Symp. (IRPS), Monterey, CA, USA, Apr. 2019, https://doi.org/10.1109/IRPS.2019.8720521.

[18] M. Meneghini et al., "OFF-State Degradation of AlGaN/GaN Power HEMTs: Experimental Demonstration of Time-Dependent Drain-Source Breakdown," in IEEE Transactions on Electron Devices, vol. 61, no. 6, pp. 1987-1992, June 2014, doi: 10.1109/TED.2014.2318671.

[19] M. Millesimo, N. Posthuma, B. Bakeroot, M. Borga, S. Decoutere and A. N. Tallarico, "Impact of Structural and Process Variations on the Time-Dependent OFF-State Breakdown of p-GaN Power HEMTs," in IEEE Transactions on Device and Materials Reliability, vol. 21, no. 1, pp. 57-63, March 2021.

[20] C. Fleury et al., "Statistics and localisation of vertical breakdown in AlGaN/GaN HEMTs on SiC and Si substrates for power applications," Microelectron. Rel., vol. 53, nos. 9–11, pp. 1444–1449, 2013.

[21] M. Borga et al., "Impact of substrate resistivity on the vertical leakage, breakdown, and trapping in GaN-on-Si E-mode HEMTs," IEEE Trans. Electron Devices, vol. 65, no. 7, pp. 2765–2770, Jul. 2018.

[22] D. Marcon et al., "Reliability analysis of permanent degradations on AlGaN/GaN HEMTs," IEEE Trans. Electron Devices, vol. 60, no. 10, pp. 3132–3141, Oct. 2013.

[23] R. Degraeve, B. Kaczer, and G. Groeseneken, "Degradation and breakdown in thin oxide layers: Mechanisms, models and reliability prediction," Microelectron. Rel., vol. 39, no. 10, pp. 1445–1460, 1999.

[24 J. Suñé, I. Placencia, N. Barniol, E. Farrés, F. Martín, X. Aymerich, "On the breakdown statistics of very thin SiO2 films," Thin Solid Films" vol. 185, no. 2, pp. 347-362, 1990.

[25] A. N. Tallarico et al., "PBTI in GaN-HEMTs With p-Type gate: Role of the aluminum content on DVTH and underlying degradation mechanisms," IEEE Trans. Electron Devices, vol. 65, no. 1, pp. 38–44, Jan. 2018. doi: 10.1109/TED.2017.2769167.