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Impact of structural and process variations on the time-dependent off-state breakdown of p-gan power hemts

This is the final peer-reviewed author's accepted manuscript (postprint) of the following publication:

*Published Version:*

Millesimo M., Posthuma N., Bakeroort B., Borga M., Decoutere S., Tallarico A.N. (2021). Impact of structural and process variations on the time-dependent off-state breakdown of p-gan power hemts. IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, 21(1), 57-63 [10.1109/TDMR.2020.3048274].

*Availability:*

This version is available at: <https://hdl.handle.net/11585/833392> since: 2021-09-24

*Published:*

DOI: <http://doi.org/10.1109/TDMR.2020.3048274>

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This is the post-print peer-review accepted manuscript of:

M. Millesimo *et al.* "Impact of Structural and Process Variations on the Time-Dependent OFF-State Breakdown of p-GaN Power HEMTs" in *IEEE Transactions on Device and Materials Reliability*, Vol. 21, No. 1, March 2021 DOI: 10.1109/TDMR.2020.3048274.

The published version is available online at:

<https://ieeexplore.ieee.org/document/9311207>

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# Impact of Structural and Process Variations on the Time-Dependent OFF-State Breakdown of p-GaN Power HEMTs

M. Millesimo, N. Posthuma, B. Bakeroot, M. Borga, S. Decoutere, and A. N. Tallarico

**Abstract**— In this paper, we present an extensive investigation of the time-dependent drain breakdown occurring in GaN-on-Si power HEMTs with p-GaN gate under long-term OFF-state stress. In particular, the time-dependent breakdown induced by high-temperature-reverse-bias stress is investigated as a function of different process and structural variations. Main results demonstrate that, by varying the gate-to-drain distance ( $L_{GD}$ ) and the field plates configuration, the physical location of failure changes as well. If  $L_{GD}$  is relatively short (3  $\mu\text{m}$ ), the time-dependent breakdown occurs through the GaN channel layer between drain and source. In this case, a thinner GaN layer significantly improves the device robustness to long-term OFF-state stress. If  $L_{GD}$  is relatively long ( $\geq 4$   $\mu\text{m}$ ), the failure occurs between the two-dimensional electron gas (2DEG) and the source field plates. In this second case, the GaN layer thickness and  $L_{GD}$  have no significant impact on the time-dependent breakdown, whereas the field plate lengths can be optimized to reduce the area exposed to high electric fields, hence limiting the probability of failure. Finally, the role of the AlGaN barrier layer has been analyzed as well. If  $L_{GD} = 3$   $\mu\text{m}$ , a thinner AlGaN layer is preferred, whereas if  $L_{GD} \geq 4$   $\mu\text{m}$ , a thicker layer with lower aluminum content gives rise to longer time to breakdown under OFF-State stress.

**Index Terms**— Gallium Nitride, OFF-state reliability, p-type gate, HEMTs, breakdown mechanisms, field plates, time-dependent breakdown.

## I. INTRODUCTION

GAN-BASED high electron mobility transistors (HEMTs) are promising candidates for high-efficiency high-voltage power electronics applications thanks to their superior electrical characteristics including high breakdown voltage, low on-resistance, and fast switching speed [1]–[4]. Solutions for enhanced-mode operation are already on the market [5]–[7]. Among those, the lateral AlGaN/GaN HEMT with p-GaN gate grown on Silicon substrates have proven to be one of the solutions offering the best stability and reliability at low cost and high performance [8]–[11]. Nevertheless, to optimize further the performance and to improve the long-term reliability, it is very important to identify and understand the main and most critical breakdown and degradation mechanisms.

In a power converter, GaN-based HEMTs are repeatedly

switched between ON-state (high current) and OFF-state (high voltage) at relatively high frequency. In the latter condition, the transistor must sustain a high drain bias that might trigger degradation processes which limit the device reliability and lifetime. Such time-dependent degradation mechanisms can be classified as follows: i) vertical drain-to-substrate breakdown of the buffer; ii) lateral drain-to-source breakdown in the GaN layer; iii) surface breakdown in the gate-to-drain access region.

The vertical breakdown has been investigated in depth by several groups. Zhou et al. [13] demonstrated that both acceptor and donor traps in the buffer layer are responsible for the drain-to-substrate conduction paths, eventually leading to premature breakdown. Time and temperature dependencies have been reported in [14, 15] and, relevant solutions concerning the buffer and the substrate layers have been proposed in [16]–[19].

The lateral breakdown is observed as an increase of the drain-to-source leakage current, mainly linked to short-channel effects [20] and/or punch-through effects [21]. The high drain voltage causes a current flow through the non-depleted region located deep into the unintentionally doped (uid) GaN under the gate. Such current strongly depends on the extension of the depleted region, which is influenced by 2DEG density and gate length [21]. A time-dependent breakdown mechanism has been identified [22]. The adoption of a double AlGaN/GaN/AlGaN heterostructure helps to better confine the 2DEG charge with a consequent reduction of the drain leakage [23].

Finally, surface breakdown has been found to mainly affect the p-type gate HEMTs with a Schottky junction. In particular, defects at the drain-side edge of the gate may cause a premature failure of the gate and/or of the passivation layer [24]. Such defects may be due to inverse piezoelectric effects [25] or to the presence or creation of defects [26]–[27] which, in combination with the high drain voltage, can promote the injection of electrons from the Schottky junction into the AlGaN barrier layer, eventually leading to gate breakdown [28]–[29]. The adoption of field plates partially suppresses this phenomenon redistributing the electric field in the gate-to-drain access region, also improving the static breakdown voltage [30]–[31].

Furthermore, a significant effort has been provided for the investigation of the current collapse mechanism [32], proposing different solutions aimed at suppressing such effect, i.e. the use of gate and source field plates [33] and/or optimized buffer

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layers [34].

This paper aims at identifying the root causes leading to time-dependent breakdown of p-GaN HEMTs when subjected to high drain voltage long-term stress. Different field plates configurations combined with various AlGaIn barrier and uid GaN layer variations have been experimentally investigated, to the best of our knowledge, for the first time. In particular, thanks to high-temperature-reverse-bias (HTRB), also referred to as time-dependent breakdown (TDB), and OFF-State leakage experimental tests, in combination with TCAD simulations, the role and the importance of structural and process parameters, fundamental for device optimization, are discussed in terms of TDB and related lifetime.

## II. TEST STRUCTURES AND EXPERIMENTAL DETAILS

P-GaN gate HEMTs rated at 200V fabricated on 200 mm Si (111) wafers by imec are considered in this study. The epi-stack grown on top of silicon features a 3.3  $\mu\text{m}$  thick superlattice buffer, with a C-doped GaN back-barrier, 200 nm, 300 nm or 400 nm thick uid-GaN channel, and different AlGaIn barrier thickness configurations. Then, a passivation layer, consisting in a thin  $\text{Al}_2\text{O}_3$  layer and a thicker  $\text{SiO}_2$  layer, is deposited in the access regions, whereas the gate is composed by 80 nm magnesium-doped p-GaN layer covered by titanium nitride (TiN) as gate metal. The structure features three field plates as shown in Fig. 1, namely a gate metal field plate (FP1), a source ohmic metal field plate (FP2) and a source metal1 field plate (FP3). More structural and process details can be found in [35].

Four sets of devices are defined, characterized by different gate-to-drain distances ( $L_{GD}$ ), ranging from 3 to 6  $\mu\text{m}$ , and field plate lengths ( $L_{FP}$ ), as summarized in Table I.

OFF-state experiments, both high-temperature-reverse-bias and OFF-State leakage tests, have been performed with a parameter analyzer Keysight B1505 by applying a high

TABLE I

P-GaN HEMTs WITH DIFFERENT STRUCTURAL VARIANTS. ALL OTHER PARAMETERS IN TERMS OF GEOMETRY AND PROCESS ARE THE SAME.

Device	$L_{GD}$ ( $\mu\text{m}$ )	$L_{FP1}$ ( $\mu\text{m}$ )	$L_{FP2}$ ( $\mu\text{m}$ )	$L_{FP3}$ ( $\mu\text{m}$ )
Device 1	3	0.35	0.65	1
Device 2	4	0.65	1.35	2
Device 3	5	1	2	3
Device 4	6	1	2	3

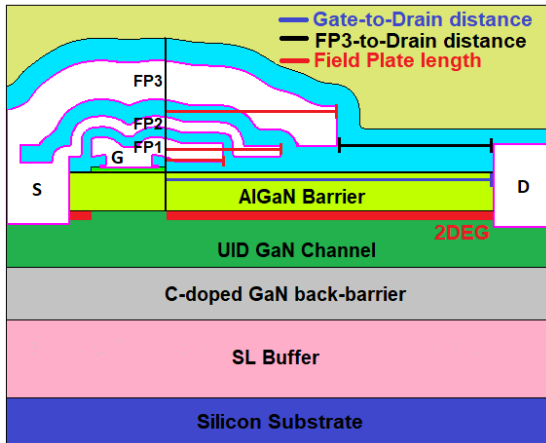


Fig. 1. Schematic representation of the device under test (not in scale).

constant drain bias up to stress and failure voltage, respectively, while gate, source and bulk contacts were forced to 0 V. The drain, source, gate and substrate currents were monitored during the tests. The failure drain voltage ( $V_{DF}$ ) and the time-to-failure (TTF) have been evaluated with OFF-State leakage (drain voltage sweep) and constant voltage stress (CVS or HTRB or TDB), respectively. They are defined as the voltage and the time, respectively, in which the drain current suddenly increases or reaches 1 mA/mm.

All tests have been carried out at the temperature ( $T$ ) of 210  $^{\circ}\text{C}$  to limit the stress voltage and the time-to-failure below 500 V and  $10^5$  s, respectively. Sentaurus TCAD simulations have been performed to evaluate the electric field distribution along the device.

## III. RESULTS AND DISCUSSION

### A. Preliminary OFF-State leakage and Stress Tests

The results of the OFF-State leakage tests performed on Device 1 with the shortest  $L_{GD}$  and Device 4 with the longest  $L_{GD}$ , are shown in Fig. 2 (a) and (b), respectively. Both devices feature a GaN channel and an AlGaIn thickness of 400 nm and 14 nm, respectively, and 25% of aluminium content. Fig. 2 shows that the drain leakage current ( $I_D$ ) mainly flows towards the source ( $I_D \approx |I_S|$ ). In particular, as the device approaches the breakdown a large current is measured on the source contact ( $I_S$ ), whereas the gate ( $I_G$ ) and the substrate ( $I_B$ ) currents remain low, thus excluding the gate breakdown and the vertical breakdown between drain and substrate as, otherwise a sharp increase in  $I_G$  or  $I_B$  would be observed. A similar trend in currents, i.e.  $I_D \approx |I_S|$ , has been observed for Devices 2 and 3

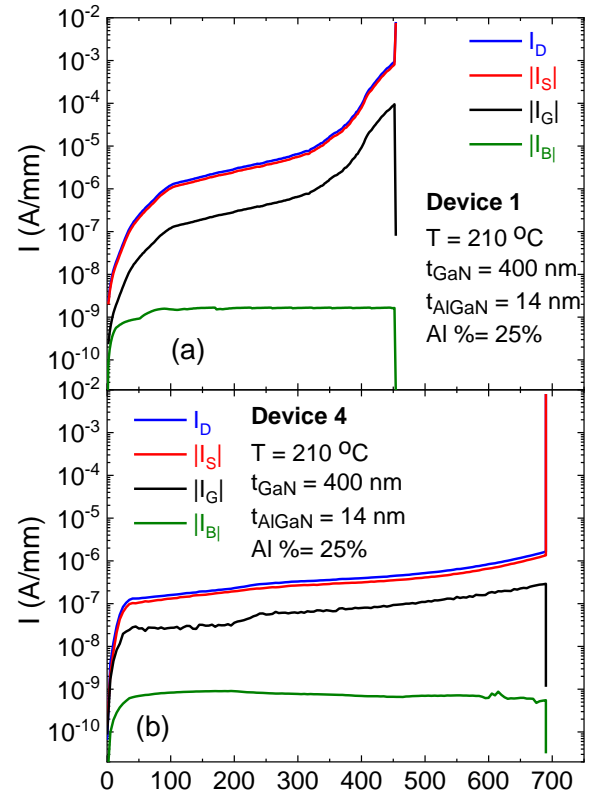


Fig. 2. Drain, source, gate and substrate current monitored during OFF-state leakage test for (a) Device 1 and (b) Device 4. During the test, gate, source, and substrate are forced to 0 V, the temperature is 210 $^{\circ}\text{C}$ .

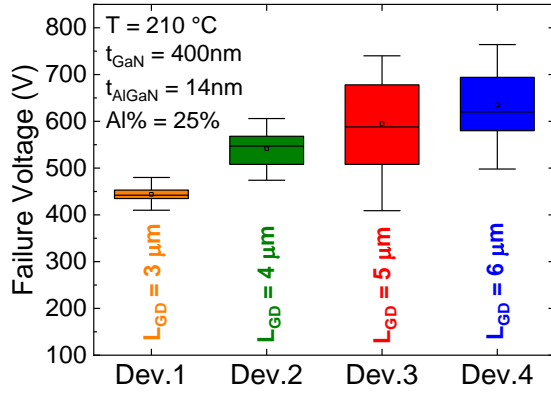


Fig. 3. Failure voltages at  $I_D = 1$  mA/mm attained from OFF-State leakage tests for the four device types as summarized in Table I. 20 samples for each type have been measured. Note that by reducing  $L_{GD}$ , the field plates length are shortened as well (Table I) to guarantee a minimum distance between FP3 and drain metal (see Fig. 1).

(not shown). Moreover, by reducing  $L_{GD}$ , the drain and source currents increase due to increasing longitudinal electric field in the channel layer as  $L_{GD}$  and field plate lengths are shortened, leading also to a lower failure voltage. In addition, the gate leakage increases due to the higher vertical electric field at the drain-side edge of the gate (not shown), again caused by shortening gate field plate. Finally, the substrate current is rather insensitive to  $L_{GD}$  variations.

Fig. 3 confirms the dependence of the failure voltage ( $V_{DF}$ ) on  $L_{GD}$  and field plate lengths.  $V_{DF}$  is extrapolated from OFF-State leakage tests (Fig. 2) performed on 20 samples for each device family reported in Table I. Note that, the shorter  $L_{GD}$  and field plate lengths, the lower  $V_{DF}$ , further confirming the lack of vertical breakdown between drain and substrate, since it would be insensitive to  $L_{GD}$  and field plate lengths variations. However, the lowest  $V_{DF}$  is still substantially higher than the

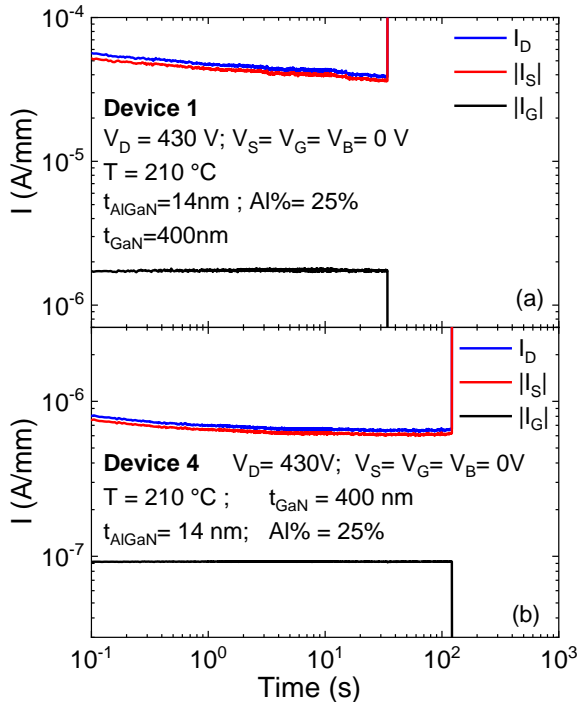


Fig. 4. Drain, source and gate current monitored during constant voltage stress (CVS or HTRB) test for (a) Device 1 and (b) Device 4.

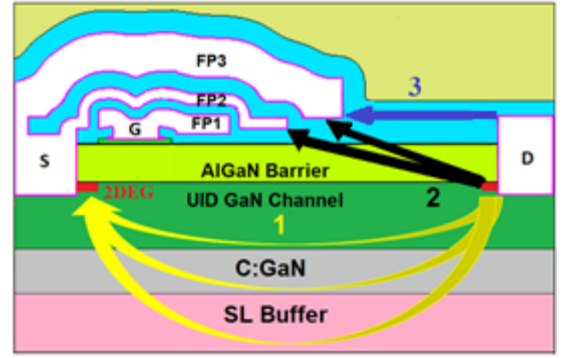


Fig. 5. Possible breakdown mechanisms between drain and source: 1) Drain-to-source breakdown through the UID GaN channel or C-doped GaN back-barrier or super lattice buffer layers; 2) breakdown between the 2DEG and the source field plates; 3) FP3-to-drain metal breakdown in the passivation layer.

device's voltage rating, i.e. 200 V. The measured failure voltages were used as reference values for the definition of the drain biases that were used in the constant voltage stress.

Fig. 4 shows a representative case of CVS (or HTRB) test with  $V_D = 430$  V at  $T = 210$  °C on Device 1 (a) and 4 (b). Unlike the drain and source currents,  $I_G$  does not show variation during the stress, suggesting that no significant degradation is taking place in the gate stack. As for the OFF-State leakage test, during CVS experiments the source current suddenly increases when the device fails, following the same trend of  $I_D$  and suggesting time-dependent breakdown occurring between the drain and source contacts. The latter hypothesis is strengthened by the drain and source current decrease during the stress, usually related to charge trapping mechanisms. The substrate current is always low during the stress and failure, not shown for the sake of clarity of the figure. However, as reported in Fig. 5, the failure might occur at different locations: 1) through the uid-GaN channel or C-doped GaN or the super lattice buffer layers (yellow arrow); 2) between the 2DEG (close to drain) and the source field plates (black arrows); 3) in the passivation layer between the drain metal and field plate FP3 (blue arrow). Note that in Fig. 5 the 2DEG is depleted along the all drain access region to qualitatively indicate the high drain voltage condition.

#### B. Investigation of Breakdown Mechanisms

In order to understand the location of failure in Device 1, CVS tests have been performed on transistors featuring different thicknesses of GaN channel layer ( $t_{GaN}$ ) and AlGaN

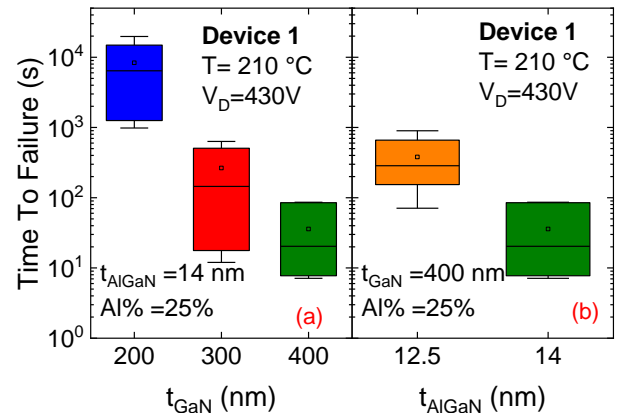


Fig. 6. Time-to-failure (TTF) extrapolated from CVS tests on Device 1 with different GaN (a) and AlGaN (b) thicknesses.

layer ( $t_{\text{AlGaIn}}$ ). Fig. 6 shows the time-to-failure (TTF) for Device 1 with  $L_{\text{GD}} = 3 \mu\text{m}$  at  $V_D = 430 \text{ V}$  and  $T = 210^\circ\text{C}$ , as a function of different  $t_{\text{GaN}}$  (a) and  $t_{\text{AlGaIn}}$  (b) values. It is noted that TTF is longer for thinner  $t_{\text{GaN}}$  (a) and  $t_{\text{AlGaIn}}$  (b). On one hand, the observed trend of the time-to-breakdown as a function of the  $t_{\text{GaN}}$ , suggests that the failures occur in the uid GaN channel layer (yellow arrow in Fig. 5). In particular, by reducing its thickness, enhanced depletion of the GaN channel is attained, effectively suppressing the drain leakage and increasing the TTF. Such effect will be further explored in the discussion of Fig. 9. On the other hand, a thinner AlGaIn barrier layer induces a lower 2DEG density due to lower induced polarization [36], again leading to a weaker depletion of the uid GaN channel layer.

Previous statements can be strengthened by Fig. 7, where the relationship between TTF and the inverse of the drain leakage current ( $I_{\text{DLS}}$ ) for a virgin device is shown as a function of different (a) GaN and (b) AlGaIn thicknesses. The initial drain leakage at the start of the stress test has been used as the  $I_{\text{DLS}}$  value. By decreasing  $t_{\text{GaN}}$  and  $t_{\text{AlGaIn}}$ , the drain leakage is reduced because of the enhanced depletion of the GaN channel layer, leading to longer TTF.

The role of the GaN channel thickness on the  $I_{\text{DLS}}$  and on the TTF has been investigated also on Device 2, 3 and 4 featuring longer  $L_{\text{GD}}$  and field plate lengths (see Table I), as shown in Fig. 8, reporting TTF as a function of  $1/I_{\text{DLS}}$  for different samples, featuring 200 nm or 400 nm  $t_{\text{GaN}}$  values. It can be observed that

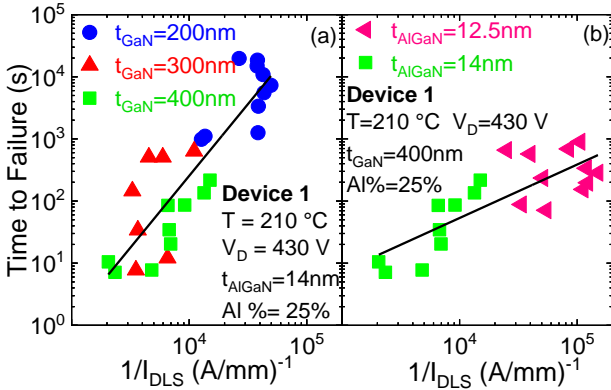


Fig. 7. Relationship between time-to-failure and inverse of the initial drain leakage current ( $1/I_{\text{DLS}}$ ), monitored at the beginning of the stress in Device 1, as a function of different (a) GaN and (b) AlGaIn thicknesses.

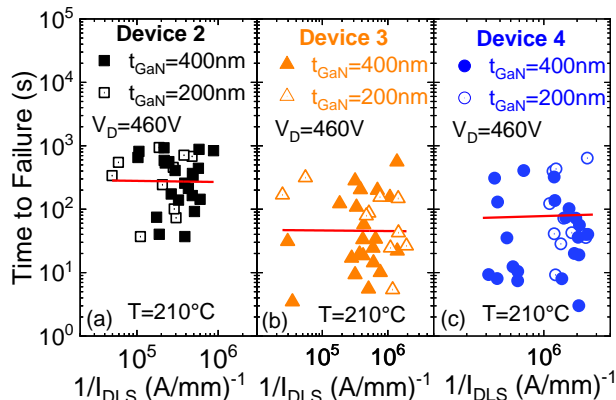


Fig. 8. Relationship between time-to-failure and inverse of the initial drain leakage current ( $I_{\text{DLS}}$ ), monitored at the beginning of the stress on (a) Device 2, (b) 3, and (c) 4 with different GaN layer thicknesses ( $t_{\text{GaN}}$ ). All devices feature the same AlGaIn barrier with same  $t_{\text{AlGaIn}} = 14 \text{ nm}$  and  $\text{Al}\% = 25\%$ .

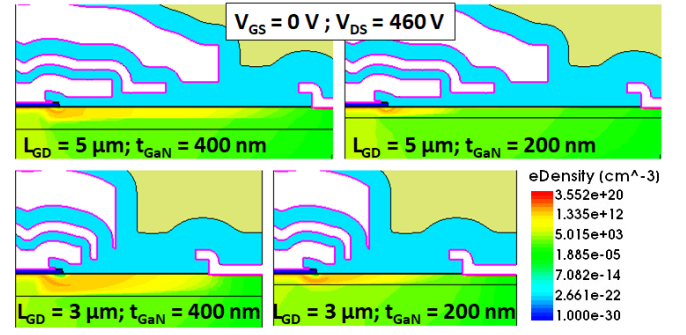


Fig. 9. Simulated electron density map with  $V_D = 460 \text{ V}$  and  $V_S = V_G = V_B = 0 \text{ V}$  on devices with different  $L_{\text{GD}}$  and GaN channel thicknesses. The thicker the GaN channel (left), the smaller the depletion region (green GaN region) between gate and drain. This is much more accentuated by reducing  $L_{\text{GD}}$  (bottom).

$I_{\text{DLS}}$  and TTF are rather insensitive to  $t_{\text{GaN}}$ , suggesting that time-dependent drain breakdown is no longer occurring through the uid GaN channel layer as for Device 1.

Fig. 9 shows the electron density map simulated under OFF-state condition with  $V_D = 460 \text{ V}$  for two different  $t_{\text{GaN}}$  (200 nm and 400 nm) and  $L_{\text{GD}}$  (3  $\mu\text{m}$  and 5  $\mu\text{m}$ ) values. The simulations indicate that devices with  $L_{\text{GD}} = 5 \mu\text{m}$  (same for  $L_{\text{GD}} = 4 \mu\text{m}$  and 6  $\mu\text{m}$ , not shown) guarantee a high level of GaN channel layer depletion under the drain-side gate edge and in the access region between gate and drain (green region, low electron density), independent of the  $t_{\text{GaN}}$ , due to combined effect of longer  $L_{\text{GD}}$  and field plate lengths. As a result, a thinner uid GaN layer has not impact on the drain-to-source leakage and TTF, as reported in Fig. 8. On the contrary, if  $L_{\text{GD}}$  is shorter (3  $\mu\text{m}$ ), a thin GaN layer is required to compensate the effect of the higher lateral electric field due to shorter drain-to-source distance and field plate lengths, as observed in Fig. 9. Note that, the shortening of the field plate lengths is mandatory for small  $L_{\text{GD}}$  in order to maintain a minimum allowable distance between the source field plate  $FP3$  and the drain metal.

The exclusion of the failure through the GaN channel layer for devices with  $L_{\text{GD}}$  longer than 3  $\mu\text{m}$  narrows the focus on the remaining two failure modes, i.e. failure 2 and 3 shown in Fig. 5. However, Device 2 features longer time-dependent drain breakdown (TTF) compared to Device 3 and 4 as shown in Fig. 8. This difference indicates that the breakdown between field plate  $FP3$  and drain-metal through the passivation layer (failure 3) can be excluded as the main failure mode, since Device 2 and 3 share the same distance from  $FP3$  to drain contact. In addition, the longer distance between  $FP3$  and the drain metal of the Device 4 should lead to the highest robustness in the case of failure 3, which is not in agreement with the observations. Overall, it can be concluded that, when submitted to HTRB stresses, devices with  $L_{\text{GD}} \geq 4 \mu\text{m}$  (Device 2, 3 and 4) most likely break in the region located between the 2DEG (GaN channel) and the source field plates (Fig. 5, failure 2).

The longer TTF of the Device 2 (Fig. 8), compared to device 3 and 4, can be explained by the TCAD simulated profile of the electric field under the field plates, i.e. the region of interest for failure 2 during OFF-state stress. Fig. 10 (a) and (b) show the electric field distribution at  $V_D = 460 \text{ V}$  in the case of Device 2 and 4, respectively, whereas Fig. 11 reports the electric fields calculated under the field plates in the case of Device 2, 3 and 4 along the cutline shown in Fig. 10. The magnitude of the



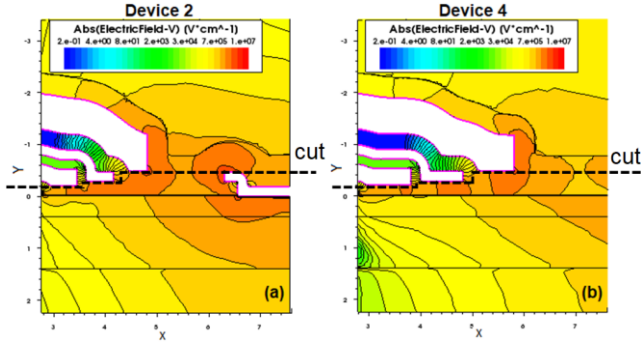


Fig. 10. TCAD Simulated electric field distribution at  $V_{DS} = 460$  V in the case of (a) Device 2 and (b) Device 4. All other contacts are set to 0 V.

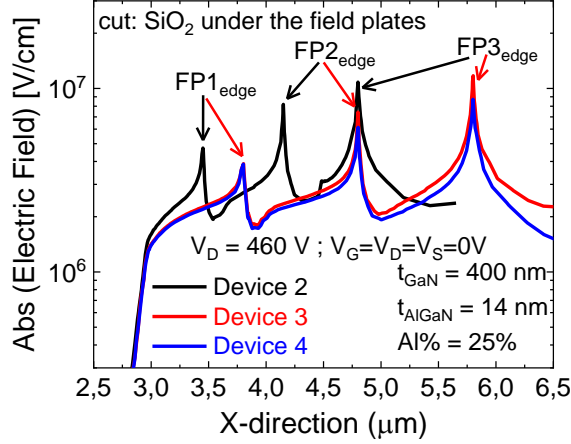


Fig. 11. Simulated electric field distribution monitored under the field plates on Device 2, 3 and 4 along the cutline shown in Fig. 10.

electric field peaks under the field plates do not change significantly by changing  $L_{GD}$  (Fig. 11), as a matter of fact the TTF of Device 3 and 4 are similar (Fig. 8), whereas the area exposed to high fields is smaller in Device 2 because of shorter field plates (Fig. 10). As a result, since the time-dependent breakdown through the  $\text{SiO}_2$  (dielectric passivation layer) is strongly area dependent [37], the smaller the area subjected to the high electric field, the lower the probability of defects creation, the longer the time to failure. Moreover, the high electric field peak values at the field plates edges, combined with the high temperature ( $210^\circ\text{C}$ ), strengthens the hypothesis of the failure through the dielectric layer in relatively short stress time (TTF  $\sim 100$  s), in the case of Device 2, 3 and 4.

### C. Lifetime Extrapolation

Once the different locations of failure causing time-dependent drain breakdown during OFF-state stress in devices with different  $L_{GD}$  and field plate lengths were determined, additional reliability tests have been performed to evaluate the impact of some structural and process parameters on the two degradation mechanisms. Only Device 1 and Device 2 are considered, since Devices 3 and 4 share the same failure mechanism of Device 2 but are less robust.

Fig. 12 reports the dependence of lifetime on the thickness of the GaN and AlGaIn layers in the case of Device 1 ( $L_{GD} = 3$   $\mu\text{m}$ ). Note that drain stress voltages higher than breakdown voltage, shown in Fig. 3, have been applied, since the considered devices, featuring thinner AlGaIn barrier and/or uid GaN layer are less prone to OFF-State degradation. In

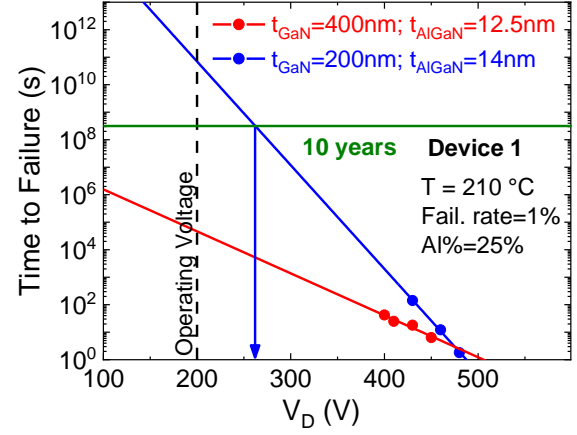


Fig. 12. Lifetime plot for Device 1 with different GaN channel and AlGaIn thicknesses. Failure criterion: 1% of failure at  $T = 210^\circ\text{C}$  extrapolated from a Weibull plot. The huge difference between the two devices is due to the thinner GaN channel. Note that, the extrapolated maximum  $V_D$  is, in any case, lower than Device 2 featuring same AlGaIn barrier (Process 2A in Fig. 14).

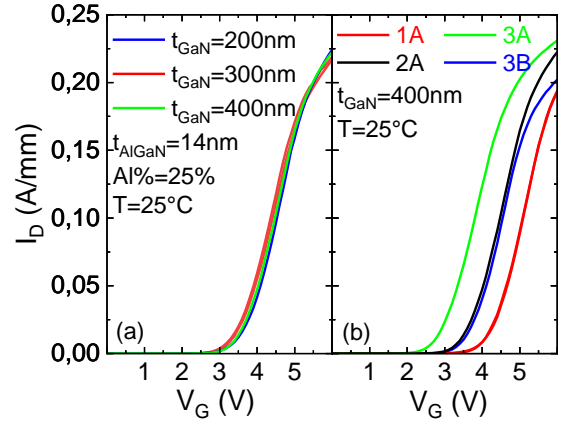


Fig. 13.  $I_D$ - $V_G$  characteristics for devices with different uid GaN thickness (a) and AlGaIn barrier configurations (b). Reference device 2A with  $t_{\text{AlGaIn}} = 14$  nm and Al content 25%. Then, moving from 1 to 3 means thicker AlGaIn, whereas from A to B lower aluminium content (Al%).

particular, the breakdown voltage for the Device 1 with  $t_{\text{GaN}} = 200$  nm ranges between 490 V and 510 V (not shown), for the reasons explained in section III.B. The lifetime plot allows to extrapolate the maximum operating drain voltage in OFF-state regime, considering a lifetime of 10 years at  $210^\circ\text{C}$  and a failure rate of 1% [38]. The TTF at 1% of failure for each drain bias condition has been extrapolated from Weibull plots with a shape parameter of  $\sim 1.3$ . As reported in section III.B, since the failure in Device 1 occurs in the GaN channel layer, an important improvement can be noticed by adopting a thinner GaN layer (blue), in spite of the thicker AlGaIn barrier which, as discussed in section III.B, degrades the reliability associated to failure 1.

In the case of devices with  $L_{GD} = 3$   $\mu\text{m}$ , the adoption of a 200 nm thick GaN channel layer guarantees 262V maximum applicable drain bias for a lifetime of 10 years at  $210^\circ\text{C}$ , which is higher than the maximum operating voltage (200 V at  $150^\circ\text{C}$ ). Importantly, we would like to emphasize that caution is advised in estimating the lifetime based on the stress measurements far beyond the normal operation conditions. However, the different devices' robustness caused by different degradation mechanisms is clearly observed from these plots.

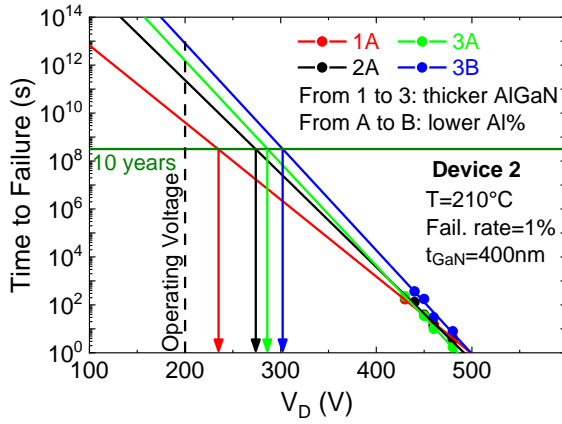


Fig. 14. Lifetime plot in the case of Device 2 with different AlGaIn barrier configurations. Reference device 2A with  $t_{\text{AlGaIn}} = 14$  nm and Al content 25%. Failure criterion: 1% of failure at  $T = 210^\circ\text{C}$  extrapolated from Weibull plot. A higher robustness is attained by adopting a thicker AlGaIn with a lower Al% (blue).

Moreover, as shown in Fig. 13 (a), the uid GaN layer thickness has no impact on the threshold voltage ( $V_{TH}$ ), trans-conductance ( $gm$ ) and on-resistance ( $R_{ON}$ ), therefore, it can be optimized without degrading the performance.

Fig. 14 shows the lifetime of Device 2 featuring a 400 nm thick uid GaN layer and different AlGaIn barrier configurations in terms of thickness and aluminium (Al) content. In particular, the reference device featuring  $t_{\text{AlGaIn}} = 14$  nm and Al% = 25 % is indicated as 2A. In the adopted coding system, the numerical index, ranges from 1 to 3 for progressively thicker AlGaIn; the letter index A corresponds to higher aluminium content (Al%) than B. Unlike Device 1, the long-term reliability, limited by the time-dependent OFF-State breakdown, is improved by adopting a thicker AlGaIn barrier layer and a lower Al%, further confirming the occurrence of failure 2 between the 2DEG close to drain and source field plates. An important conclusion here is that the AlGaIn barrier plays an important role and, in general, each layer between the source field plates and the channel is important. In particular, a thicker AlGaIn implies a higher number of defects that must be created to form a percolation path, whereas a lower Al content reduces the mechanical stress in the AlGaIn barrier due to a lower lattice constant mismatch with the GaN channel layer, possibly reducing the creation of structural defects [20, 38].

However, unlike the uid GaN layer thickness, the AlGaIn barrier plays, as expected, an important role on the ON-state characteristics (see Fig. 13 (b)), therefore, it must be optimized accordingly, as is the case for gate-stack reliability [40].

#### IV. CONCLUSION

In this paper, the time-dependent OFF-State breakdown of GaN-based power HEMTs with p-type gate has been investigated by means of OFF-State leakage tests, HTRB stress and TCAD simulations, for devices featuring different structural and process variations.

Thanks to this approach, the different locations of failure, depending on the gate-to-drain distance and respective field plate configurations, have been identified. For  $L_{GD}$  shorter than  $3\ \mu\text{m}$ , the time-dependent breakdown occurs in the uid GaN channel layer between drain and source, whereas if  $L_{GD} \geq 4\ \mu\text{m}$ ,

a surface breakdown occurring between the 2DEG and source field plates is observed.

In the first case, the TTF is strongly dependent on the drain leakage current level, which is related to the depletion of the uid GaN channel layer in the access region and at the drain-side edge of the gate. Because of the relatively short  $L_{GD}$  and consequently, of the field plate lengths, a thin GaN layer is needed to facilitate such depletion, eventually reducing the drain leakage current and improving the TTF.

Concerning the surface breakdown between 2DEG and source field plates, results have shown that  $L_{GD}$  and uid GaN layer thickness have not a clear effect on the long-term time-dependent breakdown under OFF-State stress. Of paramount importance is the geometry configuration of the field plates for given gate-to-drain distance. Their length should be optimized to reduce the area exposed to high electric fields, hence providing longer TTF during OFF-state stress. However, such optimization must not significantly alter, as shown in Fig. 11, the electric field distribution beneath the field plates in order to ensure a good trade-off between time-to-breakdown, static breakdown voltage and possible current collapse. Moreover, the optimization of the layers between the field plates and the GaN channel, i.e. dielectric layer and AlGaIn barrier, can further improve the device robustness. In particular, this study has revealed that a thicker AlGaIn barrier with lower aluminium content gives rise to longer time-to-breakdown when surface breakdown dominates.

In conclusion, the characterization of such different degradation mechanisms with their structural and process dependencies helps to steer further device optimization in terms of on-resistance, static breakdown voltage and long-term time-dependent drain breakdown.

#### ACKNOWLEDGMENT

M. Millesimo would like to thank Prof. Claudio Fiegna, Full Professor at University of Bologna, for spending his valuable time for reading the manuscript and providing valuable suggestions.

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