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This is the final peer-reviewed author's accepted manuscript (postprint) of the following publication:

Published Version:

Mandrioli R., Ricco M., Hammami M., Viatkin A., Grandi G. (2021). A Ripple-Free Output Current Interleaved DC/DC Converter Design Algorithm for EV Charging. Institute of Electrical and Electronics Engineers Inc. [10.1109/ICIT46573.2021.9453554].

Availability:

This version is available at: <https://hdl.handle.net/11585/830164> since: 2024-02-29

Published:

DOI: <http://doi.org/10.1109/ICIT46573.2021.9453554>

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A Ripple-Free Output Current Interleaved DC/DC Converter Design Algorithm for EV Charging

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Abstract—In this paper, a ripple-free output current interleaved DC/DC converter has been analyzed for Electric vehicle charging stations. Firstly, a ripple-free control strategy able to ensure a theoretically flat output current profile and input voltage ripple minimization at any working conditions is discussed. This strategy drives the active front-end to regulate the DC-link voltage and, at the same time, the interleaved back-end converter to operate in zero ripple working points. Secondly, a generalized designing algorithm able to consider constraints like AC grid voltage and battery voltage is proposed. Finally, simulations support ripple mitigation capabilities in steady-state and transient conditions for a 12-leg scheme.

Keywords—interleaved converter, electric vehicle, battery charger, ripple minimization, optimization

I. INTRODUCTION

Electric Vehicles (EVs) are expected to be one of the leading players in the future green shift [1]. Year by year, many more producers are presenting new EV models. Meanwhile, governments are drawing up multiple policies toward more favorable market conditions and charging facilities wide deploy. The diffusion and the power rating of charging facilities are experiencing exponential growth. To face customers' "range anxiety" and provide a driving experience close to the one daily experienced with internal combustion engine vehicles, the introduction of a reliable and well-distributed back-bone fast-charging network is the priority [2]. To be defined as a fast charger, the converters should guarantee hundreds of kilometers in about 20/30 minutes [3]. From a regulatory point of view, fast charging is considered a level 3 mode 4 charging where the voltage is below 1kV. The power is at least 50kW provided through a hardwired structure permanently dedicated to the EV charging service [4], [5]. Typical output voltages range in the diapason 200-800V, and the power involved in each charging port can reach hundreds of kilowatts. Indeed, standardized plugs and sockets like Combo 1, Combo 2, and CHAdeMO can withstand charging power of about 400kW [6].

Among the multiple classical solutions presented in the literature [7]–[11], manufacturers are concentrating mainly on proposing modular solutions able to be rapidly deployed and a posteriori scaled. In this way, it is possible to follow the future market trend ensuring, at the same time, sufficient geographical coverage [12]. Moreover, modular solutions can take advantage of the cost reduction guaranteed by standardized modules' mass production. Interleaved topologies are recognized to be particularly beneficial for increasing power ratings without introducing complications and cost sources by directly coupling parallelized modules through inductors.

The interleaved structure can be successfully employed in both as AC/DC [13], [14] and as DC/DC [10], [15], [16]. For this reason, in [17]–[19], the interleaved arrangement has been considered for both power stages of the EV charger. The efficiency computation and comparison for different switching technologies in interleaved DC/DC has been carried out in [15]. Authors in [16] have analyzed the possibility of minimizing output current ripple and increasing overall efficiency employing the phase-shedding technique. Similarly, a proper control strategy has been treated in the input voltage ripple analysis and minimization [19]. This control strategy has been originally introduced in [17], [18], under the name of "ripple-free". It proposed a strategy that jointly controls both AC/DC and DC/DC stages to ensure a complete cancellation of the output current ripple in all working conditions. However, no mention of the converter design has been made, reducing the strategy's generality grade.

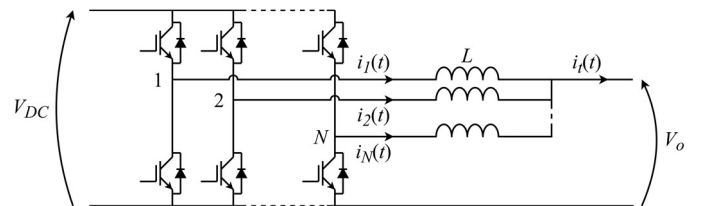


Fig. 1. N-leg interleaved buck converter.

Firstly, the ripple-free strategy has been recalled and generalized. Secondly, a ripple-free N-leg converter designing algorithm for EV charging purposes is proposed. It considers multiple constraints like minimum DC-link voltage and EV battery voltage range for providing a customized power converter and the relative control strategy after a few simple steps. Finally, a discussion of simulation results highlights the strengths and limitations of the proposed algorithm.

II. IBC INHERENT RIPPLE MINIMIZATION

As visible in Fig. 1, the Interleaved Buck Converter (IBC) is made of N parallelized legs coupled through a set of inductors L . It is known that IBC, if adequately driven, can provide an inherent output ripple minimization [15]–[19]. This effect is also reflected in an input voltage ripple minimization [19]. Interleaved carrier based PWM is one of the most common modulation principles for DC/DC high power converters. It takes advantage of N carriers evenly shifted for obtaining a destructive current ripple summation in the total output. Similarly, benefits are introduced on the input side in terms of voltage ripple minimization thanks to a destructive DC-link current pulses summation [19]. In this section, the inherent ripple minimization capability is recalled.

The current $i_k(t)$ of the k^{th} leg can be divided into two contributions, $I_k(t)$, and $\Delta i_k(t)$ as in (1). The average component $I_k(t)$ (averaged over the switching period T_{sw}) represents the total current's active part. Switching operations are the cause of the superimposed current ripple $\Delta i_k(t)$.

$$i_k(t) = I_k(t) + \Delta i_k(t) \quad (1)$$

Similarly, it is possible to describe the total output current $i_t(t)$ by employing average and ripple components, respectively $I_t(t)$, and $\Delta i_t(t)$ as in (2).

$$i_t(t) = I_t(t) + \Delta i_t(t) = \sum_{k=1}^N i_k(t) \quad (2)$$

$$\begin{cases} I_t(t) = \sum_{k=1}^N I_k(t) \\ \Delta i_t(t) = \sum_{k=1}^N \Delta i_k(t) \end{cases}$$

In the case of PWM control, it is known that the peak-to-peak leg current ripple $\Delta i_{kpp}(t)$ can be found utilizing:

$$\Delta i_{kpp} = \frac{V_{DC}}{L f_{sw}} (1 - \delta) \delta \quad (3)$$

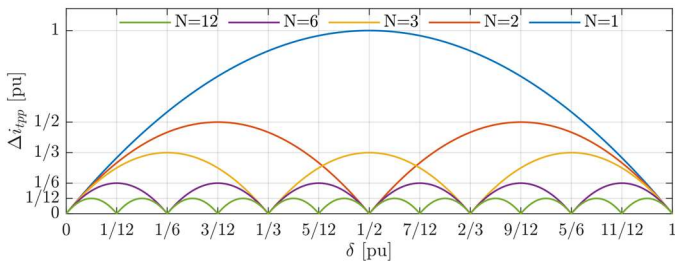


Fig. 2. Inherent ripple reduction, output current ripple peak-to-peak as a function of δ for a different number of legs N .

whereas V_{DC} , L , f_{sw} , and δ are respectively DC-link voltage, leg inductance, switching frequency, and duty-cycle.

If each leg of the interleaved converter is fired by evenly shifting the carriers, it is possible to achieve an inherent ripple reduction effect on the total output current. From [17]–[19], it is possible to write the total output current ripple peak-to-peak $\Delta i_{tpp}(t)$ at any operative condition as:

$$\Delta i_{tpp} = \frac{V_{DC}}{L f_{sw}} \left[1 - N \left(\delta - \frac{p-1}{N} \right) \right] \left(\delta - \frac{p-1}{N} \right) \quad (4)$$

where p is a natural index ranging from 0 to N computed as:

$$p = \text{ceil}(N\delta) \quad (5)$$

Fig. 2 depicts $\Delta i_{tpp}(t)$ some noticeable cases normalized considering the maximum for $N=1$ as a base. The interleaving provides, in the worst case, a current ripple reduction of about N times. As visible (4) has the following $N+1$ roots:

$$\delta = \frac{p}{N} \quad (6)$$

Therefore, there are N suitable working points ($p \neq 0$) able to provide a not null output voltage V_o and contemporary capable of nullifying the output current ripple $\Delta i_t(t)$. As explained before, this ripple reduction is entirely due to the interleaved topology and the carriers shifting.

Similarly, it is possible to demonstrate inherent ripple mitigation in the input voltage as well. As pointed out in [19], the input voltage ripple peak-to-peak $\Delta v_{DCpp}(t)$ at any operative condition is:

$$\Delta v_{DCpp} = \frac{I_t}{N C f_{sw}} \left[1 - N \left(\delta - \frac{p-1}{N} \right) \right] \left(\delta - \frac{p-1}{N} \right) \quad (7)$$

where C is the DC-link capacitor.

III. RIPPLE-FREE STRATEGY FOR AN N-LEG IBC

The operative conditions introduced in (6) could theoretically ensure null ripple regardless of the switching frequency f_{sw} and inductance L . An original control strategy able to guarantee ripple-free at any working point has been introduced in [17] and subsequently improved in [18], [19]. It effectively tunes the DC-link voltage V_{DC} to eliminate the output current ripple in an IBC with nine legs. In this section, the ripple-free control strategy is generalized, taking into account some design constraints not considered in the literature yet.

As known, the IBC output voltage V_o can be calculated as:

$$V_o = \delta V_{DC} \quad (8)$$

By introducing the N suitable roots computed in (6), inside (8), it is possible to find suitable V_{DC} able to guarantee ripple-free operations as:

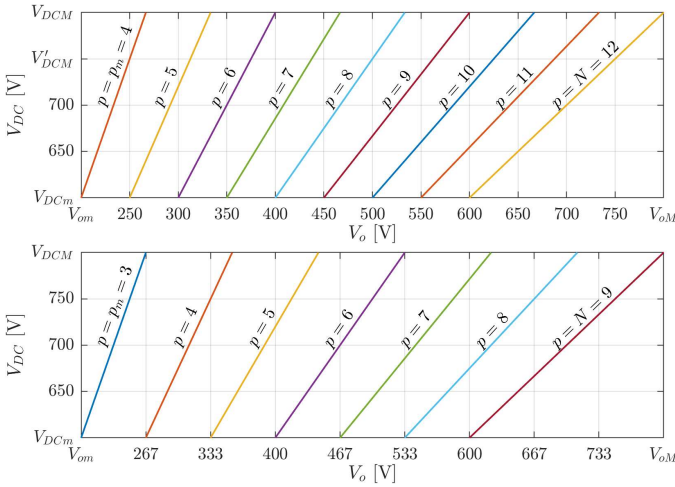


Fig. 3. Set of ripple-free working points on a $V_{DC} - V_o$ framework for $N = 12$ (top), and $N = 9$ (bottom) assuming $V_{DCm} = 600\text{V}$, $V_{om} = 200\text{V}$, and $V_{oM} = 800\text{V}$.

$$V_{DC} = \frac{N}{p} V_o \quad (9)$$

Fig. 3 shows the set of suitable ripple-free working points introduced in (9) on an arbitrary $V_{DC} - V_o$ framework for $N = 12$ and $N = 9$.

However, the DC-link range might be limited by previous rectifier stage capability. In most cases, the minimum DC-link voltage V_{DCm} generable depends on the AC/DC topology, PWM scheme, and the AC grid voltage. For those reasons, V_{DCm} should be considered as a given design constraint. Similarly, the range of output voltage levels V_o depends on the EV battery voltage, which usually falls within the range of 200-800V. For the generalization introduced here, minimum and maximum output voltages are respectively displayed as V_{om} and V_{oM} .

Once V_{DCm} and V_{om} have been defined, it is possible to compute the minimum number of legs N_m necessary for operating in ripple-free conditions as:

$$N_m = \text{ceil}\left(\frac{V_{DCm}}{V_{om}}\right) \quad (10)$$

Replacing V_{DCm} and V_{om} in (9), and by considering $N \geq N_m$, one could find the minimum index p_m and the minimum duty-cycle δ_m as:

$$p_m = \text{floor}\left(N \frac{V_{om}}{V_{DCm}}\right) \rightarrow \delta_m = \frac{p_m}{N} \quad (11)$$

It can be easily seen that as higher the number of available legs N is, as more ductile the IBC is because it can produce lower output voltage levels without having a particularly low minimum DC-link voltage V_{DCm} . Moreover, by employing a higher number of legs ($N > N_m$), there is a certain redundancy able to guarantee ripple-free working conditions even with one or multiple legs out of service (although a power downgrade is unavoidable).

Since V_{DCm} should be considered as a given parameter, the maximum DC-link voltage value defines the magnitude of the DC-link range of voltage variation ΔV_{DC} necessary for operating in ripple-free conditions. As visible in Fig. 3, maximum DC-link voltage can be either defined by looking at V_{oM} magnitude (displayed as V_{DCM}) or by the necessity of having a continuous V_o span from V_{om} to V_{oM} (marked with ' symbol). The output voltage continuity must be guaranteed for low V_o voltage values (when working point slopes of Fig. 3 are steeper) when the transition from p_m to p_m+1 takes place. The output voltage continuity condition might be described as:

$$V'_{DCM} \delta_m \geq V_{DCm} \left(\delta_m + \frac{1}{N} \right) \quad (12)$$

rewriting (12):

$$\begin{cases} V'_{DCM} \geq V_{DCm} \left(1 + \frac{1}{N \delta_m} \right) = V_{DCm} \left(1 + \frac{1}{p_m} \right) \\ \Delta V_{DC} = V'_{DCM} - V_{DCm} \geq \frac{V_{DCm}}{N \delta_m} = \frac{V_{DCm}}{p_m} \end{cases} \quad (13)$$

It is possible to notice that as higher the leg number N and the minimum output voltage level V_{om} are, the lower V_{DCM} and ΔV_{DC} are. However, the maximum DC-link voltage might require to be higher than the one computed in (13), when happens that $V_{oM} > V_{DCm}$ ($\delta=1$), and therefore equation (14) should be employed for high output voltage values.

$$V_{DCM} \geq V_{oM} \quad (14)$$

The ripple-free strategy has the task of selecting a proper couple of values δ (or p) and V_{DC} able to provide a suitable working point regardless of the output voltage reference. As visible in Fig. 3, output voltage reference values could be generated utilizing multiple δ and V_{DC} couples. This notion is equivalent to saying that (9) is not an injective function since when V_{DC} is free to float, numerous solutions can be found. A further designing criterion called "leg current ripple minimization" should be therefore introduced. This additional criterion aims to select the working point that guarantees the minimum current ripple in each leg at any working point.

Equations (15) can be obtained by replacing (8) into (3). A graphical representation is available in Fig. 4 for $N = 12$ (top) and $N = 9$ (bottom).

$$\Delta i_{kpp}(t) = \frac{1}{2} \frac{V_o}{L f_{sw}} (1 - \delta) = \frac{1}{2} \frac{V_o}{L f_{sw}} \left(1 - \frac{V_o}{V_{DC}} \right) \quad (15)$$

Equation (15) states that for a given value of V_o , having a lower DC-link voltage V_{DC} or a greater δ (or p) produces a lower-leg current ripple. Even though output current ripple $\Delta i_i(t)$ is called off (when working inside (6)), the current ripple in each leg $\Delta i_k(t)$ does not take advantage by itself of the interleaved connection. Having introduced the ripple-free strategy might also improve the leg current ripple, rather than only on the output current ripple as it would have been with the sole interleaved topology. Equations (16) and (17) summarize in steady-state the

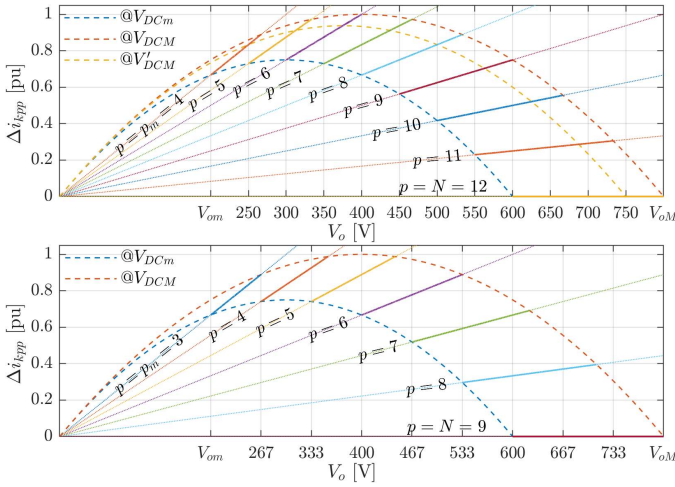


Fig. 4. Leg current ripple peak-to-peak in ripple-free condition normalized for Δi_{kpp} global maximum for $N = 12$ (top), and $N = 9$ (bottom).

ripple-free strategy able to consider all the previously stated considerations for a generic N-leg IBC. The AC/DC front-end regulates the DC-link voltage to the reference value indicated with * in (16). On the other hand, the interleaved DC/DC is driven employing (17). A visual representation of the ripple-free control strategy is presented in Fig. 5 and Fig. 6.

$$\begin{cases} V_{DC}^* = V_o^* \frac{N}{\text{floor}\left(\frac{NV_o^*}{V_{DCM}}\right)} & V_o^* \leq V_{DCM} \\ V_{DC}^* = V_o^* & V_o^* > V_{DCM} \end{cases} \quad (16)$$

$$\delta = \frac{V_o^*}{V_{DC}^*} \quad (17)$$

As displayed in Fig. 5, working points (in red) always stand on the ripple-free trajectories, and at the same time, tend to use the lowest V_{DC} available. Moreover, as more V_o approaches V_{DCM} , as smaller the dc-link voltage span needs to be.

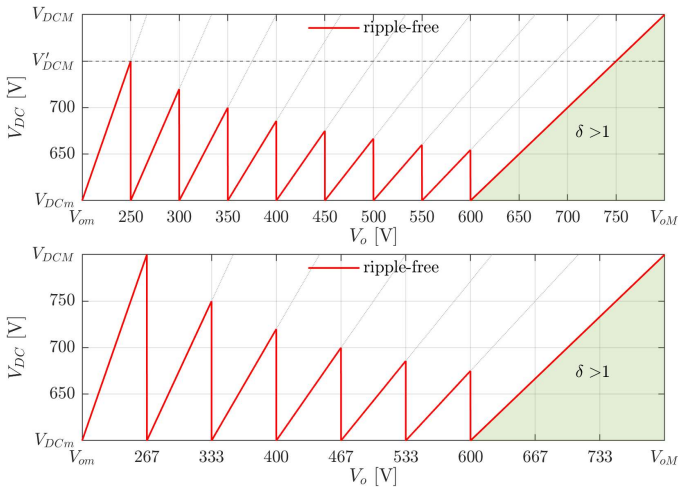


Fig. 5. Set of steady-state ripple-free working points in ripple-free conditions, for $N=12$ (top), and $N=9$ (bottom).

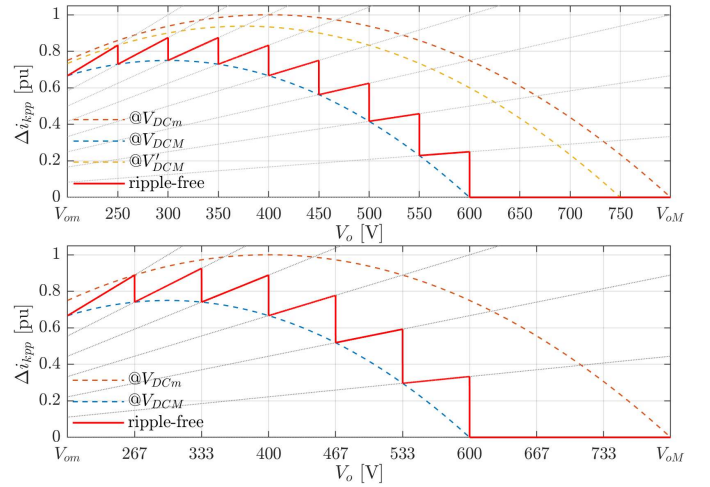


Fig. 6. Leg peak-to-peak current ripple in ripple-free conditions, normalized for Δi_{kpp} global maximum ($@V_{DCM}$) (b) for $N = 12$ (top), and $N = 9$ (bottom).

When V_o becomes higher than V_{DCM} , the IBC enters the $\delta = 1$ zone forcing the dc-link voltage to range up to V_{oM} . On the other hand, Fig. 6 depicts the "Leg current ripple minimization" criterion. It can be readily seen that the trajectory (in red) always ensures the lowest leg current ripple. It worth noticing that, although in $\delta = 1$ zone V_{DC} assumes high values, the leg current ripple is always kept equal to zero.

However, to obtain the behavior visible in Fig. 5 and Fig. 6, the DC-link should be able to change its voltage level sharply without any delay. The actual action requires introducing a not null DC-link transient time in which $V_{DC} \neq V_{DC}^*$ and, therefore, δ briefly falls outside the ripple-free conditions ((5) is no longer respected). As suggested in [18], relation (17) should be replaced with (18), introducing the actual DC-link voltage value.

$$\delta = \frac{V_o^*}{V_{DC}} \quad (18)$$

IV. DESIGN ALGORITHM

The relations of the previous section might be summarized as a coherent design algorithm. The initial constraints to be determined are minimum DC-link voltage V_{DCm} , and minimum and maximum output voltage (V_{om} and V_{oM}). The following step is to determine through (10) the minimum number of legs N_m necessary for obtaining ripple-free conditions. Considering reliability, redundancy, and desired power-sharing, the actual number of interleaved legs N is chosen ($N \geq N_m$). By applying in cascade (11), (13), and (14), maximum DC-link voltages are obtained. Converter components should be chosen accordingly to the maximum value among the two. This procedure is visualized in Fig. 7. Once the converter framework in terms of output voltage range (V_{om} and V_{oM}), DC-link voltage range (V_{DCm} , and V_{DCM}), and the number of legs N have been defined, it is possible to introduce the actual ripple-free strategy of (16) and (18).

Table I. and Table II. some computations are reported for cases having V_o ranging from 200V to 800V considering a variegate number of legs N . The maximum voltage and voltage range of the DC-link for a given legs number are reported in bold. In particular, Table I. shows the typical case in which a

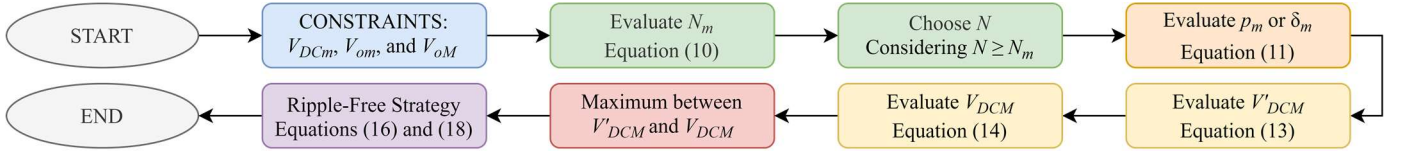


Fig. 7. Ripple-free IBC designing algorithm.

two-level active front-end is connected to a line-to-line voltage of 400V. As visible, employing more than 9 legs will not provide any benefits in the DC-link voltage range for the considered framework. On the other hand, Table II reports calculations referring to the same active rectifier as before but connected to a grid experiencing a line-to-line voltage of 240V. In this case, $V_{DCM} = V_{oM}$, and therefore, unless current sharing is desired, selecting $N = N_m$ is the optimal solution. It should be noted that previous formulations have general validity and can be employed straight once V_{DCm} has been determined regardless of what is the AC/DC stage and the grid voltage considered.

N	p_m	δ_m	V'_{DCM}	V_{DCM}	ΔV_{DC}	$V_{DCM} - V_{DCm}$
$N_m = 3$	1	0.33	1200V	800V	600V	200V
6	2	0.33	900V	800V	300V	200V
9	3	0.33	800V	800V	200V	200V
12	4	0.33	750V	800V	150V	200V
15	5	0.33	720V	800V	120V	200V
18	6	0.33	700V	800V	100V	200V

¹ Constraints: $V_o = 200\text{-}800\text{V}$ and $V_{DCm} = 600\text{V}$.

N	p_m	δ_m	V'_{DCM}	V_{DCM}	ΔV_{DC}	$V_{DCM} - V_{DCm}$
$N_m = 2$	1	0.50	600V	800V	300V	500V
4	2	0.50	450V	800V	150V	500V
8	5	0.63	360V	800V	60V	500V
10	6	0.60	350V	800V	50V	500V
12	8	0.66	338V	800V	38V	500V
14	9	0.64	333V	800V	33V	500V

² Constraints: $V_o = 200\text{-}800\text{V}$ and $V_{DCm} = 300\text{V}$.

Real scenario applications might introduce further considerations that can play a relevant role in design decisions. For instance, if a strong power density is desired, one possibility is to employ cheap and not bulky surface mounting devices (SMDs) by selecting a leg number N well above the minimum value N_m given by the design algorithm. Although, as explained above, a high number of legs might not provide strong benefits in terms of DC-link voltage span reduction, it might open to the phase shedding technique proposed in [16]. Indeed, it is possible to mitigate losses due to devices' non-idealities and parasitic components by reducing the number of active legs when the full current rating is not necessary.

V. SIMULATION RESULTS

The ripple-free strategy has been validated with experimental and simulation results in [17]–[19]. No mention of the detrimental effects introduced by the DC-link transient is available yet. To represent appreciably the not null output current ripple that is experienced when $V_{DC} \neq V_{DC}^*$, the following two cases are depicted: output voltage staircase and output

voltage ramp. Moreover, for the sake of enhancing visualization quality, the current ripple effects on the output voltage are extremized by employing a purely resistive load (5Ω). Finally, the simulation duration (seconds) is much shorter than an actual charging process (minutes), increasing each transient's relevance. It should be mentioned that a real battery charger works with much more favorable conditions, and therefore detrimental effects here depicted are barely noticeable.

In Fig. 8, $V_{dc}(t)$ (light blue) has a continuous variation that brings the converter outside ripple-free conditions during transients. However, as reflected on the output current $i_t(t)$, (orange), the output voltage tracking is always ensured (ripple apart). However, when the staircase voltage is in the $\delta = 1$

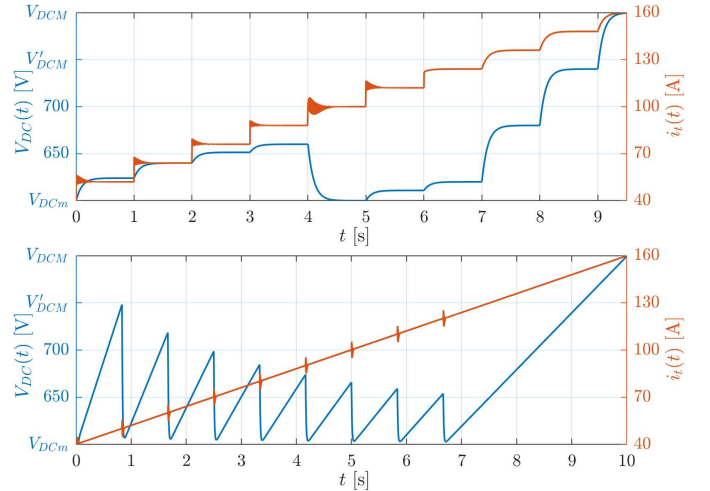


Fig. 8. Output current i_t and V_{DC} time evolution for a V_o staircase (top) and a V_o ramp (bottom). For a 12 legs IBC with a 5Ω resistive load.

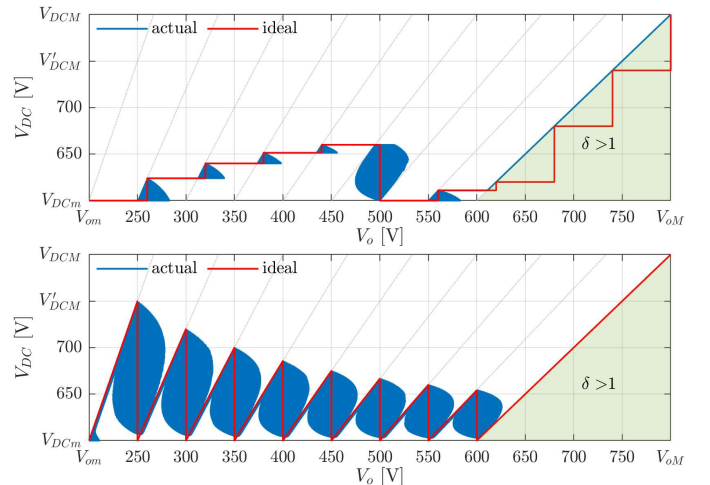


Fig. 9. Ideal and actual V_o tracking for a voltage staircase (top) and ramp (bottom). For a 12 legs IBC with a 5Ω resistive load.

working condition (if present), the tracking is lost because the converter cannot work at $\delta > 1$. This phenomenon is negligible in the voltage ramp case (similar to an actual charging operation). In any case, as soon as the DC link transient is ended, the perfect tracking and the ripple-free output is always guaranteed.

What is described in the previous paragraph is well visible in the V_{dc} - V_o framework depicted in Fig. 9. As visible, when the strategy must jump from one p to the other, the actual profile (blue) stops following the ideal profile (red), and the ripple lobes appear. Again, this is due to the DC-link that cannot change its voltage sharply as in the ideal conditions. Finally, when an output voltage ramp is employed as a reference, the strategy does not select working points in the overmodulation area (depicted in green).

In a more realistic condition, Fig. 8 would display a much sharper current $i_i(t)$ profile. Moreover, output voltage ripple lobes visible in Fig. 9 would present a smaller dimension to follow the ideal profile strictly.

VI. CONCLUSION

A generalized ripple-free control technique for EV charging purposes is provided here. It effectively drives both active front-end AC/DC and back-end interleaved DC/DC to ensure the output voltage reference tracking and an output current profile free from ripple at any working conditions. It can handle any working conditions and tolerates transient. A complete and coherent design algorithm able to consider design constraints has been proposed and employed for some reference cases. Moreover, multiple considerations about the leg current ripple and the output current ripple have been provided, trying to optimize internal converter parameters. Additionally, real scenario applications discussion is provided based on devices' power density and non-idealities. Finally, numerical simulations able to support and discuss the mentioned above statements have been introduced.

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