Ka-band 4 W GaN/Si MMIC power amplifier for CW radar applications

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***Abstract* — In this contribution it is reported the design, implementation and characterization of a 4-stage single-ended Ka-band power amplifier based on 100 nm GaN/Si commercial process. The amplifier, designed for CW radar applications, has been measured under small-signal and pulsed large-signal conditions. The amplifier exhibits an output power above 4 W, together with power added efficiency in excess of 28 % and operative gain larger than 25 dB over the 34 GHz – 38 GHz frequency range.**

***Keywords* — Gallium nitride, MMICs, Power amplifiers, Millimiter wave.**

I. Introduction

Ka-band (26.5 GHz – 40 GHz) is becoming the reference frequency range for a large number of applications, including 5G, satellite communication systems and high-resolution radar detection and imaging. Although traveling wave tube amplifiers (TWTAs) remain the standard in this frequency band, especially for space applications, the adoption of solid state power amplifiers (SS-PAs) based on GaN is becoming increasingly appealing, thanks to a reduced footprint and hence lighter, less complex equipments. Despite this, both at commercial and research level, the availability of GaN MMICs at Ka-band is still limited, especially above 30 GHz where 150 nm (or higher) gate-length technologies are really close to their limit and shorter gate lengths are required (see Table 1).

This work reports a 4 W PA designed to operate at the upper limit of Ka-band, based on the commercial 0.1 μm GaN/Si process from OMMIC, designed for high-resolution CW radar applications. The measured performance of the PA is in line with the state-the-art at this frequency, achieving a remarkably good output power density for a GaN/Si process compared to GaN/SiC.

II. Technology

For the development of the MMIC power amplifier, the technology adopted was the D01GH 100 nm GaN/Si HEMT process, released by OMMIC [7]. It is characterized by a cutoff frequency of 130 GHz, with a maximum stable gain of 13 dB at 30 GHz. The power density is about 3.3 W/mm for a biasing voltage of 12 V, with a maximum breakdown voltage of 40 V. The active device periphery can be arbitrarily scaled up to 8 fingers and 150 μm unit gate width. For Ka-band operation, it is recommended by the foundry to limit the maximum periphery to 400 μm to avoid gain degradation. Thus, the selected device for the final stage was a 8x50 μm HEMT.

Table 1. Ka-band MMIC PA state-of-the-art and comparison with the present work (P.W.). Peak output power, small-signal gain, power added efficiency and output power density values are reported.

Ref.	Technol.	Freq. GHz	P_{out} dBm	Gain (SS), dB	PAE %	P_{out} d. W/mm
[1]	0.15 GaN/SiC	28 – 31	39	29	30	2.5
[2]	0.25 GaN	32 – 38	38	33	NA	2
[3]	0.18 GaN/SiC	29 – 31	43	8	15	3.1
[4]	0.15 GaN/SiC	25 – 30	39	23.5	26.5	2.5
[5]	0.15 GaN/SiC	32 – 38	40	25	36	3.1
[6]	0.1 GaN/Si	28 – 34	39	25	30	2
[7]	0.1 GaN/Si	38 – 40	40	20	30	2.4
[8]	0.2 GaN/SiC	30 – 34	39.1	23	42	4.4
[9]	0.1 GaN/SiC	26 – 35	39.6	22	25	2.4
P.W.	**0.1 GaN/Si**	**34 – 38**	**36.4**	**30**	**29.5**	**2.7**

A peculiar characteristic of the selected process is the adoption of a Silicon (Si) substrate, instead of the more widely adopted Silicon Carbide (Sic) one (see also Table 1). On one hand, Si implies reduced costs of wafer fabrication, on the other hand, its lower thermal conductivity [10] limits the maximum power dissipation of each device, and thus decreases the effective power density that can be delivered by the active devices [11].

III. Amplifier Design

The amplifier was designed to cover the frequency range from 35 GHz to 40 GHz, providing an output power of 4 W (36 dBm) with a power gain larger than 20 dB, operating in continuous wave (CW) mode. A multi-stage combined PA architecture was selected for the MMIC. Concerning the thermal aspects, a maximum MMIC backside temperature of $T_{BS} = 50\,^{\circ}\mathrm{C}$ was assumed, at which the maximum channel temperature T_J in the active devices should be kept 200 °C, which is the maximum safe limit for terrestrial applications according to the foundry directives.

A 20 % class-AB bias point was selected, as a compromise between achievable gain and dissipated power,

corresponding to roughly I_{DQ} = 250 mA/mm (gate supply voltage V_{GG} = -1.25 V), while the drain supply voltage was set to V_{DD} = 12 V. The first design step was the identification of the optimum PA architecture, i.e. the most suitable number of active stages and device per stage to achieve the target specifications. To this aim, the performance attainable with different devices was analyzed, through extensive load-pull simulations. In order to respect the temperature constraints, the maximum dissipated power limit was taken into account and the optimum load was selected as a trade-off between output power, efficiency, gain and maximum dissipated power, as shown in Fig. 1. Here are reported the output power (blue), efficiency (red) gain (green) load-pull contours at center frequency (37.5 GHz) and at 1 dB of gain compression, for the 8x50 μm device selected for the final stage, along with the maximum allowed dissipated power contour (grey, dashed), which establishes the boundary of the usable loads' area. Given a device thermal resistance of roughly 36.3 °C/Wmm (value that was inferred from the foundry design manual), a maximum power dissipation of 4.1 W/mm was considered in all the simulations. For example, considering the 8x50 μm device, this leads to a maximum dissipated power of 1.65 W and thus to an optimum load $\Gamma_{opt} = 0.73e^{j158^\circ}$, represented by the cross symbol in Fig. 1.

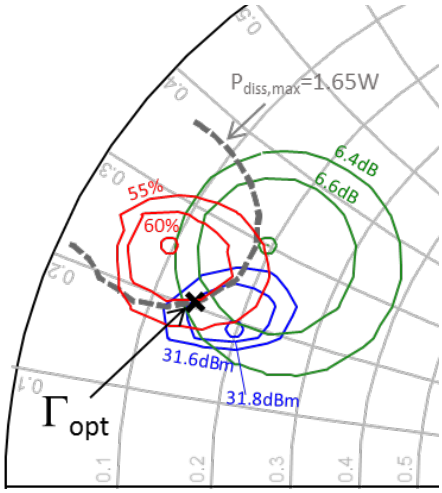

Fig. 1. Load-pull contours at 37.5 GHz for the 8x50 μm device, used in the final stage. Optimum load gives the best trade-off between output power and gain, while keeping the dissipated power within its maximum limit.

Given a device output power of 31.8 dBm, and accounting for the losses of the output power combiner in the Si substrate (roughly 1 dB), to attain the targeted output power level 4 parallel 8x50 μm devices were adopted in the final stage, for a total periphery of 1.6 mm. In order to avoid thermal coupling among the transistors of the final stage, separate via holes were used in each device. In this way, the maximum dissipated power of each transistor is not affected by the neighbours ones.

The compressed gain obtained for the final stage is around 6 dB. Therefore, in order to assure the target overall gain, a 4-stage topology was employed. In particular, to provide the necessary driving power to the final stage, two 8x50 μm devices were used for the third (driver) stage. For these devices the same optimum load already adopted for the final stage was synthesized. These devices operate in mild compression with an associated gain around 6 dB.

Analogously, a single 8x50 μm device was selected for the second (pre-driver) stage. On the same load, this operates in linear regime providing a gain higher than 7 dB. Finally, a single 4x50 μm device was used as an additional linear stage to boost the total gain of 9 dB. A picture of the realized MMIC PA is shown in Fig 2. The chip size is $5.0 \times 2.2\,\text{mm}^2$.

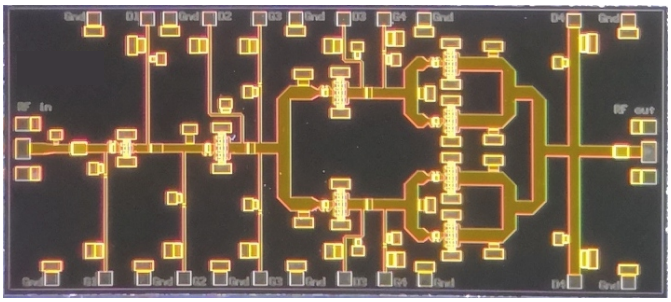

Fig. 2. Microscope picture of the MMIC PA. Chip size is 5x2.2 mm^2.

All the adopted devices are inherently stable in the design frequency band. To assure wide-band unconditional stability, an RC stabilization network was added in series with the gate of each device (see stability factor reported in Fig. 3). Odd-mode stability analysis was also checked following the Ohtomo approach [12].

In Ka-band, EM coupling cannot be neglected, thus all the MMIC passive networks were optimized through EM simulations, performed with Keysight Momentum. The small-signal simulated S-parameters of the MMIC are reported in Fig. 3: a small-signal gain larger than 22 dB is expected, together with input and output return loss better than 10 dB. The sharp variations that can be observed at some frequency points are due to the relatively coarse frequency sampling adopted in the EM simulations outside the target bandwidth.

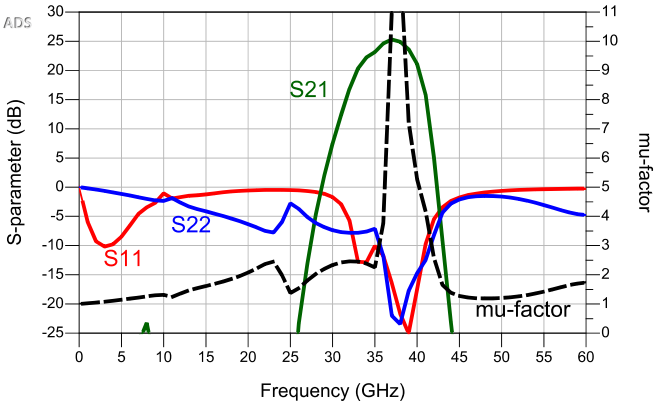

Fig. 3. Small-signal simulation results at the nominal bias point (V_{DD} = 12 V, V_{GG} = -1.25 V).

Fig. 4 reports the large-signal simulation results (output power and PAE) at center frequency. A saturated output power

of 36 dBm was obtained, with a power added efficiency close to 25 %. In the same figure, the estimated channel temperature of each device is also reported. The latter is computed from the simulated dissipated power (P_{diss}), adopting the nominal thermal resistance (R_{TH}) of the devices provided by the foundry as

$$T = T_{BS} + P_{diss} R_{TH} \quad (1)$$

With T_{BS}=50°C, all devices show a channel temperature below 200 °C.

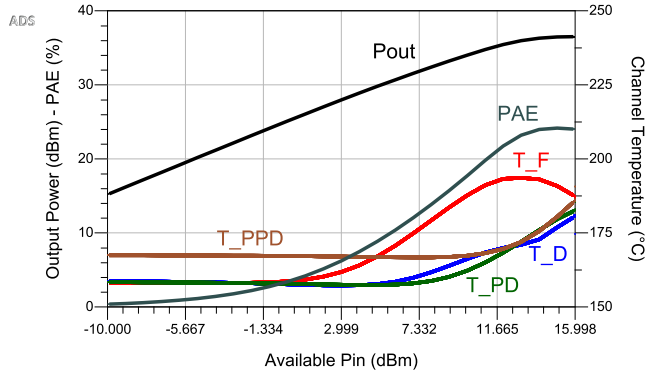

Fig. 4. Simulated large-signal performance at 37.5 GHz. F=Final, D=Driver, PD=Pre-Driver, PPD=Pre-Pre-Driver.

IV. Measurement Results

The designed PA was mounted on a prototype test-jig, shown in Fig. 5, and characterized in both small- and pulsed large-signal conditions. The quiescent drain and gate bias voltages of all stages were set to their nominal values, i.e. V_{DD} = 12 V, V_{GG} = -1.25 V, corresponding, as expected, to a quiescent drain current on each device of roughly 250 mA/mm.

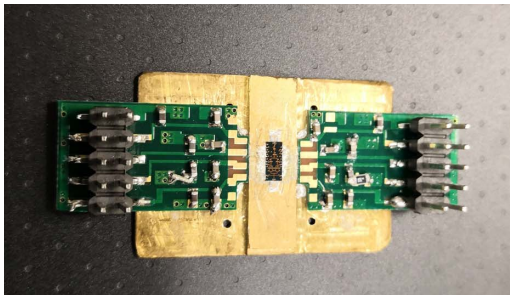

Fig. 5. Picture of the MMIC mounted on the prototype test-jig.

The small-signal performance is reported in Fig. 6, compared with simulation results. A small-signal gain higher than 20 dB is achieved in the entire bandwidth (peak value of 30 dB at 36 GHz), while the input and output return loss is better than -5 dB in the 34 GHz to 38 GHz frequency range. A 5 % frequency shift with respect to simulation prediction is observed, which can be related to two possible causes. First, the inaccuracy of the EM simulations, which proved to be very critical at such high frequencies. In particular, given the large computation effort required by the EM simulations, a trade-off between complexity and accuracy must be chosen. Considering the 4-stage architecture of the PA, even relatively small discrepancies between the EM model and the actual behavior of each passive network lead to significant differences when considering the entire PA. A second source of inaccuracy is related to the input/outpu bonding wires. In particular, the MMIC was designed accounting for the bonding wire inductance of the final assembly of the PA. However, for the measurements here reported, a prototype mounting was implemented in-house, where, with the available facilities, it was difficult to accurately control the actual shape of the bonding wires and thus their inductance.

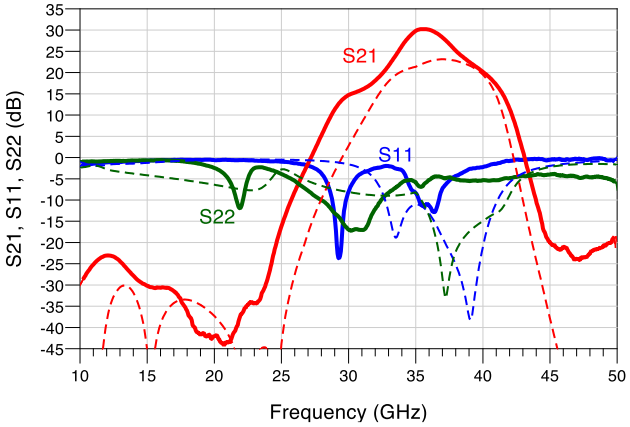

Fig. 6. Comparison between simulated (dashed) and measured small-signal performance.

For the large-signal characterization, pulsed measurements with very short pulse duty cycle (20 μs pulse width, 5 ms pulse period) had to be adopted, due to the very limited heat/power dissipation capability of the current test-jig (Fig. 5). The latter is a thin brass carrier placed on top of the probe station chuck, held steady by the vacuum pump pressure only, thus the carrier-chuck thermal resistance is very high. The final test-jig, with thermal dissipation capabilities and in/out coaxial connectors, is under development to allow for CW characterization. The measurement set-up is partially shown in Fig. 7: input and output power are measured with pulsed power meters and a commercial amplifier, providing up to 30 dBm output power in the frequency range of interest, is used as driver.

The measured large signal performance is reported in Fig. 8 and Fig. 9. Fig. 8 shows, as an example, the power sweep results at 36.5 GHz, where a maximum output power of 36.4 dBm was recorded at 6.8 dB compression. The associated gain and PAE are 25.7 dB and 29.8 %, respectively. Fig. 9 reports, instead, the measurement results in the entire 34 GHz – 38 GHz frequency range (at present frequencies above 38 GHz have not been tested due to the limitations of the measurement set-up), compared to simulation predictions: the measured output power is in excess of 36 dBm while the operative gain and PAE are above 25 dB and 28 %, respectively at all frequencies. The observed discrepancies between simulations and measurements can be ascribed to the

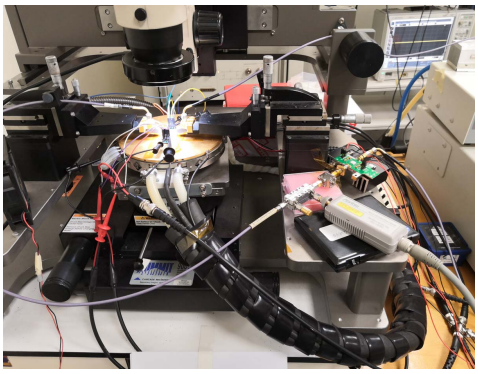

Fig. 7. Picture of the large-signal characterization set-up.

large difference in the thermal state of the MMIC under CW (simulations) and pulsed regime (measurements).

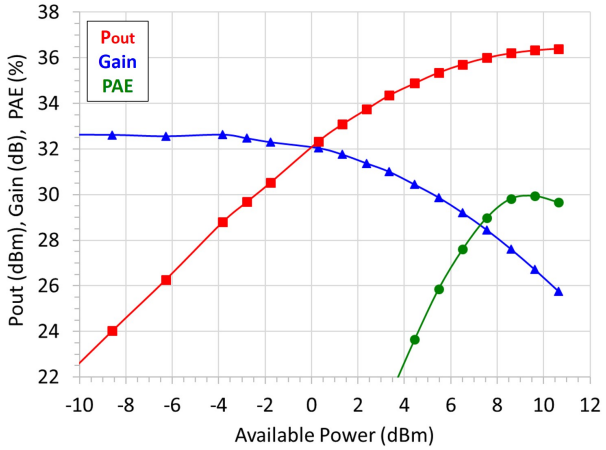

Fig. 8. Measured large-signal performance at 36.5 GHz.

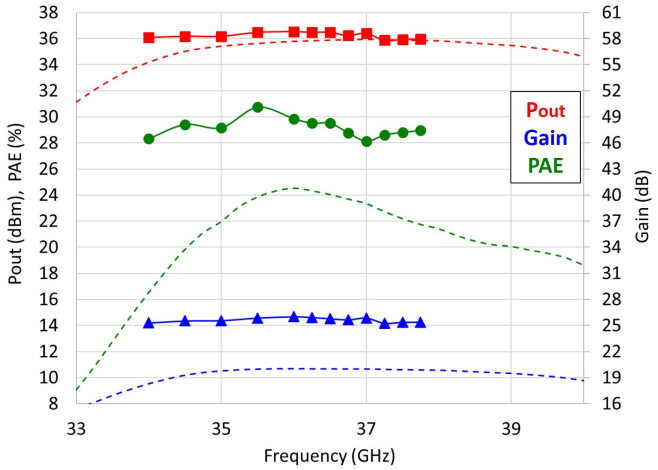

Fig. 9. Comparison between simulated (dashed) and measured large-signal performance vs. frequency.

V. Conclusion

A Ka-band 4 W MMIC power amplifier for CW radar applications, developed on 0.1 μm GaN/Si commercial process is presented. The 4-stage single-ended PA, characterized under pulsed large-signal conditions, shows an output power in excess of 36 dBm, an operative gain in excess of 25 dB and a PAE above 28 % in the 34 GHz – 38 GHz frequency range.

Acknowledgment

This research was developed under the National Project 2015CPC2MA funded by the Italian Ministry of Instruction, University and Research (MIUR).

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