Experimental Characterization of Charge Trapping Dynamics in 100-nm AlN/GaN/AlGaN-on-Si HEMTs by Wideband Transient Measurements

Experimental characterization of charge trapping dynamics in 100-nm AlN/GaN/AlGaN-on-Si HEMTs by wideband transient measurements

Alberto Maria Angelotti, *Student Member, IEEE*, Gian Piero Gibiino, *Member, IEEE*, Alberto Santarelli, *Member, IEEE* and Corrado Florian, *Member, IEEE*

***Abstract*— This work deals with the characterization of charge-trapping dynamics in a novel 100-nm double-heterojunction AlN/GaN/AlGaN-on-Si RF HEMT process. In order to study the de-trapping mechanisms, we perform wideband acquisitions of the transient behavior by sweeping the pulsed voltages to cover the entire device operating area. The fast acquisition also enables the characterization of the charge capture behavior, a key aspect for RF performance. From the analysis of the drain current transients, time constants are extracted, showing a fundamental release time constant in the order of 0.1-1 ms, and more than one capture constants, the fastest being in the order of 300 ns. To the best of our knowledge, this is the first time that trapping dynamics under large-signal regime are characterized for this type of process.**

***Index Terms*— GaN-on-Si, HEMT, charge trapping, transient measurements, pulsed measurements.**

I. Introduction

GAllium Nitride (GaN) Monolithic Microwave Integrated Circuit (MMIC) processes on Silicon Carbide (SiC) [1] or Silicon (Si) [2] are key enablers for solid-state K/Ka-band microwave power amplifiers (PAs). Despite the lower thermal conductivity, GaN-on-Si is of particular interest for the lower costs and the integrability with Si processes. However, GaN HEMTs are typically affected by electron trapping mechanisms, whose complex behavior causes well-known effects such as current collapse, knee walk-out, and kink effects [3], [4]. These phenomena have a critical impact on radio-frequency (RF) applications, e.g., in pulsed radar [5], [6] or broadband-modulated telecom transmitters [7]. Therefore, the development of characterization methods is fundamental for process improvement and for accurate empirical modeling.

Pulsed-IV (PIV) measurements are commonly used for trap-induced gate- and drain-lag characterization and modeling [8]–[12]. The estimation of the charge de-trapping time constants (τ) can be performed by means of low-frequency (LF) Y-parameters [13], drain current transient analysis [14]–[19], or noise measurements [20]. Fast charge capture [19], [21] is usually neglected, despite being important for the RF behavior [11], [19]. Since τ in GaN ranges between $\sim 10^{-8}$ and 10^{-1} s, obtaining a comprehensive characterization for both trapping and de-trapping mechanisms represents a challenge from the measurement perspective. In addition, the dynamic behavior is most often studied at just one or a very few quiescent and pulsed voltages, whereas large-signal (LS) modeling entails nonlinear dynamics across the entire safe operating area.

While most of the literature is dedicated to GaN-on-SiC RF HEMTs or on GaN-on-Si devices for power electronics, this paper investigates the charge-trapping dynamics of a novel 100-nm double-heterojunction AlN/GaN/AlGaN-on-Si RF HEMT technology. This type of stack, particularly developed for obtaining high 2DEG densities with short gate lengths [22], involves a different trapping configuration with respect to ordinary AlGaN/GaN HEMTs [23]. As such, it has been barely addressed in literature. In this work, we exploit the flexibility of a custom measurement setup to characterize, for the first time, both fast capture and slow de-trapping transients. The paper is organized as follows. In Sec. II, the technology is described. Section III outlines the adopted characterization approach by depicting the measurement bench, illustrating the configuration of the pulsed excitations and the identification of time constants. Sections IV and V are devoted to the analysis of de-trapping and trapping transients, respectively. Conclusions are drawn in Sec. VI.

II. Process technology

The considered GaN-on-Si process, a 100-nm mushroom-gate double-heterojunction AlN/GaN/AlGaN HEMT with 250-nm gate-source distance, is designed to overcome AlGaN/GaN limitations for sub-200-nm gate lengths [22], where the punch-through [24] of the buffer layer in the presence of high electric fields may induce short channel effects. As shown in Fig. 1a, the epitaxial structure is grown on

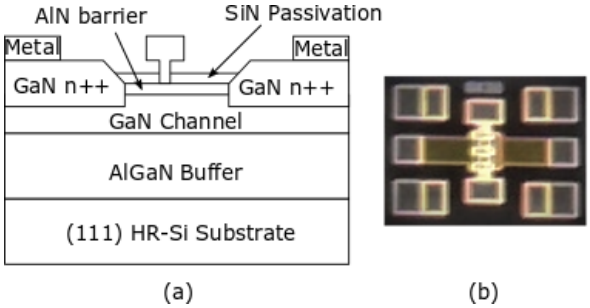

Fig. 1. GaN-on-Si technology: (a) HEMT structure. (b) Die photo.

Manuscript received XX, revised XX.

The authors are with the Department of Electrical, Electronic and Information Engineering "G. Marconi", University of Bologna, 40136, Bologna, Italy (e-mail: alberto.angelotti@unibo.it).

(111) high-resistive silicon (HR-Si) substrate. The introduction of an AlGaN layer acts as a back barrier preventing the electron flow into the buffer under high drain-source voltage (50 V breakdown), improving the electron confinement and allowing for high drain current density (1.3 A/mm at V_{DS} = 3 V) without buffer dopants [25], [26]. Due to the high spontaneous polarization and the wide-bandgap (6.2 eV) of the AlN barrier, the AlN/GaN heterostructure effectively allows for high 2DEG density ($> 10^{13}$ cm^{-2}) [27]. In-situ grown SiN layer minimizes the strain relaxation, reducing the defects on the AlN layer and improving the reliability of the device under high electric fields [28]. The resulting cutoff frequency is f_t=120 GHz. At 30 GHz and V_{DS} = 12 V, the typical RF power density is 3.3 W/mm (6.6 W/mm peak), with a maximum stable gain of 13 dB (2x25 μm device). The device-under-test (DUT) is a 6×30 μm HEMT die in common-source configuration (Fig. 1b). The threshold voltage measured at dc conditions is $V_{TH} \approx -1.6$ V for a current density of $I_D \approx 5\frac{\text{mA}}{\text{mm}}$. This value displays almost no dependency on the applied V_{DS}, due to the AlGaN back-barrier preventing significant punch-through effects [24].

III. Experimental Characterization Approach

A. Measurement bench

The developed on-wafer bench is shown in Fig. 2. The pulsed excitations are applied with a two-channel, 120-MHz arbitrary function generator (AFG) by Agilent (81150A). A supply based on a wideband current feedback amplifier (ADA4870), featuring up to 50-MHz LS bandwidth (BW) with I/V swings of 1 A and 30 V, is adopted at the drain-source port. The voltages are sensed with passive probes, and the drain current is acquired with a 100-MHz current clamp (Keysight N2893A). All the probes are connected to a 2.5-GHz, 20-GSa/s digital sampling oscilloscope (Keysight 9254A).

This wideband setup provides great flexibility for DUT characterization, allowing to apply pulsed voltage waveforms with rise/fall times down to 100 ns. Differently from others [29], [30], this bench avoids the use of bias-tees, which may influence the device terminations and introduce ringings, whose instantaneous voltage peaks can jeopardize the characterization. A fixed 100-ms time acquisition window (100 MSa/s sampling rate, 10-ns time resolution, 10^7 points per acquisition) allows to finely capture not only the slow de-trapping transients, but also the fast capture transients which often fall beyond the BW available in typical pulsed setups.

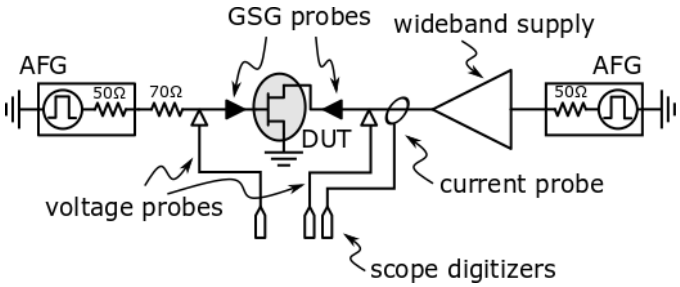

Fig. 2. Block diagram of the measurement setup.

B. Configuration of the pulsed excitations

The excitation consists of voltage pulses concurrently applied at gate and drain ports. The periodic pulsed waveforms are defined by a period $T = 100$ ms (one period per acquisition), and pulse widths $PW \in 5 \times [10^{-8}, 10^{-4}]$ s. The pulsed voltages applied during PW, i.e., the trap-filling pulses, are depicted with V_{GP} (gate) and V_{DP} (drain). The voltages applied during the $T - PW$ time-window (baseline) are referred to as quiescent voltages V_{GQ} (gate) and V_{DQ} (drain). An example of actual acquisitions is reported in Fig. 3, showing the capabilities of the setup to deliver clean pulsed voltage waveforms.

As the gate-source voltage is decreased and the drain-source voltage is increased, more charge will be trapped [3], producing gate- and drain-lag effects. A common way to evaluate the impact of these phenomena consists in measuring the differences among PIV characteristics from different quiescent points, with PW short enough to avoid self-heating (e.g., PW= 100 ns). In Fig. 4, we report the PIV characteristics from the nominal quiescent point, in comparison with the ones pulsed from $V_{GQ} = 0$ V, $V_{DQ} = 0$ V and $V_{GQ} = -2$ V, $V_{DQ} = 20$ V, exhibiting the presence of both gate and drain lag effects, and a trap-induced current reduction in the order of 100 mA/mm.

Given that trapping mechanisms can be faster than the typical PW (e.g., in the order of ns), and substantially faster than de-trapping, any of the pulsed current points of the PIV is the result of the partial trapping taking place during PW and of the de-trapping during $T - PW$. In general, a certain trapping state will be set depending on V_{GP}, V_{DP}, PW and T. These dependencies can be studied by analyzing the slow de-trapping current transients recovering to quiescent conditions (Fig. 3) after different pulsed configurations. To this aim, in Fig. 5 we report a representative characterization, in which

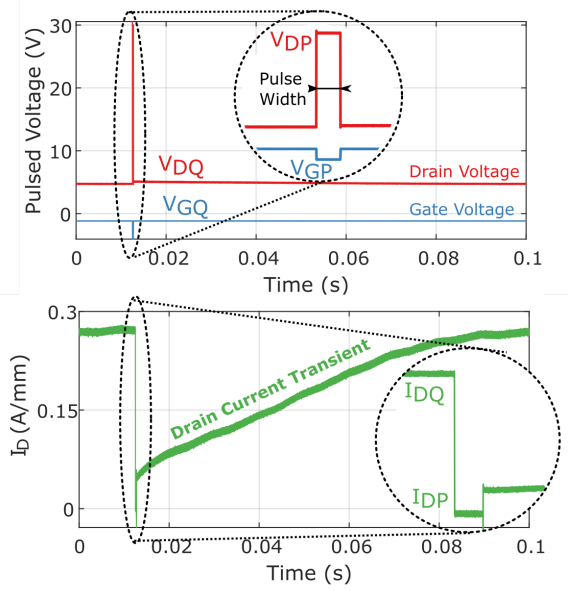

Fig. 3. Actual waveforms acquired with sampling time of 10 ns for concurrent gate and drain pulsed excitations inducing charge trapping and causing a drain current transient recovery.

the pulse amplitudes cover the four possible relationships between pulsed and quiescent values. These results confirm that the most evident current drop and longer recovery, hence the larger amount of trapped charge during PW, takes place when $V_{GP} < V_{GQ}$ and $V_{DP} > V_{DQ}$ (Fig. 5d). This is also the most evident behavior for LS PA design, as the dynamic RF loadline will typically reach maximum trapping conditions [8]. Conversely, Fig. 5a shows a practically constant current, meaning that almost no de-trapping has taken place during PW, due to the very short duration of PW w.r.t. the recovery time constants. Finally, Figs. 5b-c depict hybrid situations where either gate or drain has induced trapping and vice versa, with a mixed global effect on the resulting transients.

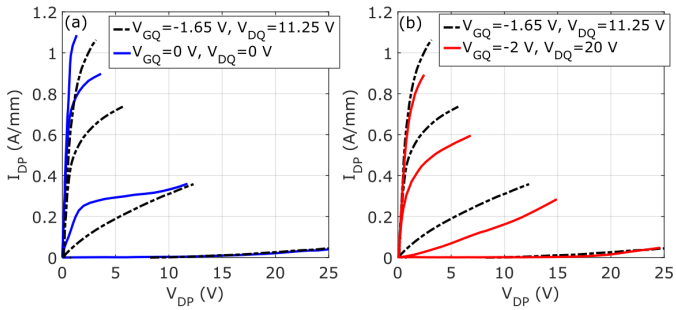

Fig. 4. Pulsed-IVs for the characterization of gate and drain lag from quiescent points (V_{GQ},V_{DQ})=(0 V, 0 V), (-2 V, 20 V) and (-1.65 V, 11.25 V). V_{GP} from -1.8 V to 0 V with 0.6 V step. PW=100 ns.

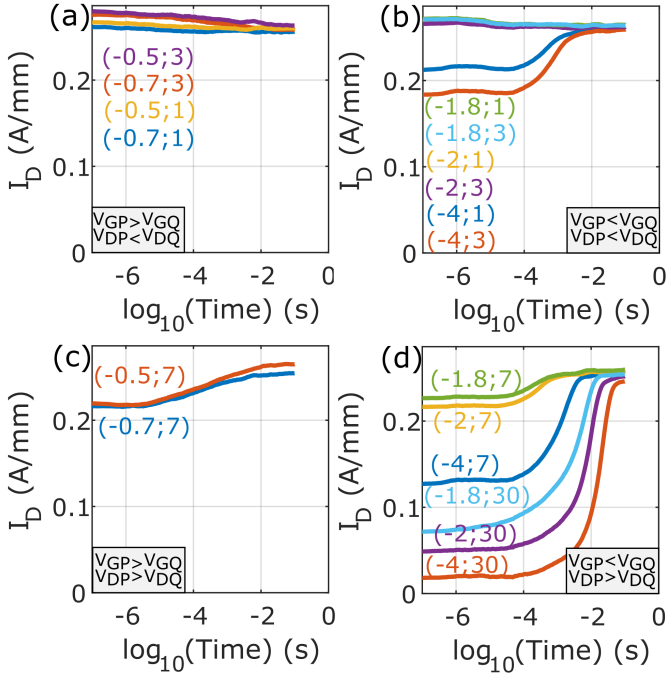

Fig. 5. Current transients in logarithmic time for all possible reciprocal relationships between pulsed values [PW=500 μs, -4 V $\leq V_{GP} \leq -0.5$ V, 10 V $\leq V_{DP} \leq$ 30 V, (V_{GP}, V_{DP}) indicated in each plot] and quiescent values ($V_{DQ} = 5$ V, $V_{GQ} = -1.14$ V, $T_c = 80$°C). a) Slight trapping transients, corresponding to a small amount of de-trapping during PW; b) de-trapping transients for $V_{GP} = -4, -2$ V, corresponding to trapping during PW; slight trapping transient for $V_{GP} = -1.8$ V, corresponding to limited de-trapping during PW; c) de-trapping transients, corresponding to trapping during PW; d) de-trapping transients, corresponding to trapping during PW.

Beyond its indirect enhancement of the de-trapping mechanisms, self-heating can have a significant direct impact on the drain current due to the dynamic dissipated power profiles between pulsed and quiescent conditions [9], so that thermal and charge trapping are often hard to separate for a given transient measurement. The thermal sensitivity of the DUT was measured, in static conditions, as being less than 0.6 $\frac{\text{mA}}{\text{mm°C}}$ for all the measured quiescent points for 40 ° $\leq T_c \leq$ 80 °C (T_c being the thermal chuck temperature). Therefore, we can exclude any significant direct thermal effect across a given transient. In addition, the quiescent points considered in the following are chosen to ensure the same quiescent dissipated power across the evaluated cases.

C. Drain Current Transient Characterization

In order to evaluate the impact of trapping on the DUT operation, two different metrics were used, both extracted from drain current transient measurements under pulsed excitations (Fig. 6): characteristic time-constants and normalized drain current differences.

The identification of characteristic time constants should allow to identify dominant trapping energy levels [15]. Beyond their physical significance, these constants give an estimate of the device memory time-scale, which is a key behavioral information for assessing application-like LS performance [7] and for developing accurate models. In general, current transients after a pulsed stimulus feature complex de-trapping dynamics, described by a continuous spectrum of exponential relaxation time-constants, which can be estimated using a wide variety of methods [14], [15], [17], [20], [31]. In this work, the popular method in [15], which is based on the log-time derivative of the current transient $\frac{dI_D(t)}{d\log(t)}$, is adopted as a representation of the time-constant spectrum for a given excitation (Fig. 6c). In this description, the presence of a strong peak (i.e., local maximum or minimum) is a key signature of the presence of a relevant trapping energy level, whose characteristic time-constant can then be deduced as the time location of the peak. Drain current differences are obtained between the beginning and the end of the current transient, and then normalized by the quiescent value to compare different

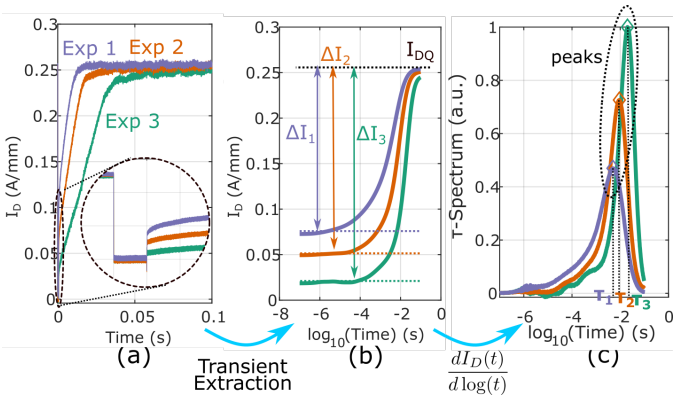

Fig. 6. Procedure used for the drain current transient measurements. (a) Current transient acquisition. (b) Plot of the current transients in logarithmic time scale and evaluation of the current drop. (c) Log-time derivative and extraction of trap time constants.

bias conditions (Fig. 6b). As such, they do not account for the time-scale in which the transient occurs [32].

IV. Analysis of Slow De-Trapping Transients

A. Thermal behavior

Arrhenius plots obtained from thermally-induced de-trapping current transients at different T_c are typically used to extract the trap activation energy (E_a). The Arrhenius plot for this DUT, extracted with $T_c \in [40, 80]$ °C and compensated for self-heating as in [33] (thermal resistance R_{TH}=110 $\frac{\text{K}}{\text{W mm}}$ as from foundry), displays a single significant trapping process (Fig. 7). The trap, with typical time constant in the order of 10^{-2} s, experiences a very weak dependence on temperature and an irregular plot alignment, eventually resulting in an approximated $E_a \simeq 0.2$ eV.

This experimental behavior has already been observed in 150-nm-gate-length AlN/GaN/AlGaN-on-Si HEMTs [34], while being significantly different from AlGaN/GaN-on-SiC HEMTs with similar gate lengths [20], pointing to possible differences in the underlying combined thermal and trapping mechanisms. In fact, since the Si substrate and the AlGaN back-barrier display a significantly higher thermal resistance w.r.t. the GaN buffer-SiC stack of typical HEMTs, the DUT internal temperature is mostly set by self-heating, reducing the sensitivity on T_c and limiting the time-constant variation, thus eventually leading to an ill-conditioned Arrhenius plot estimation. In addition, as will be shown in Secs. IV-B and IV-C, for this DUT the emission rate is strongly influenced by the actual quiescent and pulsed conditions. Whereas the Arrhenius characterization would assume a de-trapping of purely thermal origin, strong self-heating and field-induced effects on the carrier emission process, exacerbated by the extremely scaled gate length, depict a rather complex trapping kinetics. In this perspective, here E_a only represents an experimentally-derived *effective* (or *apparent*) activation energy, rather than a physical property.

B. Pulsed voltage dependency

We characterize the de-trapping recovery transients due to different voltage amplitudes when both gate and drain excitations cause fast trap activation. In particular, V_{GP} is set to -4 V (deep OFF-state), -2 V (sub-threshold region) and -1.8 V (ON-state), whereas 7 V $\leq V_{DP} \leq$ 30 V. Adopting the definitions used in Fig. 6, for each current transient acquired we evaluate the fundamental time-constant and the relative current drop, obtaining Figs. 8a and 8b, respectively. Notably, τ ranges from less than 100 μs up to more than 10 ms depending on the pulsed voltages, remarking that measuring the dynamic behavior at just one bias, akin to LF Y-parameter, or noise characterizations [20], or at just one pulsed configuration, leads only to a local description that will fall short under LS wideband regimes. The results confirm that the larger the pulsed drain voltage, and the more the gate voltage is pushed towards the OFF-state, the longer the recovery time to quiescent conditions, showing a sub-linear time-constant dependency on the pulsed drain voltage. Moreover, τ decreases as the drain quiescent voltage increases, pointing to a field-assisted emission process [31]. The relative current drop shows a similar dependency, exhibiting substantial variations up to a full drop of the quiescent current for the larger drain voltage amplitude. Considering the different trap signatures of this DUT w.r.t. the ones in C- or Fe-doped AlGaN/GaN HEMTs [35], buffer dopants are realistically ruled out in determining the characterized trapping behavior. This aspect, together with the presence of the SiN cap layer, which is expected to effectively passivate surface states, suggests that the observed effects are due to defects in the buffer stack, whose impact is

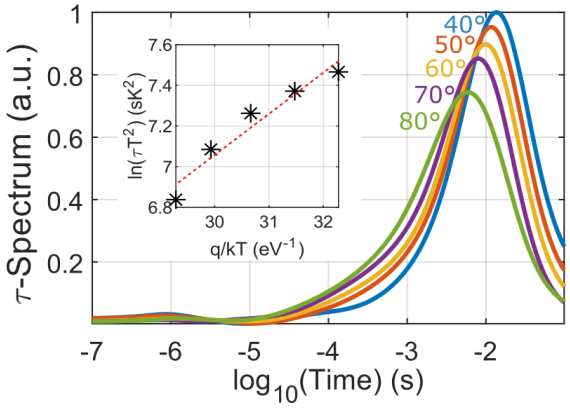

Fig. 7. Time constant spectra and thermal activation of the trap process. The resulting Arrhenius plot and activation energy are reported. Quiescent Conditions: $V_{DQ} = 5$ V, $V_{GQ} = -1.25$ V. Pulse parameters: PW=100 μs, $V_{GP} = -4$V, $V_{DP} = 20$V.

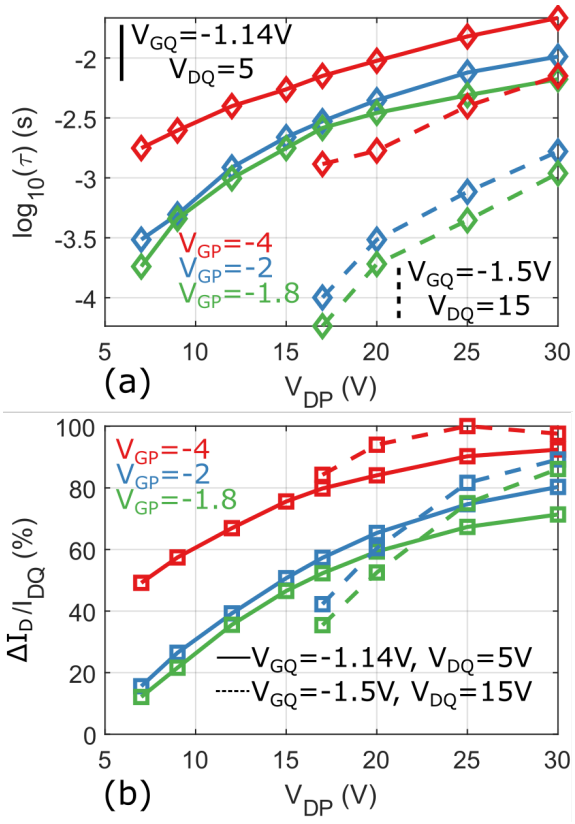

Fig. 8. Time-constant (a) and normalized current drop (b) dependence on filling pulse gate and drain voltages at a pulse width of 500 μs and chuck temperature $T_c = 80$°C, for two different bias points.

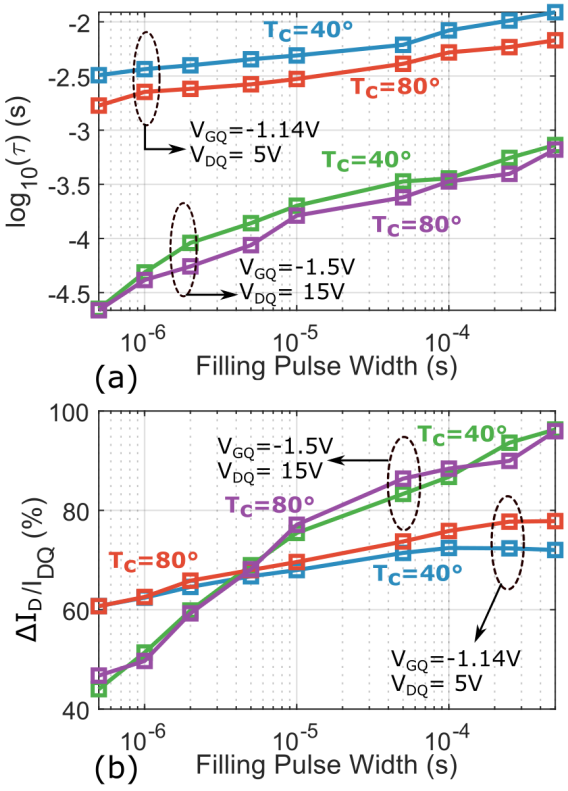

Fig. 9. Time-constants (a) and normalized current drop (b) dependence on the filling pulse width and temperature for trapping conditions to ensure full current recovery for all pulse widths and temperatures: $\boldsymbol{V_{GP} = -2}$ V, $\boldsymbol{V_{DP} = 25}$ V. Two distinct bias points are reported: $\boldsymbol{V_{GQ} = -1.14}$ V, $\boldsymbol{V_{DQ} = 5}$ V (blue: $\boldsymbol{T_c = 40}$°C, red: $\boldsymbol{T_c = 80}$°C) and $\boldsymbol{V_{GQ} = -1.5}$ V, $\boldsymbol{V_{DQ} = 15}$ V (green: $\boldsymbol{T_c = 40}$°C, purple $\boldsymbol{T_c = 80}$°C).

augmented by the high electric field induced by the short gate length [26].

C. Filling pulse dependency

Characterizing the dependency on the filling pulse width provides additional information on the characteristics of the trapping mechanisms [17], [30]. As PW increases, a larger amount of charge gets captured, up to a certain saturation level for the given pulsed voltages [30], [31]. We sweep PW from 50 ns to 500 μs at two different chuck temperatures. Figure 9a shows that τ increases from a few ms up to hundred of ms for $V_{GQ} = -1.14$ V, $V_{DQ} = 5$ V, demonstrating that the PW still influences the trapping behavior up to 500 μs. The increase rate of τ is even larger for $V_{GQ} = -1.5$ V, $V_{DQ} = 15$ V, despite showing smaller absolute values from less than 100 μs up to 1 ms. More in detail, both τ and the relative current drop (Fig. 9b) show a quasi logarithmic dependency on PW, which is only barely influenced by the chuck temperature. As documented in literature [17], [36], this type of behavior could be ascribed to the presence of point defects, given that the regular reduction of the capture rate would be caused by a localized Coulomb capture barrier, whose height increases with the filling pulse.

V. Analysis of Fast Trapping Transients

The dependency on the filling pulse in the range up to 500 μs indicates that capture mechanisms critically impact the RF performance [19], [20]. Thanks to the fine acquisition of the waveforms (10-ns resolution) and wide-ranging voltage excitation capabilities, we are able to observe the fast drain current transients during the filling pulse, which have been rarely studied in literature [19].

In Fig. 10a, we show the trapping transients during PW=500 μs (the longest acquired) with $V_{GQ} = -1.14$ V, $V_{DQ} = 5$ V for different filling-pulse amplitudes. The capture transients critically depend on the applied pulsed voltage, confirming (Sec. IV) that the electric field distribution strongly influences the trapping mechanisms. Figure 10b shows the extracted time constants with the same technique as in Sec. III-C, with three distinct processes detected: T1 and T3 display a capture-type behavior, while T2 operates as a weak electron-release trapping center. The dominant fast-trapping time constant is the one associated with T1, with a value $\sim$ 300 ns. T2 and T3, characterized by time constants in the μs - 100 μs range, are enhanced by an increase in the pulsed drain voltage. The effects of the three processes and the relative time constants tend to blur for lower values of drain pulsed voltage, leading to a unique broadened spectral peak associated with a strongly non-exponential transient behavior.

VI. Conclusion

The current transient analysis conducted, for the first time, on a 100-nm double-heterojunction AlN/GaN/AlGaN-on-Si RF HEMT process, has revealed a fundamental de-trapping time-constant in the 0.1-1 ms range, showing reduced thermal sensitivity and strong field dependency. Differently from AlGaN/GaN HEMTs, this behavior is not due to intentional doping, but indicates trapping in the buffer stack, whose impact is exacerbated by the high electric field induced by the short gate length. In addition, the logarithmic dependency on the filling pulse width suggests the presence of point defects. The capture transient analysis has revealed a much smaller

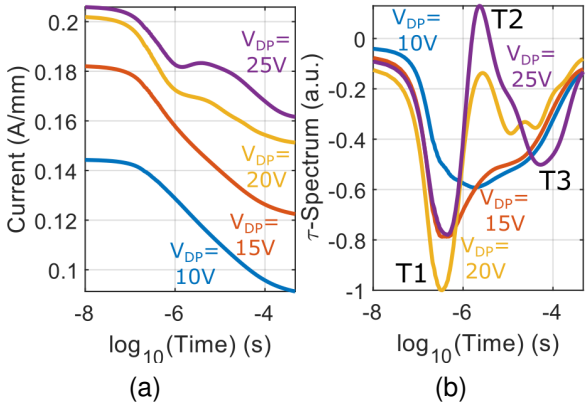

Fig. 10. Current transients (a) and relative time-constant spectra (b) during trapping pulses for four different pulsed conditions: $\boldsymbol{V_{GP} = -1.5V}$, $\boldsymbol{V_{DP} = 10 - 25V}$. The bias points is set at $\boldsymbol{V_{GQ} = -1.14}$ V, $\boldsymbol{V_{DQ} = 5}$ V, for $\boldsymbol{T_c = 40}$°C and a filling pulse $\boldsymbol{PW}$=500 $\boldsymbol{\mu}$s.

time constant at $\sim$ 300 ns, and further effects in the μs range. These experimental results indicate that known physics models are not directly suitable for this novel HEMT structure, and that the common single-bias characterization methods are not representative of the global trap behavior under LS excitation.

REFERENCES

[1] C. F. Campbell, Ming-Yih Kao, and S. Nayak, "High efficiency Ka-band power amplifier MMICs fabricated with a 0.15µm GaN on SiC HEMT process," in *IEEE MTT-S Int. Microwav. Symp. Dig.*, June 2012, pp. 1–3.

[2] J. Moron, R. Leblanc, F. Lecourt, and P. Frijlink, "12W, 30% PAE, 40 GHz power amplifier MMIC using a commercially available GaN/Si process," in *IEEE MTT-S Int. Microw. Symp. Dig.*, June 2018, pp. 1457–1460.

[3] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, March 2001.

[4] G. Meneghesso, F. Zanon, M. J. Uren, and E. Zanoni, "Anomalous Kink Effect in GaN High Electron Mobility Transistors," *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 100–102, Feb 2009.

[5] J. Delprato, D. Barataud, M. Campovecchio, G. Neveux, C. Tolant, and P. Eudeline, "Measured and simulated impact of irregular radar pulse trains on the pulse-to-pulse stability of microwave power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3538–3548, Dec 2014.

[6] G. P. Gibiino, A. M. Angelotti, A. Santarelli, and C. Florian, "Microwave characterization of trapping effects in 100-nm gan-on-si hemt technology," *IEEE Microwave and Wireless Components Letters*, vol. 29, no. 9, pp. 604–606, Sep. 2019.

[7] C. Florian, T. Cappello, A. Santarelli, D. Niessen, F. Filicori, and Z. Popović, "A prepulsing technique for the characterization of gan power amplifiers with dynamic supply under controlled thermal and trapping states," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 12, pp. 5046–5062, Dec 2017.

[8] A. Santarelli *et al.*, "A Double-Pulse Technique for the Dynamic I/V Characterization of GaN FETs," *IEEE Microw. Wirel. Comp. Lett.*, vol. 24, no. 2, pp. 132–134, Feb 2014.

[9] S. A. Albahrani, A. Parker, M. Heimlich, and B. Schwitter, "Iso-Trapping Measurement Technique for Characterization of Self-Heating in a GaN HEMT," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 102–108, Jan 2017.

[10] G. P. Gibiino, A. Santarelli, and F. Filicori, "A GaN HEMT Global Large-Signal Model Including Charge Trapping for Multibias Operation," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 11, pp. 4684–4697, Nov 2018.

[11] H. Hirshy, M. Singh, M. A. Casbon, R. M. Perks, M. J. Uren, T. Martin, M. Kuball, and P. J. Tasker, "Evaluation of Pulsed I–V Analysis as Validation Tool of Nonlinear RF Models of GaN-Based HFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5307–5313, Dec 2018.

[12] S. A. Albahrani, D. Mahajan, J. Hodges, Y. S. Chauhan, and S. Khandelwal, "ASM GaN: Industry Standard Model for GaN RF and Power Devices—Part-II: Modeling of Charge Trapping," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 87–94, Jan 2019.

[13] N. K. Subramani, J. Couvidat, A. A. Hajjar, J. Nallatamby, R. Sommet, and R. Quéré, "Identification of GaN Buffer Traps in Microwave Power AlGaN/GaN HEMTs Through Low Frequency S-Parameters Measurements and TCAD-Based Physical Device Simulations," *IEEE J. Electron Devices Soc.*, vol. 5, no. 3, pp. 175–181, May 2017.

[14] D. V. Lang, "Deep level transient spectroscopy: A new method to characterize traps in semiconductors," *Journal of Applied Physics*, vol. 45, no. 7, pp. 3023–3032, 1974.

[15] J. Joh and J. A. del Alamo, "A Current-Transient Methodology for Trap Analysis for GaN High Electron Mobility Transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 132–140, Jan 2011.

[16] S. DasGupta, M. Sun, A. Armstrong, R. J. Kaplar, M. J. Marinella, J. B. Stanley, S. Atcitty, and T. Palacios, "Slow Detrapping Transients due to Gate and Drain Bias Stress in High Breakdown Voltage AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2115–2122, Aug 2012.

[17] D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Brückner, M. Mikulla, G. Meneghesso, and E. Zanoni, "Deep-level characterization in gan hemts-part i: Advantages and limitations of drain current transient measurements," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3175, Oct 2013.

[18] S. A. Albahrani, A. E. Parker, and M. Heimlich, "Identifying a Double-Energy-Level Trap Center in a GaN HEMT by Performing Three-Stage Pulse Measurements," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3693–3699, Sep. 2016.

[19] A. Benvegnù *et al.*, "Trap characterization of AlGaN/GaN HEMTs through drain current measurements under pulsed-RF large-signal excitation," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–4.

[20] M. Bouslama, V. Gillet, C. Chang, J. Nallatamby, R. Sommet, M. Prigent, R. Quéré, and B. Lambert, "Dynamic Performance and Characterization of Traps Using Different Measurements Techniques for the New AlGaN/GaN HEMT of 0.15-μm Ultrashort Gate Length," *IEEE Trans. Microw. Theory Techn.*, pp. 1–8, 2019.

[21] J. L. Gomes, L. C. Nunes, C. F. Gonçalves, and J. C. Pedro, "Deep-Level Traps' Capture Time Constant and its Impact on Nonlinear GaN HEMT Modeling," in *Proc. Int. Workshop Int. Nonlin. Microw. Millimetre-wave Circ. (INMMIC)*, July 2018, pp. 1–3.

[22] F. Medjdoub, M. Zegaoui, B. Grimbert, D. Ducatteau, N. Rolland, and P. A. Rolland, "First demonstration of high-power gan-on-silicon transistors at 40 ghz," *IEEE Electron Device Letters*, vol. 33, no. 8, pp. 1168–1170, Aug 2012.

[23] R. Kabouche, J. Derluyn, R. Pusche, S. Degroote, M. Germain, R. Pecheux, E. Okada, M. Zegaoui, and F. Medjdoub, "Comparison of c-doped aln/gan hemts and aln/gan/algan double heterostructure for mmw applications," in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, Sep. 2018, pp. 5–8.

[24] M. J. Uren, K. J. Nash, R. S. Balmer, T. Martin, E. Morvan, N. Caillas, S. L. Delage, D. Ducatteau, B. Grimbert, and J. C. De Jaeger, "Punch-through in short-channel algan/gan hfets," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 395–398, Feb 2006.

[25] F. Medjdoub, M. Zegaoui, N. Rolland, and P. A. Rolland, "Demonstration of low leakage current and high polarization in ultrathin aln/gan high electron mobility transistors grown on silicon substrate," *Applied Physics Letters*, vol. 98, no. 22, p. 223502, 2011. [Online]. Available: https://doi.org/10.1063/1.3595943

[26] F. Medjdoub, D. Ducatteau, M. Zegaoui, B. Grimbert, N. Rolland, and P.-A. Rolland, "Trapping effects dependence on electron confinement in ultrashort GaN-on-si high-electron-mobility transistors," *Applied Physics Express*, vol. 5, no. 3, p. 034103, mar 2012.

[27] F. Medjdoub, "Ultrathin barrier GaN-on-Silicon devices for millimeter wave applications," *Microelectronics Reliability*, vol. 54, no. 1, pp. 1 – 12, 2014.

[28] G. Meneghesso *et al.*, "First reliability demonstration of sub-200-nm AlN/GaN-on-Silicon double-heterostructure HEMTs for Ka-Band applications," *IEEE Trans. Device Mater. Rel.*, vol. 13, no. 4, pp. 480–488, Dec 2013.

[29] A. Santarelli *et al.*, "Multi-bias nonlinear characterization of GaN FET trapping effects through a multiple pulse time domain network analyzer," in *Proc. Eur. Microw. Int. Circ. Conf. (EuMIC)*, Sep. 2015, pp. 81–84.

[30] C. F. Gonçalves, L. C. Nunes, P. M. Cabral, and J. C. Pedro, "Pulsed I/V and S-parameters measurement system for isodynamic characterization of power GaN HEMT transistors," *Int. J. RF Microw. Computer-Aided Eng.*, vol. 28, no. 8, p. e21515, 2018.

[31] O. Mitrofanov and M. Manfra, "Poole-Frenkel electron emission from the traps in AlGaN/GaN transistors," *Journal of Applied Physics*, vol. 95, no. 11, pp. 6414–6419, 2004.

[32] ——, "Dynamics of trapped charge in GaN/AlGaN/GaN high electron mobility transistors grown by plasma-assisted molecular beam epitaxy," *Applied Physics Letters*, vol. 84, no. 3, pp. 422–424, 2004.

[33] A. Chini, F. Soci, M. Meneghini, G. Meneghesso, and E. Zanoni, "Deep levels characterization in gan hemts—part ii: Experimental and numerical evaluation of self-heating effects on the extraction of traps activation energy," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3176–3182, 2013.

[34] M. Bouslama, A. Al Hajjar, R. Sommet, F. Medjdoub, and J. Nallatamby, "Characterization and Electrical Modeling Including Trapping Effects of AIN/GaN HEMT 4×50um on Silicon Substrate," in *Eur. Microw. Int. Circ. Conf. (EuMIC)*, Sep. 2018, pp. 333–336.

[35] D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Brückner, M. Mikulla, G. Meneghesso, and E. Zanoni, "Deep-level characterization in gan hemts-part i: Advantages and limitations of drain current transient measurements," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3166–3175, Oct 2013.

[36] A. Hierro, A. Arehart, B. Heying, M. Hansen, J. Speck, U. Mishra, S. DenBaars, and S. Ringel, "Capture Kinetics of Electron Traps in MBE-Grown n-GaN," *physica status solidi (b)*, vol. 228, no. 1, pp. 309–313, 2001.