The X-Hall Sensor: Toward Integrated Broadband Current Sensing

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***Abstract*— This paper presents the X-Hall sensor, a viable sensing architecture for implementing a silicon-integrated, broadband, current/magnetic sensor. The X-Hall sensor overcomes the bandwidth limit of the state-of-the-art Hall sensors by replacing the spinning-current technique with DC-biased-based, passive offset compensation. In this way, the X-Hall architecture removes the methodological bandwidth limit due to the spinning-current technique and allows for exploiting the Hall probe up to its practical limit, which is set by the parasitic capacitive effects. Moreover, the X-Hall architecture allows to push the practical bandwidth limit at higher frequencies due to both the removal of the switches inherent in the spinning-current approach and a specifically designed analog front-end. To this end, a differential-difference current-feedback amplifier (DDCFA) is proposed as analog front-end in the X-Hall sensor. A prototype of the proposed X-Hall architecture is implemented in BCD 0.16-µm silicon technology to experimentally assess the performance of the X-Hall architecture. The passive offset compensation implemented into the X-Hall architecture is frequency independent and preserves an adequate offset reduction performance, though less efficient than the spinning-current technique operated at low frequency. Experimental dynamic tests on the prototype identify the presence of an additive parasitic dynamic perturbation due to the package that prevents from fully exploiting the X-Hall prototype up to its designed bandwidth limit. However, the implementation of a post de-emphasis digital filter allows to mitigate for the dynamic perturbation and to experimentally achieve a sensor bandwidth of 4 MHz, which is the broadest bandwidth ever demonstrated by a purely Hall-effect based sensor.**

***Index Terms*—application specific integrated circuit (ASIC); broadband current measurement; CMOS; current sensor; Hall effect; Hall probe; magnetometers; offset; overcurrent detection (OCD); passive offset compensation; power electronics.**

I. Introduction

THERE is a general emerging need in power electronics to detect and measure fast-varying currents and magnetic fields. This need is driven by the development of innovative power devices [1], [2], which are able to operate at high frequencies and high power rates, and by the emerging of very fast response (VFR) applications, such as dynamic voltage scaling in microprocessors [3], [4] and high-frequency AC inverters [5]. In VFR applications, the power converter must be able to change the output voltage in the microsecond scale and beyond, requiring voltage and current measurements with very fine time resolutions. Associated with all the power applications, there also is the requirement of preventing failures. Among these, the most common one is the overcurrent event due to short circuits and malfunctions [6]. In high power circuits, it is fundamental to detect this kind of failure and switch off the power system within microseconds to avoid permanent damage.

The gold-standard technique for broadband current measurement is based on coils, either the Rogowski coil or current transformer (CT). Broadband current probes available on the market can achieve bandwidth in the order of GHz (e.g., Tektronix CT6 [7]) but they all lose the DC component of the current and magnetic field. To compensate for the loss of DC information, a hybrid solution combining CT with Hall sensor has been developed, achieving bandwidth in the order of hundreds of MHz (e.g., Keysight N2783A [8]). All these commercial current probes are able to measure currents with wide bandwidth (> 100 MHz) and good accuracy (1% of the reading), but their architectures are cumbersome and hard to be implemented in silicon technology. Integrating the current sensor into the same chip together with the power device would have considerable impacts on the final application since both the occupied space and the weight of the final system could be reduced, while the sensor would be less sensitive to external interferences.

The Hall-effect sensor is a viable technology to achieve integration with the power device, but it is usually limited in bandwidth to hundreds of kHz or, maximum to 1 MHz [9], [10]. The fastest current sensor based on the Hall-effect and realized in bulk CMOS technology is the Allegro® ACS730 [11], while wider bandwidth can be achieved by using quantum-well Hall

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sensor (QWHS) realized on heterostructures, like the one provided by Asahi Kasei® [12]. QWHS can achieve a bandwidth of tens of MHz [13], but must be realized by using exotic and expensive semiconductor technologies.

There have been recent attempts to either integrate the hybrid coil-Hall architecture into a silicon chip [14], [15] or to extend the bandwidth of purely Hall-effect sensors realized on bulk silicon [16], [17]. Jiang and Makinwa [14] proposed a multi-path technique that combines a spun Hall sensor with an integrated pick-up coil. This sensor achieves 3 MHz bandwidth with a residual offset of only 40 μT, but it consumes more than 7.7 mA, it requires off-chip components, and it occupies more than 8 mm^2, which is a considerable area that may greatly affect the final cost of the power system. Moreover, the multi-path architecture requires the fine tuning of the frequency responses of the two probes to minimize the attenuation at the crossover frequency point. Funk and Wicht [15] proposed to integrate a Rogowski coil into a silicon chip and combine it with a Hall sensor to preserve the sensing capabilities on DC and low-frequency components of the current. This measurement system is mainly based on the Rogowski coil: the bandwidth depends on the parasitic elements of the integrated coil, and the system shows a bandwidth-sensitivity trade-off. Moreover, the hybrid sensor suffers from a strong frequency dispersion of its global sensitivity, up to 5%. Li et al. [17] combine the standard spun Hall sensor (i.e., bias-operated by means of the so-called *spinning-current* technique, which is a dynamic offset cancellation method required to cope with the intrinsic high-value offset in CMOS Hall-effect sensor [18]–[20]) with discrete-time (DT) offset and noise cancellation circuits to optimize the accuracy and bandwidth, though the system is still prone to the main frequency limits typical of spun Hall-effect sensors. In this framework, Crescentini et al. [16] demonstrated that the lower frequency limits in Hall-effect probes are: *i)* a *practical* limit set by the capacitive load of the analog front-end (AFE) and *ii)* a *methodological* limit set by the spinning-current technique. In [16], the authors minimized the capacitive load of the AFE to about 1 pF, achieving a *practical* bandwidth limit of the Hall-effect probe of 15 MHz, but the spinning-current operation still limited the bandwidth of the current sensor to approximately 1 MHz.

This paper presents and experimentally investigates the X-Hall sensor architecture as a solution for broadening the bandwidth of purely Hall-effect sensors by both eliminating the spinning-current technique (thus, the associated methodological limit) and minimizing the capacitive load seen by the Hall probe. The X-Hall sensor is based on an innovative topology of the Hall probe: the classic spinning-current technique is replaced by a purely DC biasing, and a passive offset reduction is implemented at the probe level, in contrast to [21] where it is carried out at the sensor level. From a general standpoint, the passive offset compensation defined in the X-Hall architecture preserves an adequate offset reduction performance and offers the paramount advantage of not limiting the bandwidth, though it is less efficient than the spinning-current technique operated at low spinning frequency. As an additional feature, also the minimization of the capacitive load is facilitated by the removal of the spinning-current technique since all the switches required by the latter are now unnecessary. This further advantage of the purely DC biasing is exploited by the design of a dedicated broadband amplifier. The X-Hall architecture can be successfully exploited to implement integrated current sensors with acquisition bandwidth from DC up to the *practical* bandwidth limit or the bandwidth limit set by the electronic front-end. The X-Hall concept was proposed for the first time in [22], where the theoretical idea of the X-Hall sensor was presented.

This paper extends [23], presented at the 2020 I2MTC conference, by: *i)* improving the technological description of the X-Hall probe; *ii)* improving the theoretical description of the passive offset reduction technique; *iii)* adding details on the analog front-end; *iv)* adding the description of the prototype; *v)* adding characterization of the statistical-, time-, and temperature-dispersion of the residual offset; *vi)* validating the prototype in two case studies. The paper is organized as follows. Section II describes the proposed X-Hall architecture. Section III discusses how the X-Hall architecture is implemented in the current sensor prototype. Section IV and Section V provide the static and dynamic characterizations of the prototype, as well as its validation in application-like scenarios. Finally, Section VI reports a comparative analysis with the state of the art and draws the conclusions.

II. The X-Hall Architecture

A. Topological Aspects of the X-Hall Probe

The X-Hall probe, as standard Hall-effect sensors, can be realized in almost all the semiconductor technologies used in power electronics circuits, from Silicon Carbide (SiC) to Gallium Nitride (GaN), and Silicon Bipolar-CMOS-DMOS technology (BCD), allowing integration with any kind of power device. The probe is realized by a lowly-doped n-type well surrounded by a grounded p-type well to ensure electric isolation from the substrate. The use of an n-well as the active sensing region is preferable to a p-well because it leads to higher current-related sensitivity S_I according to [4] and [5]. The encapsulation of the n-type well in the p-type well is unavoidable in bulk technologies, and it generates a non-uniform depletion region surrounding the active region that: *i)* creates a parasitic capacitance effect, *ii)* introduces asymmetries in the sensor, since the thickness of the depletion region is proportional to the local bias potential. These two effects are at the basis of bandwidth and accuracy limitations in Hall-effect probes and will be taken into consideration in the rest of the paper. An example of the vertical section of the X-Hall probe realized in BCD technology is shown in Fig. 1-a.

In the X-Hall architecture, the active region is octagonally shaped (Fig. 1-b) and accessible by a total of 8 contacts: 4 large contacts (B, T, L, R) used to bias the probe, and 4 small contacts (1, 2, 3, 4) used to sense the Hall voltage. In contrast to spun Hall sensor and due to the specific geometrical shape, the contacts of the X-Hall probe are dedicated to a single purpose (either biasing or sensing), so they can be optimized according to their specific function. The bias contacts are large-sized to

minimize the access resistance and are orthogonally oriented to the edges of the probe to maximize the sensitivity [21]. The sensing contacts are small-sized to minimize the parasitic capacitance associated with the contacts and to maximize the sensitivity [21]. However, sensing contacts cannot be shrunk too much, otherwise, lithography errors on the exact position of the contacts will increase the offset in the probe [21].

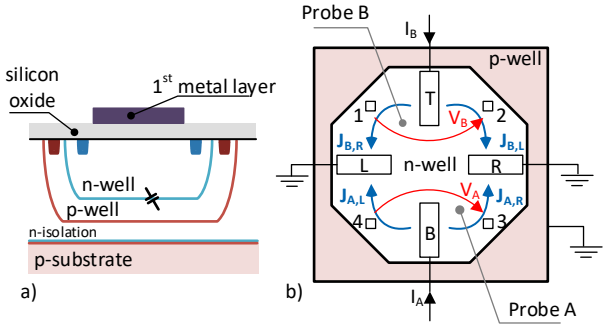

Fig. 1 (a) Vertical cross-section of the X-Hall probe showing the encapsulation of the active magnetic-sensitive region into a surrounding p-well and highlighting the presence of parasitic capacitive effects due to the reversed-biased junction. (b) Top view of the X-Hall probe showing its geometrical topology. The figure also shows the connection of the bias contacts and the nominal current densities flowing through the probe.

B. DC Biasing Scheme and Passive Offset Reduction

In the X-Hall configuration, two equal DC currents ($I_A = I_B = I_{bias}$) are fed to two opposite bias contacts (e.g., T and B) and the other two bias contacts are connected to a low-impedance node (for instance, R and L are connected to ground in Fig.1-b), while all the sensing contacts are electrically floating. This biasing scheme generates a global current density distribution with nominally uniform magnitude along the circumference inscribed in the active region, yet exciting four orthogonal directions (Fig. 2). From a general perspective, this biasing scheme concurrently polarizes the sensor in four orthogonal directions, like a "static" current-spinning technique. Actually, the orthogonal bias currents flow in different regions of the probe, thus, it is reasonable to assume that the local inhomogeneities will not be corrected.

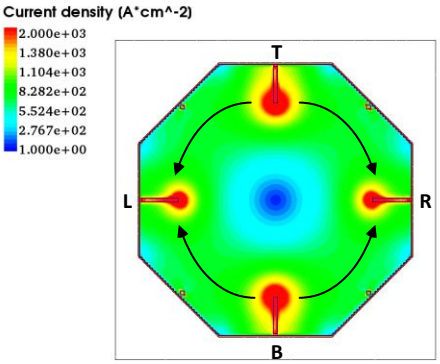

Fig. 2 TCAD simulation of the current density distribution over the octagonal probe accordingly to the X-Hall biasing scheme (500-µA currents injected into B and T contacts with no magnetic field applied).

According to this biasing scheme, it is also possible to identify two inner Hall-effect probes inside the octagonal active region. One inner probe (probe A) is placed below the horizontal axis of symmetry of the global probe, while the other inner probe (probe B) is placed above the same axis of symmetry (see Fig. 1-b). These two probes are biased by the same nominal current value I_{bias} and share the bias contacts L and R. Each inner probe works as a current splitting Hall-effect sensor. In the case of zero magnetic field and assuming a complete symmetry and homogeneity of the active region, the current density J_A splits into two equal current densities $J_{A,L}$ and $J_{A,R,}$ and the voltage potential V_A between contacts 3 and 4 is zero. The presence of a magnetic field component B_Z, i.e. orthogonally applied to the plane identified by the active region, creates a current imbalance, and the Hall voltage appears between contacts 3 and 4, so that $V_A = V_H$. Asymmetries along the horizontal axis, as well as global inhomogeneities (e.g., a resistivity gradient), give origin to an additive offset voltage:

$$V_A = V_H + V_{OS}^{(A)}. \tag{1}$$

Inner probe B behaves in the same manner but it generates a Hall voltage with opposite sign since the bias current flows in the opposite direction. Thus, voltage V_B can be written as:

$$V_B = -V_H + V_{OS}^{(B)}, \tag{2}$$

where it is reasonable to assume that the offset voltage $V_{os}^{(B)}$, even though different in value, is concordant to $V_{os}^{(A)}$, given that the two inner probes share the same active region. Thus, it is expected that the main source of offset is the same in both the inner probes.

The X-Hall architecture is completed by a cross-connection of the sense contacts along with the diagonal directions (i.e., 1 with 3 and 2 with 4) forcing the electrical equality

$$V_A = -V_B = V_{probe}. \tag{3}$$

Under the hypothesis of concordant offset voltages and substituting (1) and (2) into (3), the only possible solution to (3) implies the equality

$$V_{OS}^{(A)} = V_{OS}^{(B)} = 0. \tag{4}$$

From a physical perspective, the cross short circuits add a boundary condition to the net charge distribution, which forces the minimization of the offset contributions to voltages V_A and V_B. More precisely, if the physical origin and sign of the offset are rigorously the same for both the elementary probes, then the only value of offset that satisfies both the symmetry of the probe and the boundary condition imposed by the short circuits is zero. Actually, there will always be present uncorrelated local defects or asymmetries that lead to a residual offset voltage ΔV_{OS} that adds to the voltage $V_{probe} = V_A = -V_B$. TCAD simulations of the X-Hall probe with passive offset reduction were performed to test the idea over several physical sources of offset. Simulation results predicted an acceptable reduction of the inherent offset associated with the Hall probe over a large set of inhomogeneities and asymmetries (e.g. mask

misalignment, doping gradient, local defect), though less-effectively than a standard 4-phase spun Hall probe operated at low frequency.

The resistive bridge model of Fig. 3-a gives a straightforward understanding of the passive offset reduction provided by the X-Hall probe. By modeling each n-well segment between two contacts (either a biasing or a sensing contact) with a resistor, and applying the superposition theorem under the assumption of the same nominal currents applied to contacts B and T, then it is possible to rearrange the resistive bridge as shown in Fig. 3-b. This picture denotes a current-biased common-centroid scheme, in which any linear inhomogeneity created by a *global* effect (e.g., a resistive gradient or a doping gradient) is compensated at the output voltage V_{probe} between node 1 and node 4. The model also shows that any *local* defect or inhomogeneity that can be represented by a deviation of the resistance value of a single segment from the nominal value, as well as random variations, is not compensated and gives origin to the residual offset voltage ΔV_{OS}.

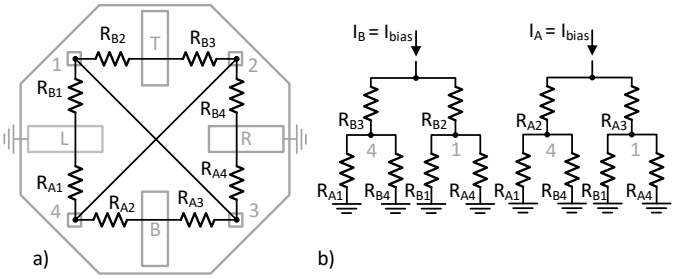

Fig. 3 (a) Resistive bridge model applied to the X-Hall probe. Each n-well segment is denoted by a single resistor. (b) Rearrangement of the resistive bridge model of the X-Hall probe to better highlight the common-centroid structure.

C. Bandwidth Enhancement

Papers [16] and [26] recognize four bandwidth limits in purely Hall-effect sensors (ordered by decreasing frequency): *i)* a *physical* limit around 1 GHz or above set by the relaxation time of the charge carriers [25]; *ii)* a *fundamental* limit set by the intrinsic capacitance due to the depletion region all over the n-well (see Fig. 1-a); *iii)* a *practical* limit set by the capacitive load added by the electronic circuits connected to the probe, as well as by the analog front-end dynamic performance, and *iv)* a *methodological* limit set by the spinning-current technique [27]–[29]. This last limit is a *soft* one because it represents the abrupt degradation of the effectiveness of the spinning-current technique in offset reduction when it is operated at high spinning frequencies.

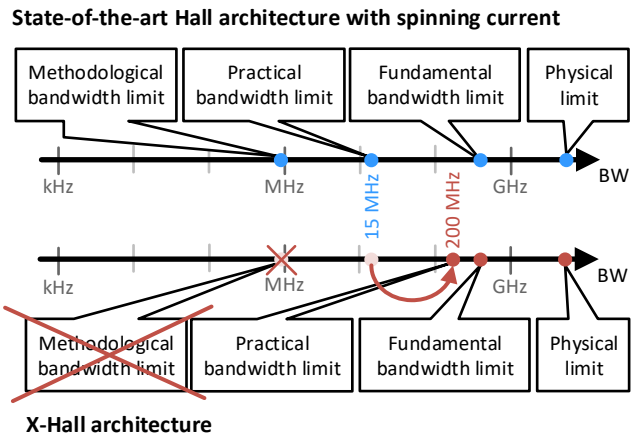

Fig. 4 Simplified diagram showing the positioning of the bandwidth limits for a state-of-the-art [16] spun Hall sensor and for the proposed X-Hall sensor. The picture highlights the possible bandwidth enhancement provided by the X-Hall architecture.

The X-Hall architecture removes the *methodological* bandwidth limit by replacing the dynamic/active spinning-current technique with the static/passive offset reduction technique described in the previous section. Moreover, removing the spinning-current technique also allows to considerably simplify the architecture of the electronic analog front-end (AFE), thus lowering the total capacitive load seen by the probe and pushing the *practical* bandwidth limit at higher frequencies (Fig. 4). According to this analysis, current sensors based on the X-Hall architecture could potentially achieve a bandwidth as high as hundreds of MHz, which is comparable to the hybrid coil-Hall architecture implemented in commercial current probes for laboratory instruments [30], provided that the AFE has sufficient bandwidth. Indeed, in the X-Hall architecture, the AFE becomes a very important element that could limit the global acquisition bandwidth because it is hard to design accurate broadband differential amplifiers.

D. Differential-Difference Current Feedback Amplifier

To completely exploit the improved practical bandwidth limit of the X-Hall probe, the AFE should be carefully designed. The X-Hall probe requires differential voltage amplifier with the following characteristics as readout circuit: *i)* high-input impedance (megaohms) to absorb theoretically zero current from the Hall-effect sensor; *ii)* high closed-loop voltage gain since the Hall voltage is typically in the order of tens to hundreds of microvolts; *iii)* low residual offset voltage (smaller than a few microvolts). Moreover, the voltage amplifier must also exhibit minimized input capacitive load and high gain-bandwidth product (GBW) to fully exploit the bandwidth capabilities of the X-Hall architecture.

For a voltage-feedback amplifier (VFA), a GBW greater than 1 GHz is required to get a bandwidth of about 20 MHz together with a closed-loop gain of 50. Such GBW is extremely challenging to achieve in power-CMOS technologies like the BCD. Note that the technology is chosen by the final application (e.g., switched power converters, motor drivers, OCD in power electronics), and cannot be defined by the current sensor. On the contrary, current-feedback amplifier

(CFA) inherently offers wider bandwidth since it does not follow the constant GBW rule of VFA. A simplified scheme of a general CFA is reported in Fig. 5-a, where the three main elements of a CFA are highlighted: the input buffer, the gain stage, and the output buffer [31]. Fig. 5-a clearly shows that the negative input of a CFA is a low-impedance node, which moves the associated pole to high frequencies, allowing wide bandwidth operation.

In order to amplify the differential output voltage V_{probe} of the Hall sensor without sinking an appreciable current from the Hall probe, the CFA architecture is extended by replacing the single-ended buffer with a differential-difference buffer [32] to realize a current-feedback differential-difference amplifier (DDCFA). The block diagram of the proposed DDCFA is reported in Fig. 5-b. In the DDCFA architecture, the output of the Hall probe is directly connected to the gate nodes of a differential coupled pair, nulling the absorbed DC current from the probe and minimizing the capacitive load to the gate capacitances of the differential pair. The exact sizing of the transistors used in the differential pair is set by the trade-off between input capacitance and Flicker noise [16].

The drawbacks of the CFA are higher offset and higher power consumption with respect to the VFA architecture. For our specific purposes, power consumption is not a major issue while offset is mitigated by designing the stages of the CFA architecture as highly symmetric, cascoded-output, single-stage, operational-transconductance amplifiers (OTA) in unity gain feedback. Moreover, the cascaded-stages-based architecture of Fig. 5-b is prone to stability issues. To cope with those, it is important to design the DDCFA for a single gain value, integrate the feedback resistive network in silicon, and takes into account all the parasitic elements by means of post-layout simulations, as well as assess process variations by means of corner analysis. In this way, the resistive and capacitive loads of the DDCFA are well defined and the stability of the DDCFA is assured. Finally, the differential-difference amplifier (DDA) structure allows to implement offset nulling strategies at the circuital level. For instance, it is possible to implement an automatic offset reduction loop (ORL) that nulls the differential offset of the DDCFA, similarly to what proposed in [33]. However, in the realized prototype, the automatic ORL is not implemented and the auxiliary voltage input V_{adj} is generated by an external variable reference voltage source that is manually trimmed to null the offset at the output of the DDCFA.

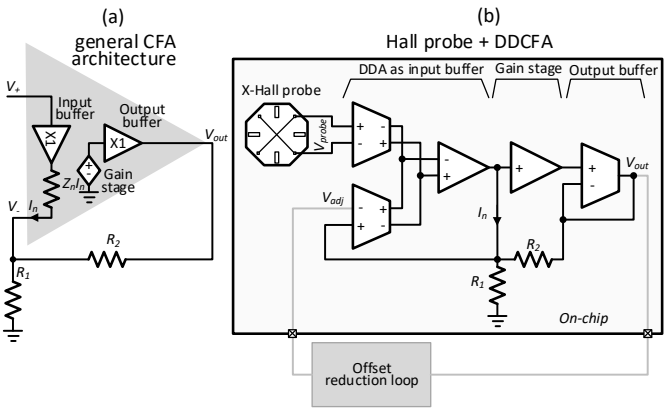

Fig. 5 (a) A simplified scheme of the general CFA architecture denoting the three main components (input buffer, gain stage, and output buffer) and the feedback in the current domain. (b) Schematic diagram of the proposed DDCFA denoting the implementation of the input buffer by using a DDA, instead of a single-ended buffer, and how the DDCFA is connected to the X-Hall probe. The picture also shows how an offset reduction loop could be connected.

III. Prototype Description

The X-Hall probe is inherently sensitive to the component B_Z of the magnetic field that is orthogonal to the probe plane. To realize a current sensor, the X-Hall probe is placed beneath a copper strip in which the current to be sensed flows (Fig. 6-a). This architecture can be easily implemented in silicon technology, allowing the integration of the sensor with the power circuits into the same silicon chip.

A prototype was implemented in 0.16-µm BCD technology provided by STMicroelctronics. The overall silicon die is 4-mm^2 sized, but most of the space is used either for replica circuits, or it is kept void for ensuring electrical isolation between sub-blocks of the sensor systems in this very first prototype. Looking at Fig. 6-b, a single X-Hall current sensor could potentially occupy an area of only 1 mm^2, or smaller. The copper strip is implemented at the top metal level to exploit the lowest resistivity of the copper redistribution layer. Width of the metal strip and area of the X-Hall probe are chosen to maximize the SNR of the sensor and allow for a maximum DC current of 20 A on the metal strip. This optimization was carried out by combining 3D Finite Element Method (FEM) simulations of the magnetic field generated by the input current I_{IN} at different strip widths with TCAD simulations of the X-Hall probe at different probe dimensions. Given the exact geometry and technology of this implementation, the current-to-magnetic field transduction factor G_{IB} was estimated to be 2 mT/A by means of FEM simulations in COMSOL®. All the transistors in the DDCFA are sized to set the bandwidth around 65 MHz and minimize the total input-referred noise power, accounting for both Flicker noise and thermal noise. Low-frequency noise due to the X-Hall probe is accounted for by exploiting an empirical, equivalent circuit-based model provided by the foundry, which takes into account both flicker-like noise for the specific BCD technology and conventional thermal noise floor.

The bandwidth of the AFE is of primary concern for the X-Hall current sensor since the X-Hall approach moved the probe-related bandwidth limits to very-high frequencies. Thus, the

bandwidth of the realized X-Hall current sensor will be limited by the AFE to 65 MHz. The DDCFA is optimized to work with a closed-loop gain of 35 dB given by the resistive feedback with R_1 = 50 Ω and R_2 = 2.5 kΩ, which are implemented on-silicon by using metal resistors. An output stage with the gain set to 2 is placed after the DDCFA to cope with external loads up to 10 pF and to show a constant and well-defined capacitive load to the DDCFA. The chip prototype is supplied at 5 V and consumes a total of 5 mA. The chip is encapsulated in a power small outline (PWSSO) package with exposed thermal pad that allows easy testing and suitable thermal dissipation.

Different test boards were developed targeting different characterizations. A first test board was specifically designed to characterize the static performance of the X-Hall with high current levels. A second test board was designed to statistically test the residual offset over a large number of samples by exploiting a spring socket for the chip. A final test board was designed to minimize the dynamic parasitics at the board level and allow accurate characterization of the dynamic performance of the X-Hall prototype.

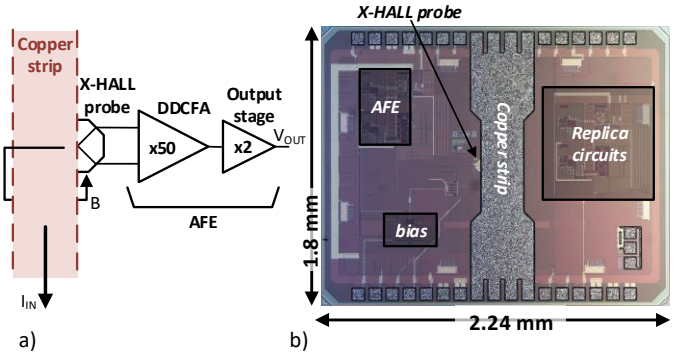

Fig. 6 (a) Block scheme of the implemented X-Hall current sensor. (b) Microphotograph of the X-Hall chip prototype.

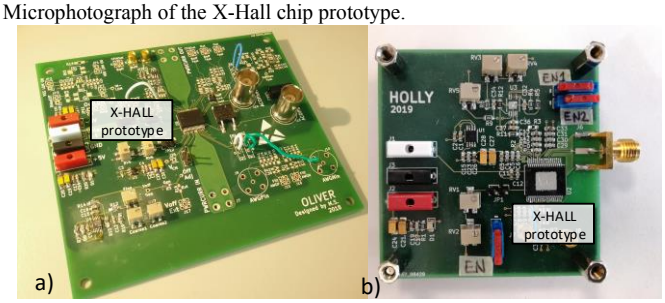

Fig. 7 (a) Test board for static characterization. (b) Test board for dynamic characterization.

IV. Static Characterization

The measurement setups for static characterization are shown in Fig. 8. The first setup (Fig.8-a) is used to characterize the response of the prototype to a static input. A Keysight E3633A power supply is connected to the copper metal strip through a 1-Ω 50-W resistor in order to generate an input current that is measured by a reference 6½-digit Keysight 34401 DMM. The power supply is programmed to generate pulsed currents (T_{ON} = 600 ms, duty cycle = 1 %) to avoid excessive heating of the sensor (measured overheating under 5 °C at the package surface), since the realized prototype is not provided with a temperature compensation circuit (which is a standard solution, and would not add value to the scope of this manuscript). The voltage V_{OUT} at the output of the amplifier is recorded by the Keysight 3458-A DMM.

The second measurement setup (Fig. 8-b) is implemented for offset characterization. The sensor is mounted on a spring socket for statistical testing on all the realized samples. A two-channel 2602B source-measurement-unit (SMU) is used to bias the Hall probe with two nominally equal currents $I_A = I_B = I_{bias}$ and known value. The differential voltage V_{probe} at the output of the Hall probe is directly measured by using a reference 8½-digit Keysight 3458-A digital multimeter (DMM) set at the minimum range of 100 mV, with a rated uncertainty of 0.7 μV. In this way, non-idealities and offset of the integrated amplifier are removed from the measurement. The sensor prototype is placed inside a thermostatic chamber for thermal control. No current flows through the copper metal strip, thus the output voltage of the probe can be modeled as

$$V_{probe} = \Delta V_{OS} + S_I I_{bias} B_{earth}, \tag{5}$$

where S_I is the current-related sensitivity of the X-Hall probe and B_{earth} is the earth magnetic field estimated according to the International Geomagnetic Reference Field (IGRF) model. From (5), the residual offset ΔV_{OS} of the X-Hall probe can be estimated by directly measuring the output voltage of the probe and subtracting the estimated effect of the earth magnetic field.

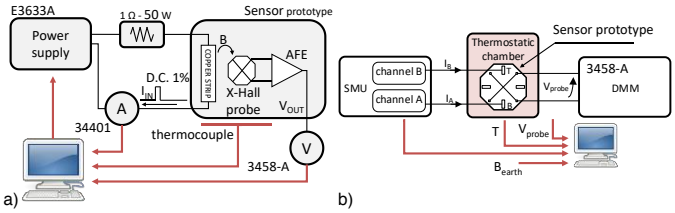

Fig. 8 Measurement setups for (a) static characterization and (b) residual offset assessment of the X-Hall sensor prototype.

A. Gain and Non-linearity

The static characteristic over the ±10 A (±20 mT) input range is measured for two bias currents, I_{bias} = 0.9 mA and I_{bias} = 0.5 mA, and is reported in Fig. 9-left. The total estimated DC sensitivity G_0 is 36 mV/A and 23 mV/A, respectively. These sensitivity values take into account the current-to-magnetic field transduction G_{IB}, the sensitivity of the Hall probe G_H, and the gain of the electronic amplifier G_{ELE}:

$$G_0 = G_{IB} \cdot G_H \cdot G_{ELE}. \tag{6}$$

By assuming G_{IB} = 2 mT/A and G_{ELE} = 100 V/V, which are the nominal values provided by simulation, the sensitivity of the Hall probe is 180 mV/T for I_{bias} = 0.9 mA and 115 mV/T for I_{bias} = 0.5 mA, corresponding to a current-related sensitivity

$$S_I = \frac{G_H}{I_{bias}} \tag{7}$$

in the range 200 – 230 V/AT, which is in agreement with the

state of the art [14]–[16] and the design target. The nonlinearity error (Fig. 9-right) is computed over the tested ±10-A FS range and showed to be less than 2 %FS range for both the sensitivity values, which is in agreement with state-of-the-art Hall sensors. The ±10-A limit of the full-scale range is given only by the limited capability of the test setup, while the X-Hall prototype can work up to very high magnetic fields and the sensor prototype is designed to handle up to 20 A.

B. *Residual Offset*

The measurement procedure of Fig.8-b is repeated over all the 75 samples available with I_{bias} = 0.5 mA and a controlled temperature of 25(1) °C. The results of the statistical measurements are reported in Fig. 10-a. Note that the estimated statistical moments are independent of the acquisition bandwidth since no dynamic offset compensation is implemented. The mean residual offset is -65(13) µV with a standard deviation of 738 µV over the entire sample population. This value corresponds to a mean input-referred offset of -0.56(11) mT with a standard deviation of 6 mT. The mean residual offset of the X-Hall prototype is thus comparable to state-of-the-art Hall sensors employing the spinning-current technique [9], [14], [17], [27], but the statistical dispersion of the offset in the X-Hall probe is one order of magnitude higher. This deterioration of the statistical dispersion of the offset was easily foreseen since the static offset reduction of the X-Hall sensor is more prone to technological and fabrication aspects.

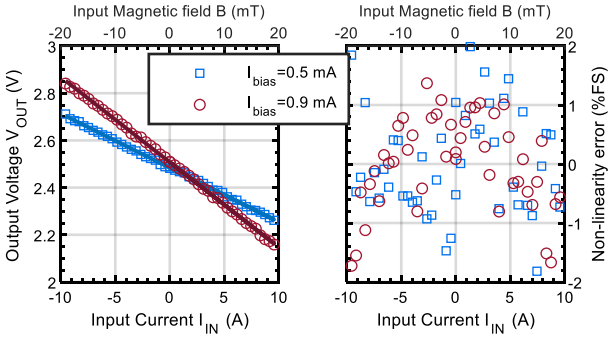

Fig. 9 (left) Static characteristic of the X-Hall sensor prototype for two bias currents showing a sensitivity of 23 mV/A (I_{bias} = 0.5 mA) and 36 mV/A (I_{bias} = 0.9 mA). (right) Non-linearity error expressed in percent of the ±10-A full-scale range.

To correctly assess the performance of the X-Hall sensor in terms of residual offset, it must be compared to a spun Hall-effect sensor realized in the same silicon technology (Fig. 10-b). In [16], a spinning-current-operated Hall-effect sensor implemented in the same BCD technology was presented and characterized. It showed a mean input-referred offset that ranged between 0.35 mT (when operated at low spinning frequencies) and 17 mT (when operated at frequencies higher than 1 MHz). The X-Hall sensor prototype shows a higher offset if compared to [16] when the latter is operated at low frequencies, but it features much lower offset if compared to [16] when operated at high frequencies. In summary, the X-Hall architecture offers an intermediate-effective but strongly frequency-independent offset reduction, allowing for wider acquisition bandwidth while preserving basically the same offset rejection capability. Thus, the X-Hall sensor is an interesting solution when the final application requires high operating frequencies, yet still featuring an acceptably low offset.

C. *Offset Dispersion*

Short- and long-term stability of the offset is even more important than the nominal offset value since one-point correction is easily implementable. To assess the long-term stability of the residual offset, a single chip prototype is placed inside a thermostatic chamber (Fig. 8-b) with temperature set to 27(1)° C and constantly biased and monitored for four days, with sampling time of 10 minutes. The thermostatic chamber is pre-set to the nominal temperature, then it is turned off during the test for better accuracy. Indeed, thermostatic chambers use an air compressor unit to stabilize the temperature that introduces strong vibrations creating electrical noise and interferences. However, the side-effect of this approach is to worsen the temperature stability of the measurement that is in the order of 1° C.

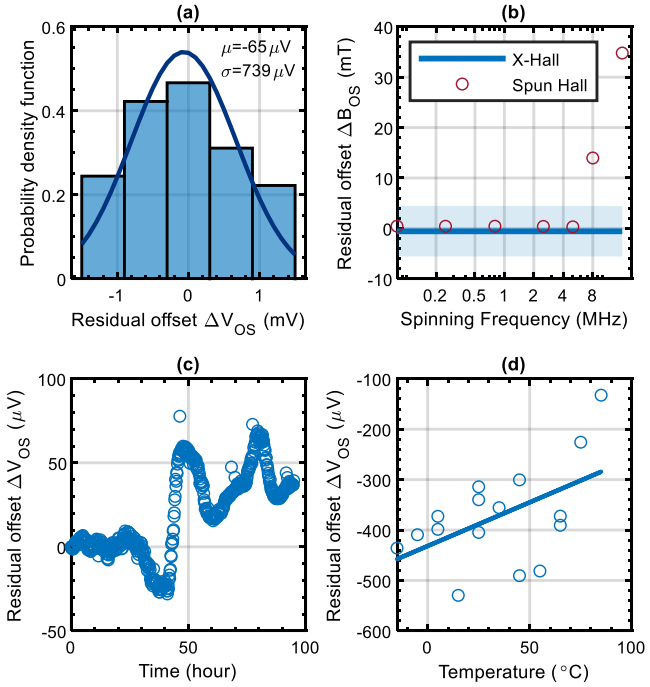

Fig. 10 (a) Statistical distribution of the residual offset ΔV_{OS} measured at the output of the X-Hall probe over 75 samples and corresponding gaussian probability density function. (b) Comparison of the residual offset of the X-Hall sensor with the offset of the spun Hall sensor reported in [16] as a function of the spinning frequency, which is related to the bandwidth. (c) Time dispersion of the residual offset ΔV_{OS} of the X-Hall sensor over 4 days. (d) Temperature dispersion of the residual offset ΔV_{OS} of a randomly chosen sample.

The recorded time dispersion of the offset voltage is reported in Fig. 10-c, showing a time-dispersion of the residual offset, with respect to the starting value, of ±50(9) µV, which corresponds to ±200(36) µT. This result is higher than what reported in the conference paper [23] because the measurement time was extended to four days. However, it is still a fairly good result, making one-point calibration an effective technique to cope with the large statistical dispersion of the offset.

Fig.10-d reports the short-term dispersion of a randomly selected chip prototype in the -15° C +85° C temperature range. The temperature was swept in both directions (heating and cooling) without revealing a noticeable hysteretic behavior. Linear interpolation of the recorded data leads to an absolute temperature coefficient of 2 µV/°C, corresponding to 11 µT/°C or 5.5 mA/°C, and a relative temperature coefficient of 0.7%/°C. The absolute temperature coefficient is considerably higher compared to the literature (i.e., spun Hall sensors) because the residual offset of the tested sample is higher. On the contrary, the state-of-the-art spun Hall sensor achieves a relative temperature coefficient of 0.4%/°C [17], which is comparable to the X-Hall performance.

V. Dynamic Characterization and Validation

A. Transfer Function

The current-voltage transfer function (TF) of the prototype is estimated by applying a 200-mA-amplitude sinewave at known frequencies to a 50-Ω resistor connected in series to the copper metal strip on the top of the metal stack inside the silicon chip. The chip prototype is soldered on the test board specifically designed for dynamic testing (Fig.7-b). The excitation sinewaves are generated by the Keysight 81150A arbitrary function generator (AFG) and monitored by the 100-MHz bandwidth N2783A current probe connected to the Keysight DSO9254A oscilloscope. The output of the X-Hall sensor (i.e., the voltage V_{OUT} at the amplifier output) is synchronously acquired by the same oscilloscope by adjusting the sampling rate to acquire a sufficient number of samples per period for all the frequency points. Coherent averaging over multiple acquisitions is performed to improve the final resolution of the test. Finally, TF computation is performed in MATLAB. The measurement setup excites the sensor with approximately 10 frequency points per decade from 1 kHz to 20 MHz (note that the test is not extended up to the 65-MHz bandwidth of the AFE for the reasons discussed below).

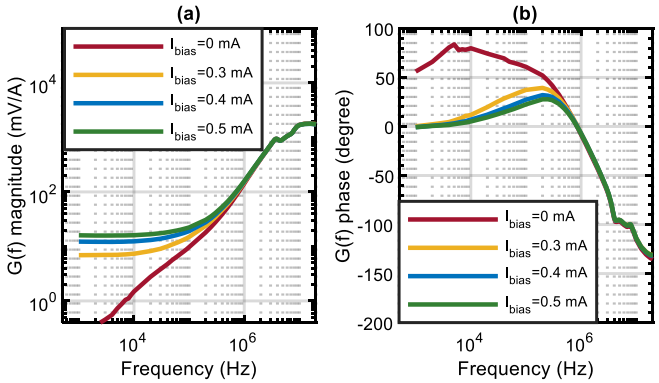

Fig. 11 TF of the X-Hall sensor prototype estimated for different bias currents: (a) magnitude and (b) phase.

Fig. 11 shows the estimated complex TF *G(f)* for different bias current levels. The absolute value of the low-frequency gain is slightly different from the one reported in Section III since the two measured values belong to two different prototype samples. Increasing the bias current boosts the low-frequency gain, as also expected from static characterization. At higher frequencies, the TF rises by about 20 dB/decade due to the presence of additive perturbative effects, which are not related to the X-Hall architecture but depend on the specific implementation of the prototype (see the discussion in Section V-B). To prove this statement, the same measurement procedure is repeated with no bias current flowing through the Hall probe, thus nulling the Hall voltage and the sensor offset. The result of this measurement is shown by the dark-red line in Fig. 11, which still presents the parasitic behavior at frequencies higher than 200 kHz. As a result, the output of the realized X-Hall prototype can be modeled as:

$$V_{OUT}(f) = G(f) \cdot I_{IN}(f) = G_0 \cdot I_{IN}(f) + \Delta V(f), \qquad (8)$$

where $\Delta V(f)$ represents the dynamic perturbation, and the ideal response of the X-Hall sensor is assumed purely algebraic in the tested 0-20 MHz frequency band.

Regardless of the physical origin of the additive perturbative effect, but only assuming linearity with respect to the input current (i.e., $\Delta V(f) \cong \tilde{G}(f) I_{IN}(f)$), it is possible to online compensate for it by implementing a post de-emphasis digital filter whose TF *H(f)* is given by

$$H(f) = \frac{G_0}{G_0 + \tilde{G}(f)} \qquad (9)$$

which allows to obtain the real-time response of the compensated X-Hall sensor $G'(f) = G(f) \cdot H(f) \cong G_0$. The post de-emphasis filter is implemented as a low-pass filter, whose TF is computed by interpolating the experimental estimation of eq. (9) up to 20 MHz. Fig. 12 reports the TF of the post de-emphasis filter and the X-Hall sensor frequency response, both before and after application of the post de-emphasis. From this figure, it is possible to appreciate an acquisition bandwidth of the prototype, defined as a 3-dB deviation from the flatness, of about 4 MHz. To the best knowledge of the authors, 4-MHz bandwidth is the broadest bandwidth ever achieved by a purely Hall-effect based sensor, although still far from the results demonstrated by TCAD physical simulation of the X-Hall probe, which define the practical bandwidth limit.

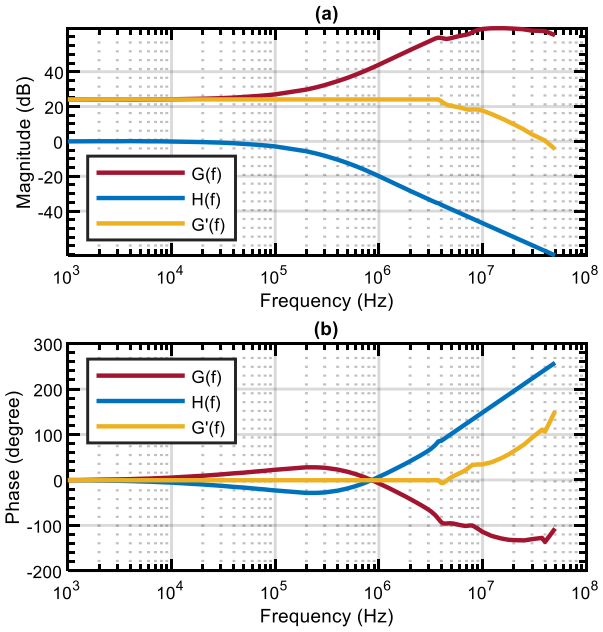

Fig. 12 Measured TF of the X-Hall prototype before de-emphasis (G(f)) and after de-emphasis (G'(f)), and implemented TF of the de-emphasis filter (H(f)). (a) Magnitude and (b) phase responses.

Fig. 13 reports the simulated dynamic response of the X-Hall probe to a 50-mT step of the input magnetic field at $t = 0$ s. The simulation takes into account a bias current of 500 µA and aims to define the practical bandwidth limit of the probe by considering an equivalent input capacitance of the electronic amplifier of 500 fF. The simulation was realized by using Sentaurus TCAD with the model described in [20], [24] and shows a practical bandwidth limit of about 200 MHz. According to the simulation result, the X-Hall sensor could ideally achieve a bandwidth higher than 200 MHz if *i)* the dynamic perturbations are made negligible by improving/optimizing the technology of the prototype package, *ii)* the capacitance of the amplifier is minimized to 500 fF or less, and *iii)* the bandwidth of the AFE is made compatible with the frequency response of the X-Hall prove. Given the bandwidth and input capacitance of the implemented DDCFA, a 65-MHz bandwidth of the X-Hall sensor could be achieved in a future version of the prototype by solving issue *i)* only.

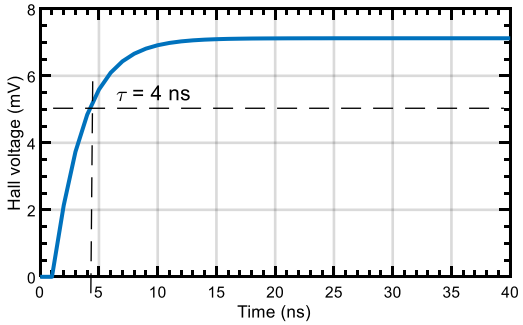

Fig. 13 TCAD simulation result of the theoretical response of the X-Hall sensor to a 50-mT step of the magnetic field. The X-Hall probe is biased by a 500 µA and a 500 fF capacitor is connected to the output to simulate the loading effect of the amplifier. The simulation shows a practical bandwidth limit higher than 200 MHz for the X-Hall probe.

B. Investigation on the Dynamic Perturbation

The physical origin of the dynamic parasitic effect could be ascribed to a linear inductive coupling at the package level between the input current signal and other input/output signals (e.g., the output voltage V_{OUT} or auxiliary input V_{adj}), or supply voltages (e.g., V_{DD}), or ground nodes. Inductive coupling at package level is a well-known problem in RF integrated circuits, where the input/output signals are in the hundreds of MHz and beyond, and they are characterized by very high dI/dt values. Even though the frequencies of interest for the X-Hall sensor are lower than RF applications, the target input current I_{IN} of the X-Hall sensor is characterized by high dI/dt values because of the large amplitudes typical of power circuits, making the inductive coupling at package level a critical problem.

To numerically assess these assumptions, self-inductance and mutual-inductance between adjacent pins were added in the CAD model of the X-Hall chip prototype. The values of these parasitic elements were estimated by using typical arc models for the bonding wires and assuming the effect of the lead frame and other package elements to be negligible. We considered a constant self-inductance of 3 nH for all the bond wires and

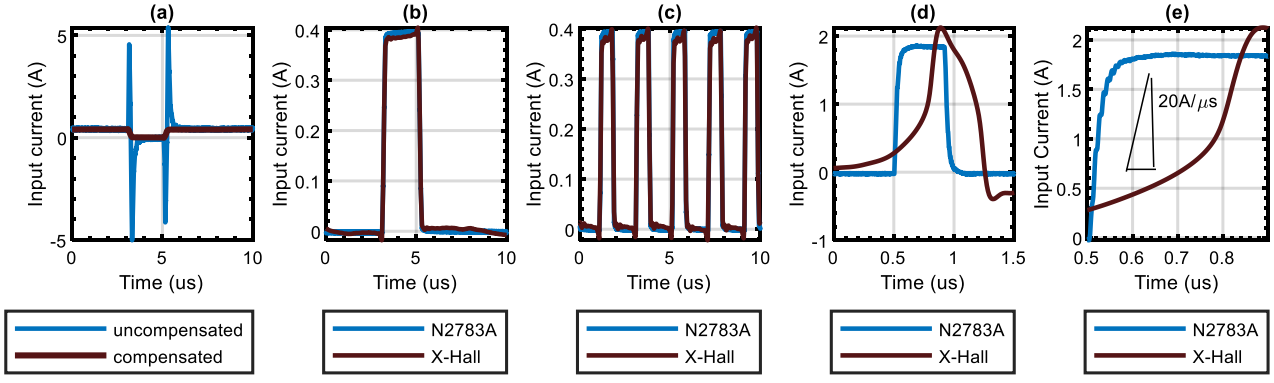

Fig. 14 Results of validation tests. (a) Comparison between compensated and uncompensated output of the X-Hall sensor in the monitoring of a square pulse. (b) Comparison of the compensated X-Hall output with a commercial current probe in the monitoring of a 100-kHz, 400-mApp, current square wave with DC 20% and 125 ns trail edges, typical of VFR application. (c) Comparison of the compensated X-Hall output with a commercial current probe in the monitoring of a 500-kHz, 400-mApp, current square wave with DC 30% and 50 ns trail edges, typical of VFR application. (d) Comparison of the compensated X-Hall output with a commercial current probe in the monitoring of a 1.8-A current pulse. (e) Rising edge detail of the 1.8-A current pulse.

Table 1 Summary of reported X-Hall performance.

	GAIN				OFFSET				BANDWIDTH		
Input range FS	Current-to-field G_{IB}	AFE G_{ELE}	Hall probe G_H 0.5 mA bias	Nonlin. error	Mean value	Time dispersion over 100 hours	Temp. dispersion [-15°,85°] C	Relative temp. coeff.	AFE sim.	X-Hall Probe sim.	X-Hall sensor meas.
10 A	2 mT/A	100	115 mV/T	<2% FS	0.56 mT 280 mA	0.2 mT 100 mA	11 µT/°C 5.5 mA/°C	0.7 %/°C	65 MHz	200 MHz	4 MHz

mutual inductance of 1.5 nH only between adjacent bond wires. The simulation took into account also all the RC layout-extracted parasitics at the chip level. Fig. 14 compares the result of the simulation with the measured TF, validating the hypothesized origin of the dynamic parasitic. Further tests based on more accurate models of the package will be carried out to fully verify the relationship between the package and inductive coupling, so that novel packages will be investigated to further enlarge the bandwidth of the X-Hall architecture up to the AFE limit. To fully exploit the bandwidth potentiality of the X-Hall architecture, not only dynamic parasitics must be removed, but faster AFE needs to be developed since the current AFE has a bandwidth of 65 MHz.

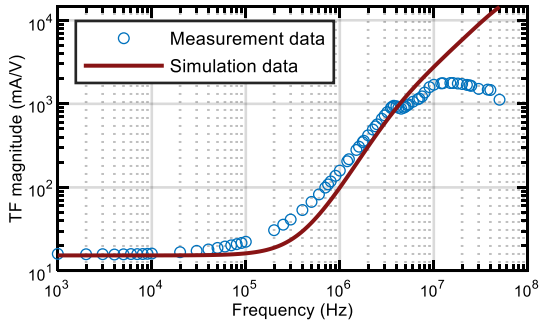

Fig. 15 Comparison of the TF G(f) between measurement results and post-layout SPICE simulation taking into consideration also the parasitics of the bond wires by using standard RLC+L models.

C. *Validation*

The X-Hall prototype is validated in two different case studies reproducing the requirements typical of power applications with fast events. The first case study targets the very fast change of the load current in a VFR DC-DC buck converter [4]. To this aim, the Keysight 81150A AFG is used to create two different square wave currents of 400 mApp with frequency of 100 kHz, duty cycle 20% and trail edges of 125 ns, in the first case, and frequency of 500 kHz, duty cycle 30% and trail edges of 50 ns, in the second case. The results of the validation test are reported in Fig. 15. The first chart (Fig.15-a) compares the output of the X-Hall sensor before (blue line) and after (dark red line) the de-emphasis filter. As expected, the dynamic parasitic effects originate high spikes in correspondence to the edges of the input signal, which are well compensated for by the de-emphasis filter. The second chart (Fig.15-b) and the third chart (Fig.15-c) report the results of the VFR test for the 100-kHz and 500-kHz stimulus, respectively. In both cases, the estimated input current of the X-Hall sensor prototype is compared to the commercial N2783A current probe, showing a very good agreement, and demonstrating the potentiality of the X-Hall probe in VFR applications.

The second case study aims at replicating the more demanding over-current protection (OCP) application. OCP usually requires the detection of sporadic current spikes with very high current derivatives in the order of tens to hundreds of A/µs. The current sensor system should be able to detect such fast spikes with a short delay. To implement the current spikes, a half-bridge architecture employing GaN power transistors from EPC is exploited (dev. Board EPC9001). The output of the EPC board is connected to a 12-Ω resistive load in series with the X-Hall prototype to generate and detect current square waves. The EPC board is able to generate currents up to 15 A with a trailing edge as low as a few ns. In this test, a 1.8-A, 500-ns current pulse is generated with edge-time limited to approximately 20 ns, corresponding to an edge slope of 90 A/µs. The current spike estimated by the X-Hall sensor is shown in Fig. 15-d. The generated one is a very steep current spike characterized by a bandwidth well above the 4-MHz cut-off of the prototype. Therefore, the post-emphasis filter is not able to completely correct the X-Hall response. Nonetheless, the X-Hall demonstrates to be able to detect such challenging spike. In this context, it is worth noticing that even the commercial probe is not able to follow the time derivative of the current pulse. Fig.15-e reports a detail of the rising edge of the current pulse estimated by using both the X-Hall sensor and the commercial current probe, showing an estimated slope of roughly 20 A/µs and 40 A/µs, respectively, which are considerably lower than the nominal value of 90 A/µs. Fig. 15-d also shows that the X-Hall prototype detects the overcurrent spike within a 400-ns delay, which is sufficiently small to allow shutting-down the power circuits before any damage could happen.

VI. Conclusions

This paper presented the X-Hall sensor as a viable architectural solution for developing broadband current/magnetic sensors integrated into silicon technology together with the power electronic circuits to be monitored. The paper experimentally characterized and validated the architecture by testing a prototype implemented in BCD technology.

The X-Hall sensor overcomes the bandwidth limit of state-of-the-art Hall sensors by replacing the spinning-current technique with a DC-bias-basing and a passive offset

compensation. At low/medium-frequency input regimes (hundreds of kHz), the X-Hall sensor is less effective than spun Hall sensors in offset compensation, but the passive compensation preserves an adequate offset reduction performance at high frequencies, thus it does not limit the acquisition bandwidth. In other words, the elimination of the spinning-current technique removes the methodological bandwidth limit and pushes the practical limit close to the fundamental one. In this way, the X-Hall probe could theoretically achieve a bandwidth as high as 200 MHz, as demonstrated by means of TCAD simulation. However, the tests on the X-Hall prototype identified the presence of a parasitic dynamic perturbation that prevents from fully exploiting the X-Hall prototype up to its designed bandwidth limit, which was set to 65 MHz by the capabilities of the implemented AFE. The dynamic perturbation is not related to the X-Hall architecture nor inherent to this approach but can be ascribed to the inductive coupling at the package level, as demonstrated by CAD simulation. However, the implementation of a post de-emphasis digital filter allowed to partially compensate for the dynamic perturbation and to experimentally achieve a sensor bandwidth of 4 MHz, which is the broadest bandwidth ever demonstrated by a purely Hall-effect based sensor.

The present and future work are devoted to the design of a more refined package that will allow to remove the parasitic inductive effect and to achieve a bandwidth close to the 65-MHz limit set by the AFE. Moreover, refinements on the current AFE design will be developed to improve the frequency response of the DDCFA.

The mean residual offset of the X-Hall sensor is lower than the offset of high-frequency-operated spun Hall sensors, but higher with respect to low-frequency-operated ones. Moreover, the X-Hall sensor shows a low time dispersion of the residual offset, which allows to cope with the statistical dispersion of the offset by the simple one-point calibration procedure. All the discussed performance of the X-Hall sensor are summed up in Table 1.

Fig. 16 places the X-Hall sensor present performance in the framework of integrated current sensors and highlights the target achievable in the near future.

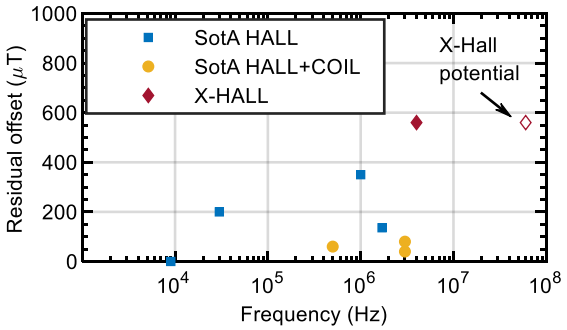

Fig. 16 Comparison of the X-Hall prototype with state-of-the-art integrated current sensors based on purely Hall effect with spinning-current technique (squares) and Hall + coil hybrid architectures (circles).

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