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Hot-Carrier Degradation in Power LDMOS: Drain Bias Dependence and Lifetime Evaluation

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***Abstract*—In this paper, we present an analysis of the degradation induced by hot-carrier stress in new generation power LDMOS transistors. When a relatively high drain voltage is applied during the on-state regime, high energetic and/or multiple cold electrons are recognized as the main source of degradation affecting the LDMOS lifetime: the latter is usually extrapolated at typical operating drain voltages. Hence, the extrapolation criterion is particularly critical and different models have been proposed in the past and discussed in this letter. In particular, the dependence of on-resistance degradation (ΔR_{ON}) on drain bias is investigated and a simplified extrapolation model, accounting for the saturation effects of the ΔR_{ON} at long stress times, is proposed and validated by comparison with experiments and advanced physics-based TCAD simulations, confirming the ability to accurately estimate lifetime on devices featuring short-circuited source-body contacts.**

***Index Terms*— Hot-carrier stress, on-resistance degradation, LDMOS transistor, lifetime evaluation, TCAD simulation.**

I. Introduction

Lateral double-diffused MOSFET (LDMOSFET) is widely adopted for medium voltage and smart power applications due to its low on-resistance (R_{ON}) [1, 2] and its compatibility with standard CMOS process [3, 4].

LDMOS transistors are particularly vulnerable to hot-carrier degradation caused by high electric fields leading to the generation of interface traps in the proximity of the Si/SiO_2 interface within the drift region [5]. This causes the shift of the electrical parameters (e.g., R_{ON}) limiting the device lifetime [6].

Since device lifetimes up to 10, 10 years are required in smart-power applications, accelerated stress tests and extrapolation approaches have been implemented in order to access device reliability in reasonable times [7-12].

Hu et al. [7] proposed a model where the time-dependent hot-carrier degradation in MOSFETs follows a simple power-law, whereas in [8] it was shown that the degradation follows a logarithmic time-dependence at longer times. In [9], the model by Goo [10] is enhanced by using a high-resolution measurement technique and non-linear least-square fit of the experimental degradation curves. A similar model has been implemented in the case of power LDMOS transistors [11, 12]. In particular, the model takes into account the self-limiting (saturation) behavior of the degradation. However, all the previous models are based on an acceleration factor (ξ), representing the fraction of hot carriers possessing enough energy to break bonds at the Si/SiO_2 interface. Since the source and body currents need to be separately measured to calculate ξ, such models cannot be applied to the LDMOS architectures featuring shorted source and body contacts to avoid the turn-on of the parasitic BJT between N-drift/P-body/N-source.

In this paper, the experimental R_{ON} degradation induced by hot-carrier stress (HCS) is reported as a function of drain voltage. The model proposed in [9, 11, 12] is modified for application to LDMOS with shorted source-body contacts. Finally, the results of a simple time-power-law and of the simplified self-limiting degradation model are compared, and TCAD simulations aimed at validating the applicability of the model to LDMOSFETs are performed for extremely long stress times.

II. Results And Discussion

N-channel STI-based power LDMOS transistors with an operating drain voltage of 18 V, fabricated on 200mm silicon wafers by STMicroelectronics, are considered in this work. Fig. 1 shows a sketch of the drift region, where the major contribution to degradation during hot-carrier stress is localized [13]. Accelerated stress tests have been carried out for V_{GS} = 1.9 V, representing the worst case of HCS, as shown by the simulated body-current peak [13]. In order to preliminary identify possible issues related to process variability, devices with very similar I_DV_G transfer characteristics have been selected within the wafer and then stressed. The maximum relative deviation for measured ΔR_{ON} due to dispersion was less than 0.7% while stressing four selected devices for the same stress bias.

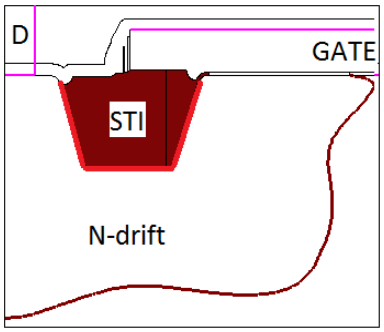

Fig. 1. Sketch of the N-drift region of the STI-based LDMOS transistor. The red line at the STI/N-drift interface is the region where interface trapped charge is monitored in Fig. 6.

This paragraph of the first footnote will contain the date on which you submitted your brief for review. It will also contain support information, including sponsor and financial support acknowledgment. For example, "This work was supported in part by the U.S. Department of Commerce under Grant BS123456."

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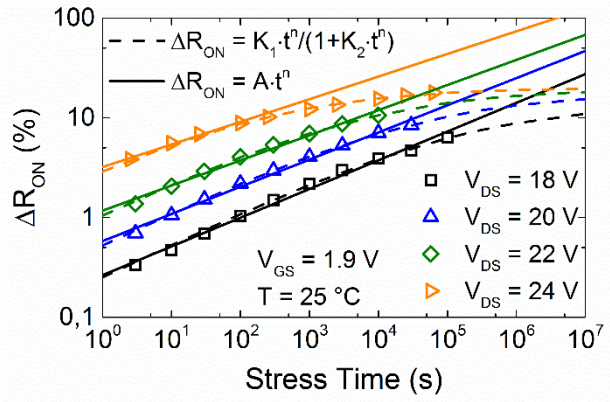

Fig. 2. Experimental (symbols) ΔRON vs stress time as a function of the drain voltage. Experimental data have been fitted with a simple power-law (solid line) and with the proposed model (dashed line).

Fig. 2 shows ΔRON vs stress time for different VDS, measured on-wafer by the constant voltage stress (CVS) technique. By monitoring ΔRON in linear regime, a saturation occurs at long stress times, particularly evident for VDS = 24 V. The limited increase of ΔRON at long stress times is typical of LDMOS devices, as they experience the saturation of the broken bonds at the STI corner, followed by a lateral extension of the degradation hot spot. This effect usually takes place for ΔRON well below the 10% variation. A simple time-power-law (solid line) nicely reproduces the early stage of HCS degradation, but overestimates ΔRON at long stress times inducing a relevant underestimation of the lifetime projection (Fig. 2).

A more exhaustive model able to account for the saturation behavior of ΔRON has been proposed over the years [9, 11, 12]:

$$\Delta R_{ON} = \frac{C_1(V_G)\cdot(\xi\cdot t)^{n(V_G)}}{1+C_2(V_G)\cdot(\xi\cdot t)^{n(V_G)}} \quad (1)$$

$$\xi(V_{GS},V_{DS}) = \frac{I_{source}(V_{GS},V_{DS})}{W}\cdot\left(\frac{I_{body}(V_{GS},V_{DS})}{I_{source}(V_{GS},V_{DS})}\right)^{\beta} \quad (2)$$

However, the model in this form, although its physical validity, cannot be applied without monitoring the body and source currents separately, as they are needed to calculate the acceleration factor (ξ) and its dependence on VGS and VDS. In order to overcome such limit, the model has been simplified according to:

$$\Delta R_{ON} = \frac{K_1(V_{GS},V_{DS})\cdot t^n}{1+K_2(V_{GS},V_{DS})\cdot t^n}. \quad (3)$$

with the two parameters K1(VGS,VDS) = C1·ξ^n and K2(VGS,VDS) = C2·ξ^n to be identified by fitting measurements.

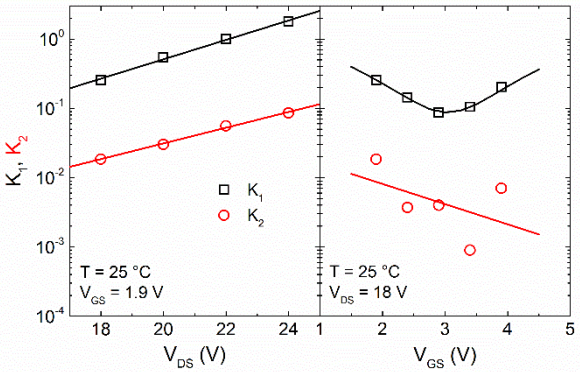

Fig. 3. Drain and gate bias dependent fitting constants K1 and K2.

The parameter n (fixed to 0.33 in our case) is the power slope determined by fitting the experimental ΔRON in a range where the saturation is not taking place, as in the case with the lowest VDS (18 V) at relatively short stress times (< 10^3 s).

Dashed lines in Fig. 2 report the result of the Eq. (3) showing a good agreement with the ΔRON. The fitting constants K1 and K2 are extracted for each stress condition and their dependence on VDS and VGS is shown in Fig. 3. The relationship is universal and can be used in all the cases, even with shorted body-source contacts.

The accuracy of the adopted extrapolation model has been validated against TCAD simulations. The solution of the full-band Boltzmann Transport Equation (BTE) implemented in [14] has been used to predict the energetic distribution of hot electrons. The physics-based degradation model proposed in [15] has been adopted, as it is specifically suited for the HCS in LDMOSs. More details about the model calibration and the physical mechanisms contributing to the de-passivation bonds at the Si/SiO2 interface can be found in [13, 16].

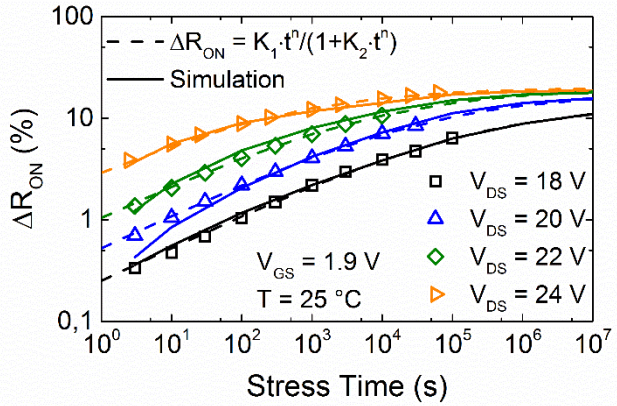

Fig. 4. Experimental data (symbols), TCAD simulated results (solid lines) and model fitting (dashed lines) of ΔRON vs stress time.

Fig. 4 shows the ΔRON reproduced with the proposed model (dashed line) and simulated with the TCAD tool [14] (solid line). Both simulation and equation (3) provide an accurate agreement with experimental data for all the considered stress conditions, and allow for an extension to longer stress times confirming the potential and the accuracy of the model, in spite of the simplification introduced (ξ = 1 independently of bias conditions).

Fig. 5 compares the lifetimes extrapolated from the experiments by using the different models and from the TCAD data. The corresponding lifetime extrapolations at lower drain biases are given by the conventional power-law (blue lines). By adopting as a failure criterion a ΔRON of 10% in 1000 hours, the maximum applicable drain voltage at room temperature and VGS = 1.9 V has been extrapolated to be 16.2 V for the simple power-law [7] and 18 V for the proposed model and TCAD simulations.

As expected from Figs. 2 and 4, the difference between the lifetime extrapolated with the simple power-law (Fig. 5, squares) and those extrapolated by the proposed model (Fig. 5, black circles) or by the TCAD simulations (Fig. 5, red circles), increases with the reduction of the applied stress bias, leading to a difference of about one order of magnitude at VDS = 18 V. As a result, an underestimated lifetime or maximum applicable voltage is obtained if the experimental ΔRON is fitted/reproduced by a simple time-power-law.

Finally, Fig. 6 shows the simulated interface traps generated and charged after a stress of 10^6 s along the STI interface (red line in Fig. 1) for the biases analyzed in Fig. 4. Independently of VDS, the

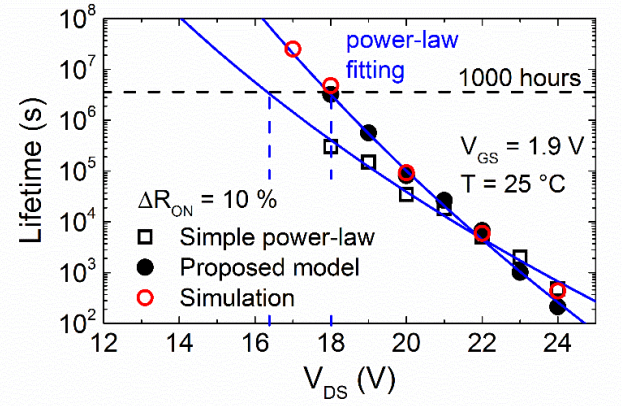

Fig. 5. The 10% of ΔR_{ON} is extrapolated from experiments by the simple power-law (squares), the proposed model (black circles) and the simulation results (red circles).

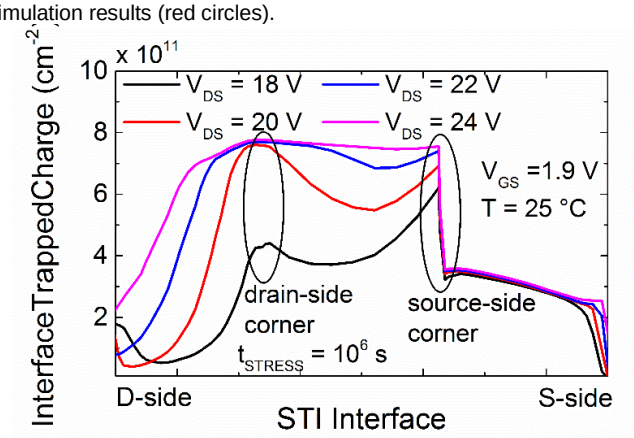

Fig. 6. Traps filled with electrons along the STI interface after 10^6 s of stress at V_{GS} = 1.9 V and different V_{DS}.

interface-trap generation shows a hot spot at the source-side corner, while a second peak at the drain side under the field-plate edge increases with larger V_{DS}. As detailed in [13], at V_{DS} = 18 V impact ionization takes place close to the source-side corner generating a hot spot, whereas by increasing V_{DS} the impact ionization peak increases but it expands toward the drain, intensifying the interface trap generation at the STI bottom and at the drain-side corner.

III. Conclusion

In this paper, we investigated the drain-bias dependence of the HCS degradation in a new generation STI LDMOS architecture. By monitoring the ΔR_{ON} during CVS tests, the saturation dynamics is shown, as expected, for long stress times. Previous models in the literature have been taken into account highlighting the respective weaknesses. On the one hand, by adopting a simple time-power-law the saturation effect of the ΔR_{ON} is not accounted for, leading to an overestimated degradation and to an underestimated device lifetime. On the other hand, the adoption of a more complex model [11, 12] is not possible when the body and source contacts are internally shorted as in the case of power LDMOSFETs, not allowing the calculation of the acceleration factor. As a consequence, we proposed a simplified model able to easily evaluate the long-term degradation and hence the device lifetime independent of the body current. Its applicability and accuracy have been proved by comparison with TCAD simulations.

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