Hot-carrier degradation in power LDMOS: Drain bias dependence and lifetime evaluation

15 October 2024

This is the post peer-review accepted manuscript of:

A. N. Tallarico *et al*. "Hot-Carrier Degradation in Power LDMOS: Drain Bias Dependence and Lifetime Evaluation" in *IEEE Transactions on Electron Devices*, vol. 65, no. 11, pp. 5195-5198, Nov. 2018.

The published version is available online at:

Hot-Carrier Degradation in Power LDMOS: Drain Bias Dependence and Lifetime Evaluation

Andrea Natale Tallarico, Susanna Reggiani, Riccardo Depetro, Stefano Manzini, Andrea Mario Torti, Giuseppe Croce, Enrico Sangiorgi, *Fellow, IEEE*, and Claudio Fiegna

Abstract—In this paper, we present an analysis of the degradation induced by hot-carrier stress in new generation power LDMOS transistors. When a relatively high drain voltage is applied during the on-state regime, high energetic and/or multiple cold electrons are recognized as the main source of degradation affecting the LDMOS lifetime: the latter is usually extrapolated at typical operating drain voltages. Hence, the extrapolation criterion is particularly critical and different models have been proposed in the past and discussed in this letter. In particular, the dependence of on-resistance degradation (ΔR_{ON}) on drain bias is investigated and a simplified extrapolation model, accounting for the saturation effects of the ΔR_{ON} at long stress times, is proposed and validated by comparison with experiments and advanced physics-based TCAD simulations, confirming the ability to accurately estimate lifetime on devices featuring short-circuited source-body contacts.

Index Terms— Hot-carrier stress, on-resistance degradation, LDMOS transistor, lifetime evaluation, TCAD simulation.

I. INTRODUCTION

Lateral double-diffused MOSFET (LDMOSFET) is widely adopted for medium voltage and smart power applications due to its low on-resistance (R_{ON}) [1, 2] and its compatibility with standard CMOS process [3, 4].

LDMOS transistors are particularly vulnerable to hot-carrier degradation caused by high electric fields leading to the generation of interface traps in the proximity of the Si/SiO_2 interface within the drift region [5]. This causes the shift of the electrical parameters (e.g., R_{ON}) limiting the device lifetime [6].

Since device lifetimes up to 10, 10 years are required in smart-power applications, accelerated stress tests and extrapolation approaches have been implemented in order to access device reliability in reasonable times [7-12].

Hu et al. [7] proposed a model where the time-dependent hot-carrier degradation in MOSFETs follows a simple power-law, whereas in [8] it was shown that the degradation follows a logarithmic time-dependence at longer times. In [9], the model by Goo [10] is enhanced by using a high-resolution measurement technique and non-linear least-square fit of the experimental degradation curves. A similar model has been implemented in the case of power LDMOS transistors [11, 12]. In particular, the model takes into account the self-limiting (saturation) behavior of the degradation. However, all the previous models are based on an acceleration factor (ξ), representing the fraction of hot carriers possessing enough energy to break bonds at the Si/SiO_2 interface. Since the source and body currents need to be separately measured to calculate ξ, such models cannot be applied to the LDMOS architectures featuring shorted source and body contacts to avoid the turn-on of the parasitic BJT between N-drift/P-body/N-source.

In this paper, the experimental R_{ON} degradation induced by hot-carrier stress (HCS) is reported as a function of drain voltage. The model proposed in [9, 11, 12] is modified for application to LDMOS with shorted source-body contacts. Finally, the results of a simple time-power-law and of the simplified self-limiting degradation model are compared, and TCAD simulations aimed at validating the applicability of the model to LDMOSFETs are performed for extremely long stress times.

II. RESULTS AND DISCUSSION

N-channel STI-based power LDMOS transistors with an operating drain voltage of 18 V, fabricated on 200mm silicon wafers by STMicroelectronics, are considered in this work. Fig. 1 shows a sketch of the drift region, where the major contribution to degradation during hot-carrier stress is localized [13]. Accelerated stress tests have been carried out for V_{GS} = 1.9 V, representing the worst case of HCS, as shown by the simulated body-current peak [13]. In order to preliminary identify possible issues related to process variability, devices with very similar I_DV_G transfer characteristics have been selected within the wafer and then stressed. The maximum relative deviation for measured ΔR_{ON} due to dispersion was less than 0.7% while stressing four selected devices for the same stress bias.
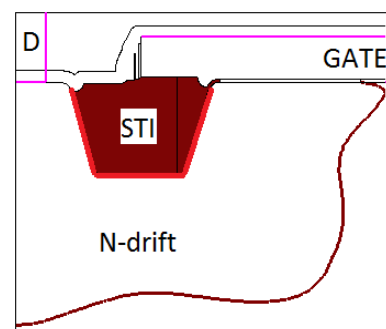
Fig. 1. Sketch of the N-drift region of the STI-based LDMOS transistor. The red line at the STI/N-drift interface is the region where interface trapped charge is monitored in Fig. 6.

A. N. Tallarico, S. Reggiani, E. Sangiorgi, and C. Fiegna are with the Advanced Research Center on Electronic System, Department of Electrical, Electronic, and Information Engineering, University of Bologna, 47521 Cesena, Italy (e-mail: a.tallarico@unibo.it; susanna.reggiani@unibo.it; enrico.sangiorgi@unibo.it; Claudio.fiegna@unibo.it).

R. Depetro, S. Manzini, A. Torti, and G. Croce are with Technology R&D, STMicroelectronics, Agrate Brianza, Italy (e-mail: Riccardo.depetro@st.com; Stefano.manzini@st.com; andreamario.torti@st.com; Giuseppe.croce@st.com).

Fig. 2. Experimental (symbols) ΔR_{ON} vs stress time as a function of the drain voltage. Experimental data have been fitted with a simple power-law (solid line) and with the proposed model (dashed line).
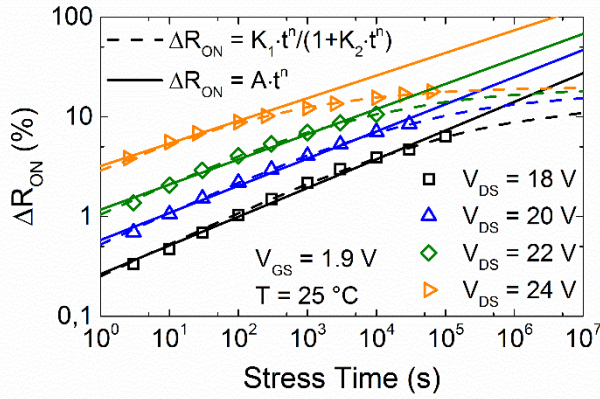
Fig. 2 shows ΔR_{ON} vs stress time for different V_{DS}, measured on-wafer by the constant voltage stress (CVS) technique. By monitoring ΔR_{ON} in linear regime, a saturation occurs at long stress times, particularly evident for V_{DS} = 24 V. The limited increase of ΔR_{ON} at long stress times is typical of LDMOS devices, as they experience the saturation of the broken bonds at the STI corner, followed by a lateral extension of the degradation hot spot. This effect usually takes place for ΔR_{ON} well below the 10% variation. A simple time-power-law (solid line) nicely reproduces the early stage of HCS degradation, but overestimates ΔR_{ON} at long stress times inducing a relevant underestimation of the lifetime projection (Fig. 2).

A more exhaustive model able to account for the saturation behavior of ΔR_{ON} has been proposed over the years [9, 11, 12]:

$$\Delta R_{ON} = \frac{C_1(V_G)\cdot(\xi\cdot t)^{n(V_G)}}{1+C_2(V_G)\cdot(\xi\cdot t)^{n(V_G)}} \qquad (1)$$

$$\xi(V_{GS}, V_{DS}) = \frac{I_{source}(V_{GS},V_{DS})}{W} \cdot \left(\frac{I_{body}(V_{GS},V_{DS})}{I_{source}(V_{GS},V_{DS})}\right)^{\beta} \qquad (2)$$

However, the model in this form, although its physical validity, cannot be applied without monitoring the body and source currents separately, as they are needed to calculate the acceleration factor (ξ) and its dependence on V_{GS} and V_{DS}. In order to overcome such limit, the model has been simplified according to:

$$\Delta R_{ON} = \frac{K_1(V_{GS},V_{DS})\cdot t^n}{1+K_2(V_{GS},V_{DS})\cdot t^n}. \qquad (3)$$

with the two parameters $K_1(V_{GS},V_{DS}) = C_1\cdot\xi^n$ and $K_2(V_{GS},V_{DS}) = C_2\cdot\xi^n$ to be identified by fitting measurements.
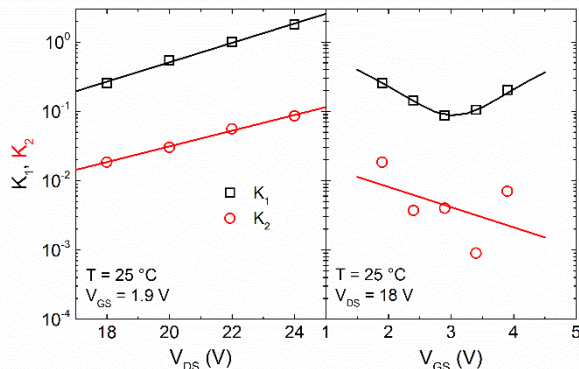

Fig. 3. Drain and gate bias dependent fitting constants K_1 and K_2.

The parameter n (fixed to 0.33 in our case) is the power slope determined by fitting the experimental ΔR_{ON} in a range where the saturation is not taking place, as in the case with the lowest V_{DS} (18 V) at relatively short stress times (< 10^3 s).

Dashed lines in Fig. 2 report the result of the Eq. (3) showing a good agreement with the ΔR_{ON}. The fitting constants K_1 and K_2 are extracted for each stress condition and their dependence on V_{DS} and V_{GS} is shown in Fig. 3. The relationship is universal and can be used in all the cases, even with shorted body-source contacts.

The accuracy of the adopted extrapolation model has been validated against TCAD simulations. The solution of the full-band Boltzmann Transport Equation (BTE) implemented in [14] has been used to predict the energetic distribution of hot electrons. The physics-based degradation model proposed in [15] has been adopted, as it is specifically suited for the HCS in LDMOSs. More details about the model calibration and the physical mechanisms contributing to the de-passivation bonds at the Si/SiO$_2$ interface can be found in [13, 16].
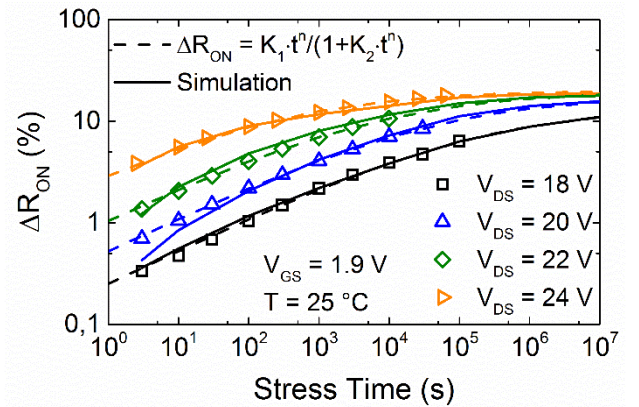

Fig. 4. Experimental data (symbols), TCAD simulated results (solid lines) and model fitting (dashed lines) of ΔR_{ON} vs stress time.

Fig. 4 shows the ΔR_{ON} reproduced with the proposed model (dashed line) and simulated with the TCAD tool [14] (solid line). Both simulation and equation (3) provide an accurate agreement with experimental data for all the considered stress conditions, and allow for an extension to longer stress times confirming the potential and the accuracy of the model, in spite of the simplification introduced ($\xi = 1$ independently of bias conditions).

Fig. 5 compares the lifetimes extrapolated from the experiments by using the different models and from the TCAD data. The corresponding lifetime extrapolations at lower drain biases are given by the conventional power-law (blue lines). By adopting as a failure criterion a ΔR_{ON} of 10% in 1000 hours, the maximum applicable drain voltage at room temperature and V_{GS} = 1.9 V has been extrapolated to be 16.2 V for the simple power-law [7] and 18 V for the proposed model and TCAD simulations.

As expected from Figs. 2 and 4, the difference between the lifetime extrapolated with the simple power-law (Fig. 5, squares) and those extrapolated by the proposed model (Fig. 5, black circles) or by the TCAD simulations (Fig. 5, red circles), increases with the reduction of the applied stress bias, leading to a difference of about one order of magnitude at V_{DS} = 18 V. As a result, an underestimated lifetime or maximum applicable voltage is obtained if the experimental ΔR_{ON} is fitted/reproduced by a simple time-power-law.

Finally, Fig. 6 shows the simulated interface traps generated and charged after a stress of 10^6 s along the STI interface (red line in Fig. 1) for the biases analyzed in Fig. 4. Independently of V_{DS}, the
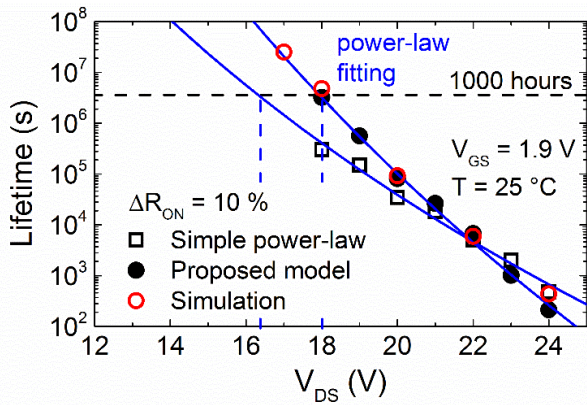
Fig. 5. The 10% of ΔR_{ON} is extrapolated from experiments by the simple power-law (squares), the proposed model (black circles) and the simulation results (red circles).
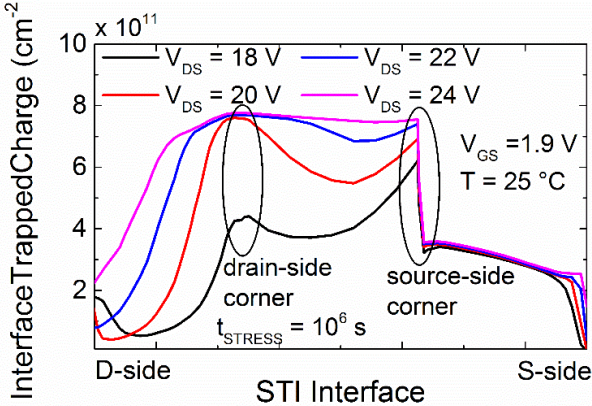

Fig. 6. Traps filled with electrons along the STI interface after 10^6 s of stress at V_{GS} = 1.9 V and different V_{DS}.

interface-trap generation shows a hot spot at the source-side corner, while a second peak at the drain side under the field-plate edge increases with larger V_{DS}. As detailed in [13], at V_{DS} = 18 V impact ionization takes place close to the source-side corner generating a hot spot, whereas by increasing V_{DS} the impact ionization peak increases but it expands toward the drain, intensifying the interface trap generation at the STI bottom and at the drain-side corner.

III. CONCLUSION

In this paper, we investigated the drain-bias dependence of the HCS degradation in a new generation STI LDMOS architecture. By monitoring the ΔR_{ON} during CVS tests, the saturation dynamics is shown, as expected, for long stress times. Previous models in the literature have been taken into account highlighting the respective weaknesses. On the one hand, by adopting a simple time-power-law the saturation effect of the ΔR_{ON} is not accounted for, leading to an overestimated degradation and to an underestimated device lifetime. On the other hand, the adoption of a more complex model [11, 12] is not possible when the body and source contacts are internally shorted as in the case of power LDMOSFETs, not allowing the calculation of the acceleration factor. As a consequence, we proposed a simplified model able to easily evaluate the long-term degradation and hence the device lifetime independent of the body current. Its applicability and accuracy have been proved by comparison with TCAD simulations.

REFERENCES

[1] K. Shirai, K. Yonemura, K. Watanabe, K. Kimura, "Ultra-low on-resistance LDMOS implementation in 0.13 um CD and BiCD process technologies for analog power IC's," IEEE ISPSD, pp. 77-79, Barcelona, Spain, June 2009, DOI: 10.1109/ISPSD.2009.5158005.

[2] W. Ge, X. Luo, J. Wu, M. Lv, J. Wei, D. Ma, G. Deng, W. Cui, Y. H. Yang, K. F. Zhu, "Ultra-low on-resistance LDMOS with multi-plane electron accumulation layers," IEEE Electron Device Lett., vol. 38, no. 7, pp. 910-913, May 2017, DOI: 10.1109/LED.2017.2701354

[3] M. Li, J-M. Koo, R. V. Purakh, "0.18μm BCD Technology Platform with Performance and Cost Optimized Fully Isolated LDMOS", IEEE EDSSC, pp. 820-822, Singapore, June 2015, DOI: 10.1109/EDSSC.2015.7285244

[4] T. H. Lee and P. A. Abshire, "Design and Characterization of High-Voltage NMOS Structures in a 0.5 um Standard CMOS Process", IEEE Sensors J., vol. 13, no. 8, pp. 2906-2913, May 2013, DOI: 10.1109/JSEN.2013.2263795.

[5] P. Moens, G. Van den bosch, C. De Keukeleire, R. Degraeve, M. Tack, and G. Groeseneken, "Hot Hole Degradation Effects in Lateral nDMOS Transistors", IEEE Transactions on Electron Devices, Vol. 51, no. 10, pp. 1704-1710, Sept. 2004, DOI: 10.1109/TED.2004.834913.

[6] P. Moens, and G. Van den bosch, "Characterization of Total Safe Operating Area of Lateral DMOS Transistors", IEEE Transactions on Device and Materials Reliability, Vol. 6, no. 3, pp. 349-357, Oct. 2006, DOI: 10.1109/TDMR.2006.882212.

[7] C. Hu, S. C. Tam, F. C. Hsu, P. K. Ko, T. Y. Chan, K. W. Terrill, "Hot-electron-induced MOSFET degradation: Model, monitor, and improvement," IEEE Transactions on Electron Devices, vol. 32, no. 2, pp. 375-385, Feb. 1985, DOI: 10.1109/T-ED.1985.21952.

[8] C. Liang, H. Gaw, P. Cheng, "An analytical model for self-limiting behavior of hot-carrier degradation in 0.25 μm n-MOSFET's," IEEE Electron Device Letters, vol. 13, no. 11, pp. 569-571, Nov. 1992, DOI: 10.1109/55.192843.

[9] R. Dreesen, K. Croes, J. Manca, W. De Ceuninck, L. De Schepper, A. Pergoot, G. Groeseneken, "Modelling hot-carrier degradation of LDD NMOSFETs by using a high-resolution measurement technique," Microelectronics Reliability, vol. 39, no. 6-7, pp. 785-790, Jun. 1999, https://doi.org/10.1016/S0026-2714(99)00101-8.

[10] J. S. Goo, H. Shin, H. Hwang, D. G. Kang, and D. H. Ju, "Physical Analysis for Saturation Behavior of Hot-Carrier Degradation in Lightly Doped Drain N-Channel Metal-Oxide-Semiconductor Field Effect Transistors," Japanese Journal of Applied Physics, vol. 33, no. 1B, pp. 606-611, Jan. 1994, https://doi.org/10.1143/JJAP.33.606.

[11] P. Moens, J. Mertens, F. Bauwens, P. Joris, W. De Ceuninck, and M. Tack, "A Comprehensive Model for Hot Carrier Degradation in LDMOS Transistors," IEEE IRPS, pp. 492-497, Phoenix, AZ, USA, Apr. 2007, DOI: 10.1109/RELPHY.2007.369940.

[12] E. Riedlberger, R. Keller, H. Reisinger, W. Gustin, A. Spitzer, M. Stecher, "Modeling the Lifetime of a Lateral DMOS Transistor in Repetitive Clamping Mode," IEEE IRPS, pp. 2F4.1-2F4.7, Anaheim, CA, USA, May 2010, DOI: 10.1109/IRPS.2010.5488833.

[13] A. N. Tallarico, S. Reggiani, A. Depetro, A. Torti, G. Croce, E. Sangiorgi, C. Fiegna, "Hot-Carrier Degradation in Power LDMOS: Selective LOCOS- vs. STI-based Architecture," IEEE Journal of Electron Device Society, Vol. 6, no. 1, pp. 219-226, Jan. 2018, DOI: 10.1109/JEDS.2018.2792539.

[14] Sentaurus-Device U.G. v. L-2016.03, Synopsys Inc., 2016.

[15] S. Reggiani, G. Barone, S. Pioli, E. Gnani, A. Gnudi, G. Baccarani, M-Y. Chuang, W. Tian, and R. Wise, "TCAD Simulation of Hot-Carrier and Thermal Degradation in STI-LDMOS Transistors", IEEE Trans. Electron Devices, vol. 60, no. 2, pp. 691-698, Feb. 2013, DOI: 10.1109/TED.2012.2227321.

[16] A. N. Tallarico, S. Reggiani, P. Magnone, G. Croce, R. Depetro, P. Gattari, E. Sangiorgi, C. Fiegna, "Investigation of the hot carrier degradation in power LDMOS transistors with customized thick oxide," Microelectronics Reliability, vol. 76-77, pp. 475-479, Sept. 2017, https://doi.org/10.1016/j.microrel.2017.07.043.