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A Nano-Power Synchronous Charge Extractor IC for Low Voltage Piezoelectric Energy Harvesting with Residual Charge Inversion

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***Abstract*—The paper presents a power converter for piezoelectric energy harvesting implementing a modified version of synchronous electrical charge extraction with quiescent current as low as 160 nA. The input energy is increased of more than 200% for weak vibrations, by inverting the residual charge left on the capacitance of the transducer after each energy extraction. Moreover, a power management policy, named two-way energy storage, is introduced in order to improve significantly the efficiency of the energy harvesting system in battery-less systems during the start-up phase, when the energy storage is fully depleted. The converter behaves as a buck-boost converter and the measured peak efficiency is 85.3%. The IC has been designed in a 0.32 µm microelectronic technology from STMicroelectronics in an active area of 0.95 mm^2.**

***Index Terms*—piezoelectric transducers, energy harvesting, power converter, power management, nano-power.**

I. Introduction

THE field of piezoelectric energy harvesting has been undergoing continuous advances over the last years. In this context, systems make use of piezoelectric transducers and of dedicated electronic interfaces in order to extract power from environmental energy sources such as vibrations, shocks and human movement with the purpose of ubiquitously supplying miniaturized autonomous electronic systems, e.g. wearable or environmental sensors and wireless nodes. The relative high energy density and relative ease of fabrication of piezoelectric materials [1] make them promising candidates for pursuing this goal.

Several types and shapes of piezoelectric transducers have been reported in literature targeting many different types of applications [2][3]. More specifically, a growing effort is devoted to the miniaturization of transducers, key for unobtrusive applications [4]. This means that energy harvesting systems and applications have to deal with very limited power levels, since optimized electro-mechanical designs with macro-scale transducers yield power densities as low as 10-100 µW/cm^3 in many practical cases [5]. In addition, the current trend is to further shrink down transducers with MEMS fabrication processes [6][7], with available power levels down to few µW.

For this reason, a special care has to be put in designing efficient electrical interfaces for power conversion and energy storage with very low intrinsic consumption and power losses. Since the beginning, interfaces based on passive diode rectifiers [8] or switching step-down converters with fixed or variable duty-cycles [9][10] have been proposed for transferring electrical charge from a piezoelectric transducer to a storage capacitor. However, diode voltage drops significantly limit the harvested power especially in case of low input voltages, as it is the case in many energy harvesting applications. Moreover, no power is harvested when the input voltage is lower than that on the output node, introducing an intrinsic limitation to the storable energy.

Such types of limitations were in part overcome by synchronized switch harvesters [11], a category of power converters based on resonant circuits activated in a way synchronous with vibrations. Thanks to the mainly capacitive impedance of piezoelectric transducers (Fig. 1), such interfaces increase both the peak voltage and the harvested power. A notable example is the SSHI technique [13], in which the transducer is connected to a rectifier bridge and to a

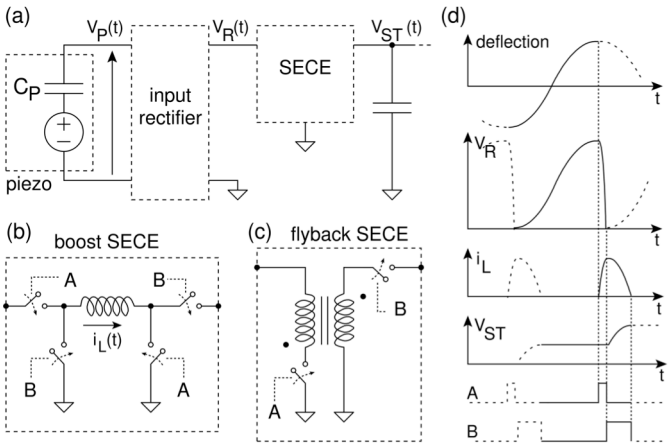

Fig. 1. (a) Structure of a power converter stage based on synchronous electrical charge extraction (SECE) for piezoelectric transducers. (b) a boost topology for SECE. (c) a flyback topology for SECE. (d) Representative waveforms of SECE under the assumption of ideal rectification

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parallel connected switched inductor used for inverting its voltage at the maximum elongation points, i.e. when the bare passive rectifier stops conducting. Such inversion brings the rectifier near the opposite conduction threshold and improves conduction during the next elongation. However, electrical charge is still transferred through the rectifier, making efficiency bias dependent and quite low in case of very low or very high load currents. Another known technique is synchronous electrical charge extraction (SECE) [12][13] in which, when a voltage peak is detected, energy is first transferred from the transducer to an inductor and then to the output through two resonant circuits, in a way similar to a boost converter, as shown in Fig. 1. SECE can also be implemented with a flyback topology [14]-[16] in order to reduce losses on freewheeling diodes. However, the resulting longer switching transients may yield higher energy losses, especially in case of large capacitive loads. Conveniently, the efficiency of SECE does not depend on the output bias, while the complete removal of electrical charge at each activation doubles the peak voltage. Besides this, SSHI [17] and more advanced synchronized harvesters based on multi stage converters or transformers, such as DSSH [18] or SSHI-MR [19] have also been reported to increase the harvested power. On the other hand, such techniques are strongly related to the load condition (SSHI-MR) whereas SECE is almost load-independent or are based on a dual-stage architecture which requires two inductors and is likely addressed to consume more power due to increased control and switching activity.

One of the main drawbacks of the above mentioned interfaces is the use of diodes in practical circuit implementations, as in [13][20][21], whose voltage drops significantly limit the harvested power especially in case of low input voltages, as it is the case in many energy harvesting applications. Alternative solutions, such as cross coupled MOSFETs rectifiers, i.e. negative voltage converters (NVCs) [22], active rectifiers [22] or digitally controlled switches [23] have been demonstrated to improve the power performance. NVCs offer the potential of zero-threshold rectification but allow bidirectional current flows and also suffer from bad performance in case of low input voltages, i.e. lower than the threshold voltage of MOSFETs. Active rectifiers reduce conduction losses at the expense of additional power consumption and are currently promising solutions mainly for integrated circuit implementations where bias currents can be strongly reduced [24][25].

In energy harvesting applications, since replacing or recharging batteries is often problematic, another important aspect is the possibility of designing self-powered battery-less circuits, such for example the SSHI interface in [20] and the SECE circuit in [26], consuming only few μA. Electrical charge is usually stored on low-leakage capacitors sized according to the actual load requirements. In many targeted applications of wireless sensor networks this constraint requires the use of supercapacitors [27], fostered by significant advances towards the reduction of geometries [28] and leakage currents [29]. Despite this, the use of large capacitances in resonant power converters such as the previously mentioned ones, combined with the further constraint of designing micro-power control circuits with limited operating frequencies and bandwidths, may lead to low electrical quality factors, as it will be pointed out later on.

Recently, several integrated circuit for energy harvesting have been proposed [30]-[33] with power consumption in the order of hundreds of nW. Silicon implementation of converters allows, besides a smaller footprint and more complex fully customizable architectures, a reduction of power of at least an order of magnitude with respect to optimized discrete components realizations [34]. Indeed, specific energy aware circuital design techniques, converter topology and silicon implementation allow the exploitation of ultra-low power sources with a positive output energy budget. The use of such sources, and of the associated power levels, would be prevented by a design using discrete components and the harvesting effectiveness is likely to be compromised.

This paper will introduce a series of circuit techniques for optimizing charge collection and power management in piezoelectric energy harvesters subject to weak vibrations. As a first contribution, the residual charge on transducers will be exploited for achieving improved energy conversion efficiency, with respect to existing solutions, when operating with low voltages. Besides this, the paper will introduce a power management policy for selectively routing the harvester power to the application load or for internal needs, with a resulting faster start-up time and higher efficiency than conventional solutions. Such techniques will be considered in the perspective of nano-power integrated circuit design, tackling realistic application constraints, including switch implementation, minimization of intrinsic power consumption and full energy autonomy. The design will be validated through the characterization of prototypes based on a full custom silicon design.

II. SECE WITH RESIDUAL CHARGE INVERSION

A careful design of the input interface is mandatory in order to achieve high efficiencies while extracting charge from piezoelectric transducers, especially when low voltages are involved. The more efficient this process is, the higher the duty cycle of operation of the final application, e.g. data acquisition and wireless transmissions, will be. In energy harvesting systems, energy should be collected as long as it is available from the environmental sources. For this reason, a buck-boost topology is a suitable candidate as input stage. In fact, in passive rectifiers and step-down converters the output voltage cannot exceed that on the input whereas it is likely required to extract energy in the opposite situation. Among buck-boost topologies, piezoelectric transducers subject to weak and irregular vibrations are efficiently handled with SECE, which is also compatible with micro-power control circuits [26]. In self-powered implementations of SECE, since piezoelectric voltages often switch from negative to positive voltages, the difficulty of generating dual voltage supplies is usually overcome by using input rectifier stages, whose

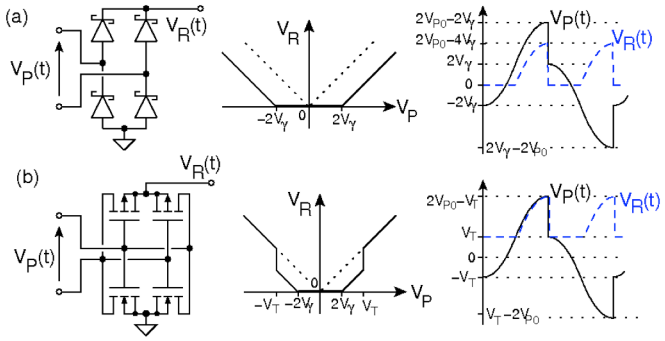

Fig. 2. Schematic, voltage transfer characteristic and transient behavior during SECE with: (a) BR; (b) NVC.

voltage drops, however, limit efficiency in case of low input voltages. Energy conversion, as mentioned in Section I and shown in Fig. 1, is activated on local maxima of the rectified voltage. Energy is first extracted from the piezoelectric capacitance C_P with a switched inductor L_1 forming a L_1-C_P resonant circuit. Then, energy is transferred from L_1 into a storage capacitor C_O by forming a second L_1-C_O resonant circuit. Since the L_1-C_O resonant circuit is never connected to the piezoelectric transducer, a measure of the capability of a SECE interface to extract power is given by the energy stored in the inductor at the end of the first phase.

Let us suppose that $V_P(t) = V_{P0}\sin(2\pi ft)$ is the voltage generated across the transducer in open circuit, where f is the vibration frequency. If a full-wave bridge rectifier (BR) is adopted (Fig. 2a) as input interface, in case of conduction the rectified voltage is $V_R(t) = |V_P(t)| - 2V_\gamma$, where V_γ is the threshold voltage of a single diode and $V_R(t) \geq 0$. When SECE is activated on a voltage peak, the transducer is discharged through the rectifier and the inductor until $V_R(t) = 0$. Then, the rectifier turns off and a residual voltage $\pm 2V_\gamma$ is left on $V_P(t)$. From this condition, since a peak-to-peak elongation produces a voltage variation $2V_{P0}$ on the transducer, a maximum voltage $2(V_{P0} - V_\gamma)$ can be reached on $V_P(t)$.

If we define $\gamma = V_\gamma/V_{P0}$, with $0 < \gamma < 0.5$, the energy stored in L_1 at the end of the first phase can be computed by solving the differential equations of the L_1-C_P circuit, as demonstrated in [34]:

$$E_L^{(BR)} = 2C_P V_{P0}^2 (1-2\gamma)^2 e^{-\pi/(\omega_{01}\tau)}, \quad (1)$$

where $\tau = 2L_1/R_1$, with R_1 assumed to be the resistance of switches, inductor and transducer of L-C_P, and $\omega_{01} \cong 1/\sqrt{L_1 C_P}$.

In case a NVC is used (Fig. 2b), $V_R(t) = V_P(t)$ as long as $|V_P(t)| > V_\gamma$, where V_γ is the absolute value of the highest MOSFET threshold voltage. With respect to diodes, MOSFETs offer negligible voltage drops and energy losses. However, on the activation of SECE, during the discharge of $V_P(t)$, the NVC turns off when $|V_P(t)| = V_\gamma$. For lower voltages, conduction may still occur through the FET body diodes, which would introduce significant losses, so that energy extraction should safely stop at V_T. Then, at the end of the subsequent elongation, a maximum absolute voltage $2V_{P0} - V_\gamma$ will be reached on $V_P(t)$.

If we define $\delta = V_T/V_{P0}$, with $0 < \delta < 1$, the energy stored in L_1 after the transducer has discharged from $2V_{P0} - V_\gamma$ to V_T can be determined:

$$E_L^{(NVC)} = 2C_P V_{P0}^2 (1-\delta) e^{\frac{-2\arccos\left(\frac{\delta}{2-\delta}\right)}{\omega_{01}\tau}}. \quad (2)$$

In the above two cases no power is harvested for absolute input voltages lower than the minimum conduction thresholds of $2V_\gamma$ and V_T, and residual charges $|Q_{BR}| = 2C_P V_\gamma$ and $|Q_{NVC}| = C_P V_T$ are left at the end of every conversion. Such residual charge has to be first canceled during the subsequent peak-to-peak elongation before the sign of $V_P(t)$ changes.

As a term of comparison, a lossless SECE with an ideal rectifier with $V_\gamma = 0$ (IR) would leave no residual charge and store in L_1 the following energy for a single activation:

$$E_L^{(IR)} = 2C_P V_{P0}^2 e^{-\pi/(\omega_{01}\tau)}. \quad (3)$$

In this section we propose an input interface based on a NVC with residual charge inversion (RCI), shown in Fig. 3. This allows to reduce energy losses through the MOSFET bridge and to remove all the charge $Q_{PP} = 2C_P V_{P0}$ generated in a peak-to-peak elongation. The inversion of residual charge applies a more favorable voltage offset for the next peak-to-peak elongation. Other types of pre-biasing techniques, in which the offset charge is drawn from the output, were introduced in [35] and showed to significantly increase the performance. However, in case of low output voltages, e.g. when high load currents are applied, the advantages of the pre-bias are reduced. Differently, this work exploits as a bias the inverted residual charge, which otherwise would impact negatively output power. This approach improves the

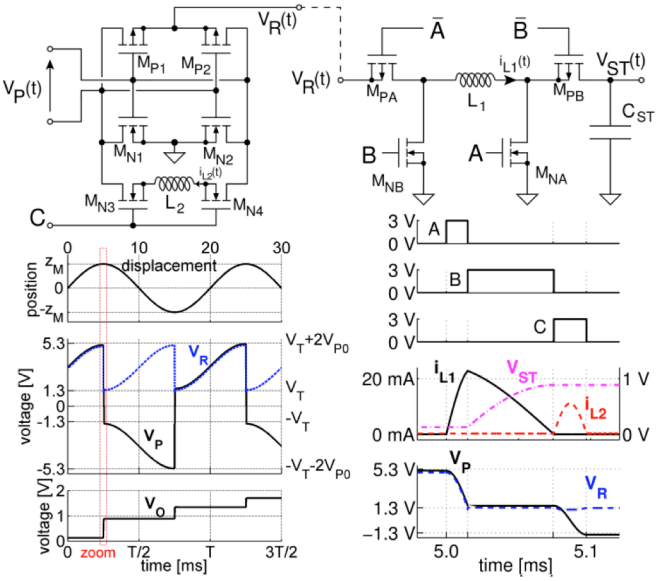

Fig. 3. Schematic and circuit simulations of a SECE circuit based on a NVC with the proposed RCI. Circuit simulations were performed with $V_{P0} = 2$ V, $f = 50$ Hz, $L_1 = 10$ mH, $L_2 = 2.5$ mH, $C_O = 1$ µF. $M_{N1..4}$ and $M_{P1,2}$ are standard discrete MOSFETs with $|V_T| = 1.3$ V A zoomed view of an individual energy conversion is also shown.

performance especially in case of low vibrations, when the input voltage is comparable to the conduction threshold and the losses would otherwise be significant. The inversion of residual charge is also performed in other synchronized switch techniques, such as for example SSHI, in which charge inversion is mostly required for keeping a rectifier bridge in a conducting state for most of the time. However, the conversion efficiency is still bias dependent. Differently, besides producing significantly higher piezoelectric voltages, performing RCI with SECE also introduces a bias independent energy conversion efficiency, because the transducer is never directly connected to the output node.

As shown in Fig. 3, with respect to SECE, an inductor L_2 and two switches M_{N3}, M_{N4} are introduced. An additional signal C is activated for inverting the residual charge left on the transducer. This is accomplished by letting the resonant circuit C_P-L_2 oscillate for a half period π/ω_{02}, where $\omega_{02} \cong 1/\sqrt{L_2 C_P}$ is its resonance frequency. This new initial offset would ideally allow to reach a higher maximum voltage $2V_{P0} + kV_T$ on $V_P(t)$, where k=exp(–π /($\omega_{02}\tau_2$)), τ_2=2L_2/R_{2eq} and R_{2eq} is the series resistance of L_2 and of the RCI switches (M_{N3} and M_{N4} in Fig. 3). It can be found that the energy stored in L_1 after the transducer has discharged from $2V_{P0} + kV_T$ to V_T is:

$$E_L^{(RCI)} = 2C_P V_{P0}{}^2 \left(1 + k\delta + \frac{k^2-1}{4}\delta^2\right) e^{\frac{-2\arccos\left(\frac{\delta}{2+k\delta}\right)}{\omega_{01}\tau}} \quad (4)$$

Typical values for the components that have been considered for analytical evaluations are $V_\gamma \cong 0.35$ V for low threshold Schottky diodes, e.g. BAT754, and $V_T \cong 1.3$ V for discrete MOSFETs with low gate charge and compatible with piezoelectric voltages of up to 20 V, e.g. BSS138PW and NTR1P02T1, and $V_T \cong 1$ V for generic integrated MOSFETs. Hence, in practical cases, it roughly holds that $\delta/\rho \cong 2\ldots3$.

The corresponding energy ratios of (1), (2) and (4) normalized to $2C_P V_{P0}{}^2$, i.e. E_0, are functions of δ and ρ for a given set of circuit parameters. A comparison plot is shown in Fig. 4. As it can be observed, Schottky rectifiers underperform with respect to NVC and RCI is the best option, especially for low input voltages. However, this holds for an integrated circuit perspective. For a discrete components design, Schottky rectifiers perform better than NVC for low input voltage due to typical high MOSFET V_T unless RCI is employed.

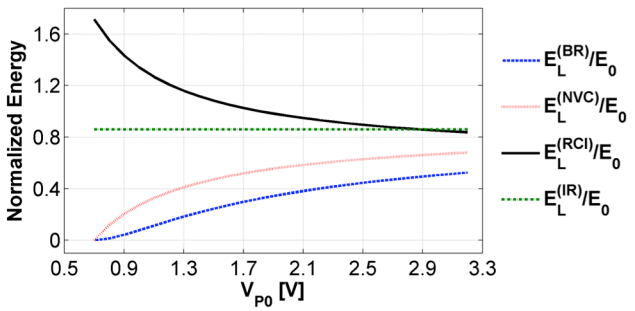

Fig. 4. Normalized energy ($E_0 = 2C_P V_{P0}{}^2$) extracted from C_P and stored in L_1 at the end of the first phase of SECE with different types of the input interface: full-wave bridge rectifier (BR), NVC, NVC with RCI enabled (RCI), and ideal rectifier (IR). The parameters used for the generation of the figure are: $V_T \cong 1$ V, $V_\gamma = 0.35$ V, $C_P = 52$ nF, $L_1 = L_2 = 560$ µH, $R_1 = 10$ Ω, $R_{2eq} = 5$ Ω.

The OSECE topology [15] is an interesting improvement of classic SECE topology. Differently from the latter, it exploits three coupled inductors and diodes. OSECE has a lower circuit complexity (switches and their controllers) and is surely more suitable than SECE for an implementation with off-the-shelf components, although some works implementing SECE converters have been reported [34]. However, in order to improve efficiency, reduce size and costs on large volumes, an integrated solution is advisable. Several works [30][33][36] use active rectifiers for diodes replacement as they have lower losses and lower inverse leakage current than diodes. The command energy required for the MOSFET and its driver is very small for integrated circuits compared to PCB circuits with discrete components and, furthermore, it can be tailored on application requirements (i. e. switching frequency, turn-on delay and on-resistance). In such a perspective, an integrated version of OSECE with active rectifiers might offer better performance than the PCB solution and even outperform an integrated SECE. A drawback of active switches and rectifiers is their inability to operate without a supply and therefore a start-up mechanism is required (e.g. a secondary passive rectifier in parallel with the active one).

However, a significant difference between SECE with RCI and OSECE lie in the amount of inverted charge on the piezoelectric transducer. With SECE-RCI such amount of charge is independent from both the load and the input parameters and depends only on the characteristics of the MOSFETs employed in the NVC (i.e. their $V_{GS,th}$). Differently, in OSECE the amount of inverted charge strongly depends on the output voltage (i.e. load), transformer turns ratio and diodes characteristics. With high turns-ratio of the transformer, the inverted charge might be very low and provide a less favorable offset than SECE-RCI.

III. Two-way Energy Storage and Power Management Policy

A typical issue of self-powered harvesting systems exploiting active converters (i.e. not a bare BR) is the start-up time required for transition from passive to active harvesting mode. Systems with a single energy storage element [21,22,28-30] rely on such energy reservoir both for supplying both the converter supply and the load. Since application requirements, e.g. for sustaining a wireless sensor node transmission, require a minimum amount of stored energy and a minimum voltage to enable operation, usually large capacitors or supercapacitors are used. As a consequence, a considerable amount of time ranging from seconds to hours [30][37] may be required for switching from a passive harvesting interface to an active power conversion interface, which also require a minimum operating voltage. During this period, the efficiency of energy extraction is negatively affected. A second issue is the inability of the load to consume

all the energy in the storage element without compromising the operations of the converter by bringing it back into passive mode. This limits the energy available to the load because a considerable amount of energy is locked in the storage capacitor just for keeping the output voltage high enough for enabling the power converter and without the possibility of being used by the load. In systems with a huge energy storage, e.g. a tens of mF supercapacitor, such amount of wasted energy is intolerable, especially if a second buck-boost regulator is placed between the harvester and the load with the task of generating a stable and regulated supply voltage

The proposed power management policy is similar to that introduced in [16], [38]-[40] and makes use of two different capacitors, as shown in Fig. 5: the converter power supply is provided by C_{DD} whereas the load is powered from C_{ST}. Furthermore, this scheme, which will be referred to in this paper as two-way energy storage (TWS), allows the load to completely drain C_{ST} without affecting the operation of the active power converter. In [16], [38], [39], C_{DD} is charged initially through a passive path to start the active converter and, when the voltage on C_{ST} is sufficient, the two capacitors are shorted or connected through a diode so that the incoming power sustains both the converter and the load. In the presented architecture, during the start-up phase C_{DD} is passively charged trough a secondary passive rectifier, implemented with a NVC with a diode in series (NVCD), until the minimum voltage V_{DDmin} required for properly powering the active conversion process. This phase is expected to be much shorter than in single storage systems because of the significantly lower value of C_{DD} with respect to C_{ST} for sustaining the power converter. Then, as soon as SECE is started, the energy flow is directed towards C_{DD} until it is recharged at least to a higher voltage $V_{DDact,max}$ in order to keep the converter supply in the required operating range, which is a priority task as it will be shown in the next paragraph. $V_{DDact,max}$ is not the maximum allowed supply voltage, but it is the higher threshold voltage of an hysteretic level comparator used for routing energy alternatively to C_{ST} and C_{DD} (i.e. for activation of S_{ST} or S_{DD} in Fig. 5). Then, the energy flow is diverted to C_{ST} as long as V_{DD} remains above a second threshold voltage $V_{DDact,min}$ chosen for preserving a high conversion efficiency. Below this voltage, energy is diverted to C_{DD} again to keep the power converter functional. It holds that $V_{DDmin} < V_{DDact,min} < V_{DDact,max}$.

In order to assess the advantages of TWS, it is useful to compare the energy extracted by the NVCD passive interface, i.e. when the minimum baseline voltage is still not reached in a single storage system with a large capacitor, with the energy extracted by SECE. The output energy in passive operation (i.e. when SECE is not activated) $E_{P,BR}$ per half-wave can be evaluated by integrating the current through the diode in the passive path in Fig. 5 with a fixed output V_{DD}, assumed to be constant in the half-period (e.g. with a large capacitor or a supercapacitor) and the resulting expression for $E_{P,BR}$ is the following:

$$E_{P,BR} = 2C_P V_{DD}\left(V_{P0} - V_{DD} - V_\gamma\right). \tag{5}$$

The SECE process has an intrinsic efficiency value η_S, defined as the energy transferred to the output divided by the energy removed from the transducer in a single charge extraction, which is also dependent on circuit parameters and components. In an ideal case it holds that $\eta_S = 1$. In order to evaluate the performances of TWS, the effectiveness of SECE with NVC and BR are compared using the ratio $\eta_P = E_{P,BR} / E_L^{(NVC)}$. The ratio η_P accounts for the efficiency of SECE with NVC and, approximating to unity the exponential term in $E_L^{(NVC)}$, it can be written as:

$$\eta_P = \frac{1}{\eta_S}\frac{V_{DD}}{V_{P0} - V_T}\left(1 - \frac{V_{DD} + V_\gamma}{V_{P0}}\right). \tag{6}$$

The numerical evaluation of (6) is illustrated in Fig. 6 for some values of V_{P0} and it is clearly shown that the theoretical efficiency of the ideal SECE (η_S=1) is higher than the BR in any case (as $\eta_P < 1$). This also holds with a non-ideal SECE with a sub-optimal efficiency $\eta_S = 0.5$. Therefore, it is advisable to use SECE with respect to a passive rectifier in any configuration, as soon as it is possible. In addition, if a supercapacitor (from mF to the F range) is required, the use of a single energy storage element for supplying both the converter and the load is not optimal for the start-up phase, i.e. from 0 V to V_{DDmin}, because this phase relies on a passive rectifier for energy harvesting. In the above considerations, RCI was not considered. Anyway, enabling also RCI reinforces the above conclusions, as it will be shown experimentally in Section V.

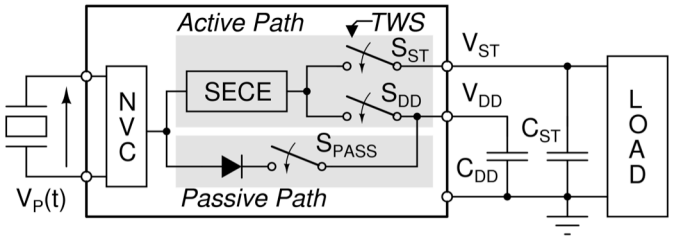

Fig. 5. Block diagram showing the active and passive charging paths in the converter and TWS for the active path.

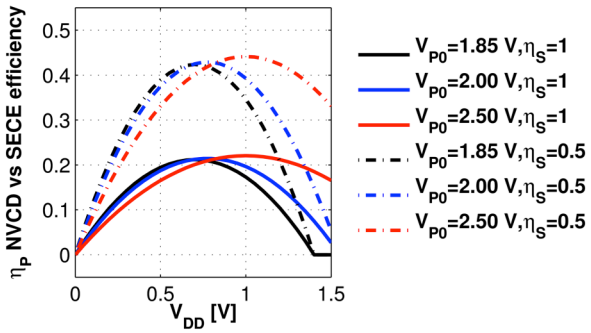

Fig. 6. Efficiency of passive charging of storage element (NVC+Diode) for start-up with respect to SECE. As can be pointed out, the efficiency is less than 50% even for SECE with a low conversion efficiency ($\eta_S = 0.5$). The values used for the evaluation are $V_T \cong 1$ V (for generic MOSFETs) and $V_\gamma = 0.35$ V (for generic Schottky diodes).

IV. Converter architecture

The architecture of the proposed converter implementing a self-starting SECE with RCI and TWS, which has been designed in a 0.32 µm microelectronic technology from STMicroelectronics, is depicted in Fig. 7. The converter requires two external capacitors C_{DD} and C_{ST}, two inductors L_1 and L_2 and a variable resistor R_{RCI}, which is used for setting the duration of RCI. In a future version of the converter, a single inductor can be utilized rather than L_1 and L_2 as the utilization factor of each inductor is very low. In fact, the use of a second inductor L_2 for the RCI circuit is not mandatory and only L_1 might be used for both the buck-boost converter and the RCI circuit, as the RCI phase can be executed immediately after a full cycle of the buck-boost converter. However, this would require major design changes in the control logic. Since the main purpose of this work was to assess the effectiveness of RCI, two separate inductors were used in this design for ease of implementation.

Once the converter has started active operations (i.e. SECE) the transducer is always kept in open circuit by the switch S_S, which is normally open. As the converter operates as a buck-boost converter, there is never a direct conduction path from the transducer to V_{ST} or V_{DD}. Moreover, RCI is performed directly on the transducer nodes and thus RCI is not affected by the load and by V_{ST} or V_{DD}. RCI depends only on the rectifier characteristics, hence on the threshold voltage $V_{GS,th}$ of the MOSFETs in the NVC, and on the series resistance of the associated L_2-C_P circuit.

The converter draws nominally a quiescent current I_{DDq} equal to 160 nA when no energy extraction cycles are preformed (i.e. in idle state) at V_{DD} = 2.7 V. The current drawn from each sub-circuit, obtained by simulations, is listed in Table I.

A. Passive start-up

This part of the circuit is shown in Fig. 8. The piezoelectric transducer is firstly connected to an NVC which outputs the rectified version V_R of the input voltage V_P (i.e. during the negative half-waves the sign is inverted). At start-up from a discharged state, a pMOS diode M_{PD} and a depletion nMOS M_{Nd} (i.e. a normally-closed switch) connect V_R to V_{DD} allowing the latter to be passively charged. The converter starts to operate actively (i.e. SECE is activated) as soon as $V_{DD} \geq V_{DDmin}$ = 1.4 V. At that voltage, an under-voltage lock-out (UVLO1) circuit triggers and M_{Nd} is turned off blocking the passive charging path towards C_{DD} and then the buck-boost *converter* is activated and SECE is performed. An hysteresis of about 100 mV is added to the UVLO in order to prevent undesired on-off switching due to noise and small variations on V_{DD}. Actually, the minimum required input voltage amplitude for a successful start-up operation is V_{P0} = 1.8 V. However, as C_{DD} is usually comparable with the output capacitance of the piezoelectric transducer (in this work $C_{DD} \cong$ 200-470 nF), it only takes a few oscillation periods in order to charge C_{DD} up to V_{DDmin} and start SECE. Once SECE and RCI are started, the converter can successfully extract energy with input voltages down to 0.7 V.

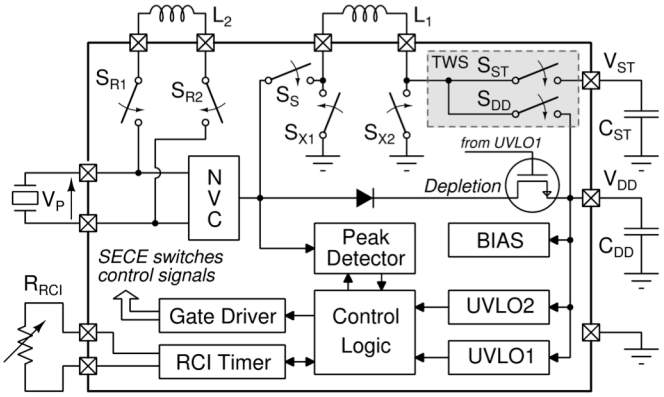

Fig. 7. Block diagram of the designed converter IC.

TABLE I SIMULATED QUIESCENT CURRENT DRAWN BY EACH SUB-CIRCUIT OF THE CONVERTER.

Sub-circuit	*Current [nA]*
Bias	48
UVLO1	16
UVLO2	16
Peak Detector	32
Bias (in Buck-boost converter)	16
Other[1]	32

[1]This current is drawn by a comparator detecting whether V_{ST} is greater than an externally applied voltage reference. Such function is not used by the converter but its consumption has been considered in the evaluation of the quiescent current as well as in the experimental results.

The passive start-up block draws 64 nA nominally and embeds a supply-independent bias circuit which generates a reference current of 16 nA and outputs the reference voltages V_{BP} and V_{BN} which are used as inputs for biasing all the analog circuitry of the IC.

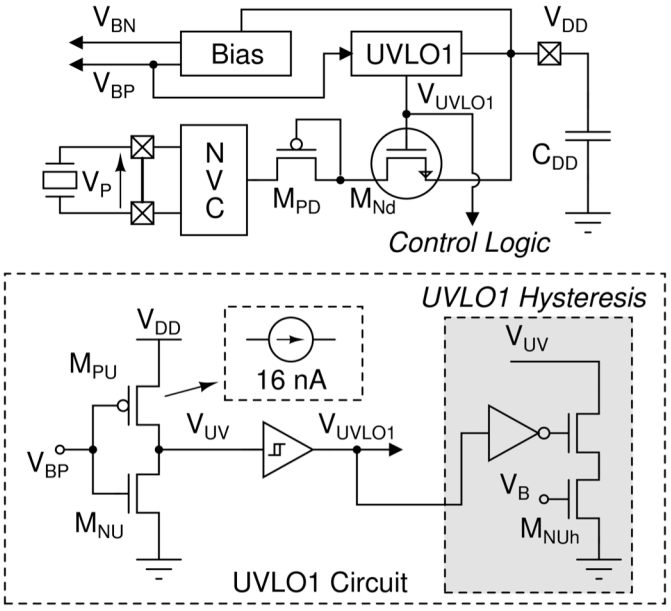

Fig. 8. Passive start-up circuit and details of UVLO1 circuit diagram.

B. Piezoelectric transducer interface

The NVC output V_R is tracked by an ultra-low power peak detector and an energy extraction cycle is performed on each maximum of V_R. The circuit diagram of the interface for the piezoelectric transducer is shown in Fig. 9. It is composed by an NVC for signal rectification, a switch for the connection to the main inductance L_1, a peak detector and the switches for RCI. The first stage of the peak detector is an input signal conditioning block and such stage is required in order to filter the input signals lower than the minimum value of V_{Pmin} = 700 mV. It also includes an RC filter (R_f and C_f) with a -3dB cut-off frequency of 5.3 kHz in order to smooth the spikes generated during RCI and prevent false peak detections. M_{F1} and M_{F3} are low threshold nMOS transistors. The next stage is composed of a voltage tracking circuit and a hysteretic comparator with hysteresis $V_h = \pm 15$ mV. The static current drawn by the peak detector is as low as 32 nA, equally divided between the voltage tracking block (OPA_{PK}) and the hysteretic comparator (CMP_{PK}). The voltage tracking block charges C_{track} with M_{P2} in order to keep $V_{track} = V_{Rf}$. As charge on C_{track} can only be added by M_{P2}, a maximum is detected by the comparator when $V_{Rf} \leq (V_{track} - V_h)$ and, in this case, the PEAK signal is set to V_{DD}. At the end of an energy extraction cycle C_{track} is reset by M_{Nr} in order to rightly track the next half-wave on V_{Rf} and detect the following maximum; V_{RESET} is generated by the logic controller on the falling edge of CONV signal, which is activated by the control logic only during energy extractions. As V_P (and thus V_R) can exceed V_{DD}, the amplifier OPA_{PK}, the current mirror M_{P1}-M_{P2} and the comparator CMP_{PK} are supplied by the highest voltage between V_{DD} and V_R by a dedicated bulk regulator circuit.

The switch connecting V_R and V_{LX1} is composed by both a nMOS and a pMOS and both gates are driven by a gate driver (GD) which, for the case of M_{PS}, is constantly supplied by the highest voltage between V_{DD}, V_{LX1} and V_R in order to completely turn off M_{PS}.

The RCI circuit is made of two nMOS switches M_{R1} and M_{R2}, which connect V_{P1} and V_{P2} to the inductor L_2. The RCI phase is started by the logic controller as soon as the energy on C_P has been extracted. In this implementation, the length of the RCI phase is set by the value of a resistor R_{RCI}, which alters the RC constant in a pulse generator (RCI Timer shown in Fig. 7). The timing of RCI is deeply analysed and illustrated in the next section, together with buck-boost converter operation.

C. Buck-boost converter with TWS

The buck-boost converter (circuit diagram shown in Fig. 10) is managed by a clock-less logic controller which implements an asynchronous finite state machine (FSM). When a maximum is detected PEAK is set to V_{DD} and the FSM is activated from idle state. The end of each phase of the energy extraction process (energy transfer from C_P to L_X and from L_X to C_{ST} or C_{DD}) is dynamically determined by means of zero-voltage switching (ZVS) and zero-current switching (ZCS) detectors, This grants many degrees of freedom in the choice of the piezoelectric transducer, C_{DD}, C_{ST}, L_X, input power level and output voltage, because conversion timings are not hard-coded in the control circuits. While the converter is performing the second phase of the energy extraction process (i.e. energy transfer from L_X to C_{ST} or C_{DD}), the RCI is activated in order to invert the residual charge on C_P. The signals of the FSM, the input voltage V_P, and V_{LX2} are shown in Fig. 11. The extraction process starts as soon as the PEAK signal rises. The analog circuitry is normally turned off in idle state in order to minimize static current (down to 16 nA). When the extraction process starts, the dynamic bias block is turned on (BM=0, active low) and, as it is the first phase of the energy extraction process, signals are set as follows: $V_{GX2} = V_{DD}$ (which is the same signal as CONV in Fig. 9) and $V_{GX1} = 0$ V. The end of the first phase is notified by the rising edge of ZVS signal. The second phase of the energy extraction is the transfer of energy from L_1 to C_{ST} (or C_{DD}) with $V_{GX1} = V_{DD}$ and $V_{GX2} = 0$ V; V_{LX2} is clamped to V_{ST} in Fig. 11 which was forced, in this case, to 2 V. Simultaneously, the RCI is performed on the piezoelectric transducer (RCI control signal high and voltage inversion on V_P shown in the traces of Fig. 11). The second

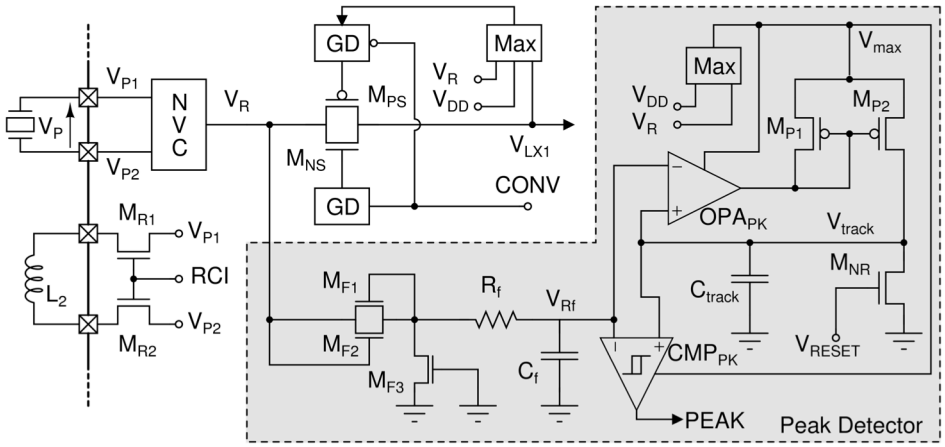

Fig. 9. Circuit diagram of the interface for the piezoelectric transducer.

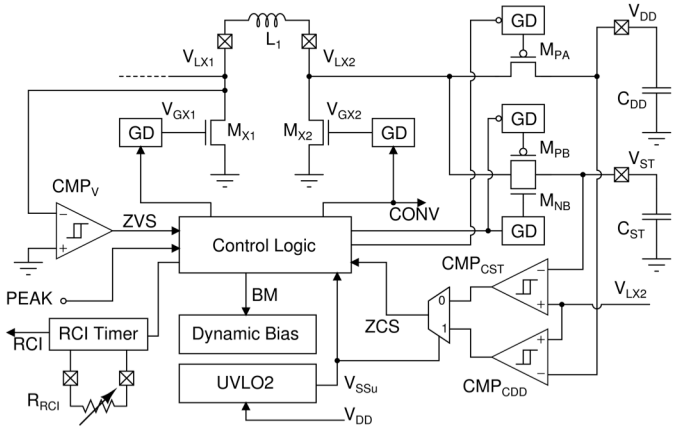

Fig. 10. Circuit diagram of the SECE converter.

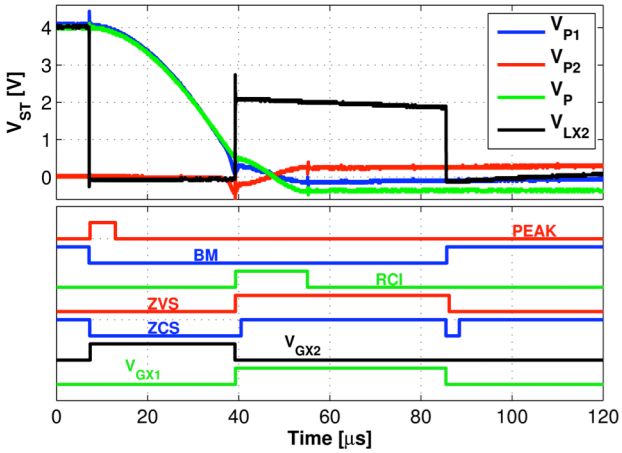

Fig. 11. Waveforms acquired from a sample device measurement during an energy extraction cycle. Both SECE and RCI are shown together with internal control signals (on bottom). In such acquisition, the energy was directed towards C_{ST}.

phase ends as all energy is moved to C_{ST} (or C_{DD}) and this is notified by a falling edge of ZCS. The inputs of the FSM are normally masked and are enabled only during the FSM state in which they are relevant in order to prevent incorrect operations. ZCS is achieved by monitoring the voltage on M_{PA} (or M_{PB}) due to its on-resistance and ZCS is effectively detected when V_{ST} - $V_{LX2} \leq$ -15 mV (or V_{DD} - $V_{LX2} \leq$ -15 mV). Such scheme allows flexibility and adaptability at the cost of a lower efficiency for values of V_{ST} approaching 5 V because di_{L1}/dt increases and the discharge time of L_1 becomes comparable with the propagation delay of the comparator CMP_{CST} (or CMP_{CDD}) which is about 800 ns.

The UVLO2 circuit in Fig. 10 is similar to UVLO1 in Fig. 8 but it has different thresholds which determine $V_{DDact,min}$ and $V_{DDactmax}$. UVLO2 switches it state when V_{DD} rises above 2.6 V and when it drops below 2 V. Its output V_{SSu} notifies the control logic whether to charge C_{ST} or to start a C_{DD} charging sequence in order to provide energy to the converter itself. On the right of Fig. 12, TWS operation on a measurement with a sample of manufactured devices is illustrated and the V_{SSu} signal, brought out of the chip with a test structure, is highlighted. The high state of the signal (about 1 V) means that the UVLO2 circuit has detected that V_{DD} is below the minimum value and thus the converter is forced to direct energy towards C_{DD} instead of C_{ST}.

V. Experimental Results

The power converter has been manufactured in a 0.32 µm technology from STMicroelectronics in an active area of 0.95 mm^2. The converter is placed in a 4.6 mm^2 die, whose micrograph is shown on the left of Fig. 13. The setup used in the performed measurements is depicted on the right of Fig. 13 and the values of the used external components are shown in Table II. The chosen piezoelectric transducer is a Q220-A4-303YB from Piezo Systems which has a nominal output capacitance C_P = 52 nF. Since the focus of the paper is on the converter design and the use of RCI and TWS, a first series of measurements has been performed with a real piezoelectric transducer in order to prove the functionalities of the proposed approach. Then, other experiments, whose aim was to

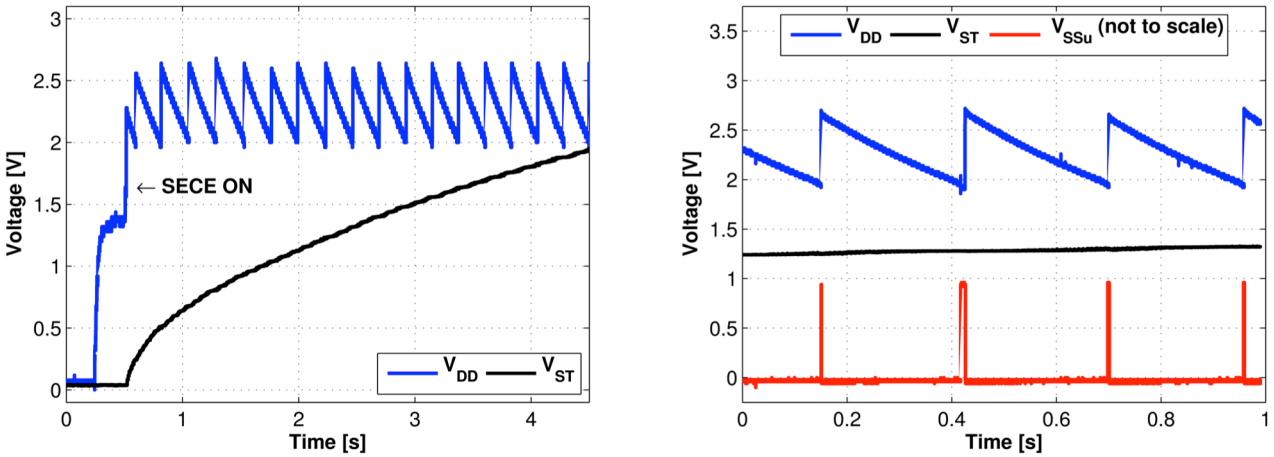

Fig. 12. (left) Waveforms acquired from a sample device measurement showing the TWS operating principle. C_{ST} is slowly charged while V_{DD} is charged only when its value is below a certain threshold, in order to keep the active converter enabled. The experimental conditions were: V_{P0} = 2 V, C_P = 47.4 nF, f = 60 Hz, C_{ST} = 66 µF, C_{DD} = 200 nF, L_1 = 10 mH, L_2 = 560 µH. (right) Detail of the TWS operations with the slow discharge of V_{DD} due to self-consumption. V_{SSu} (amplitude not to scale in the figure because it has been acquired from a test structure externally supplied) is the output of UVLO2 circuit and goes high when C_{DD} needs a re-charge sequence.

quantitatively characterize the performance of the circuit from an electric point of view, have been performed by emulating the transducer with laboratory equipment for higher accuracy and precision in the electrical quantities. The emulation was performed with an Agilent 33120A function generator setting the open-circuit voltage V_{P0} and a series-connected metallized polypropylene capacitor of 47.4 nF.

Firstly, as mentioned above, the IC has been tested with the piezoelectric transducer, as shown in Fig. 13. The load was emulated with a Keithley 2601 SMU forcing a load current of 8.25 µA in order to obtain $V_{ST} = 2.5$ V, which is a typical supply voltage for low power electronics. The piezoelectric transducer was excited with an electro-dynamic shaker vibrating at f_P=50 Hz and with an acceleration $a_{RMS} = 0.1$ *g*. With RCI enabled, the energy conversion efficiency, evaluated as the ratio between output power and available input energy times the energy extraction frequency (i.e. $f_P C_P V_{Pmax}^2$ where V_{Pmax} is the transducer peak voltage generated by the non-linear energy extraction process), has been experimentally determined at 72.2%, with an extracted power from the transducer of 28.57 µW. However, we highlight that in the above experiment the IC was self-supplied with the harvested power and the reported efficiency value also includes the contribution of the IC intrinsic (ultra-low) power consumption. For this reason, the overall efficiency of the bare power conversion is higher than this value.

The second experiment is the measurement of the quiescent current of the IC with a Keithley 2601 SMU forcing V_{DD} and measuring the drawn current while it is not performing any energy extraction and with an external bias on V_P of 1 V. The results are shown in Fig. 14. The IC draws about 160 nA in its typical operating voltage (V_{DD} from 2 V to 3 V) and this is very important for energy-limited scenarios. Then, by forcing V_{DD}=2.7 V externally with the same SMU and filtering its output with an RC filter (with $R = 1$ MΩ, $C = 4.7$ µF) the average current drawn from V_{DD} by the converter has been measured, sweeping the input signal frequency from 20 to 100 Hz with $V_{P0} = 1.5$ V and $C_P = 47.4$ nF. The obtained

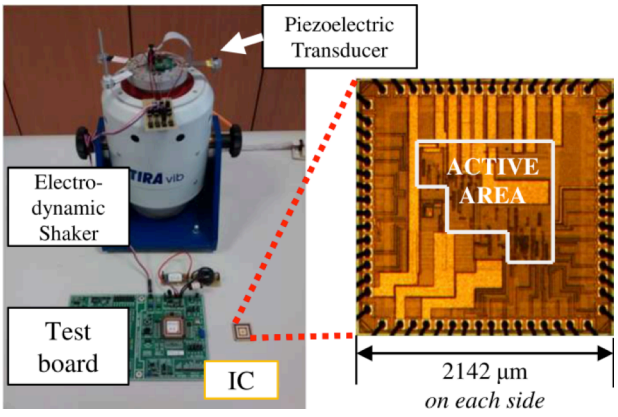

Fig. 13. Experimental setup used for measurements, based on the IC, a test board and a piezoelectric transducer stimulated by an electrodynamic shaker (left). Die micrograph with active area highlighted. (right).

TABLE II. VALUES OF EXTERNAL COMPONENT USED IN ALL EXPERIMENTS.

Component	Value	DC Series Resistance
L_1	10 mH	4.4 Ω
L_2	560 µH	0.36 Ω
R_{RCI}	1…5 MΩ*	-
C_P	47.4 nF	-
C_{DD}	470 nF	-
C_{ST}	10 mF	.

* The value of R_{RCI} must be tuned to set the duration of RCI to $\pi/\sqrt{L_2 C_P}$ in order to obtain maximum RCI performance

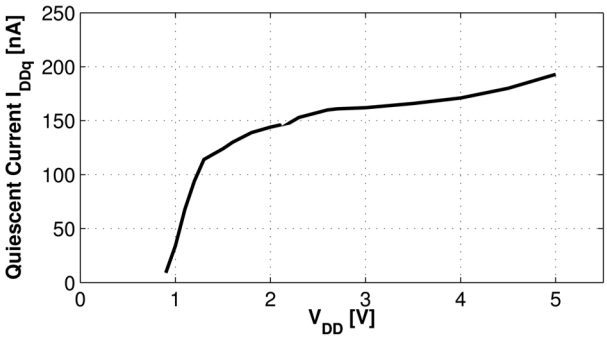

Fig. 14. Quiescent current drawn by the converter in stand-by state (no energy extractions are performed) for several V_{DD} values.

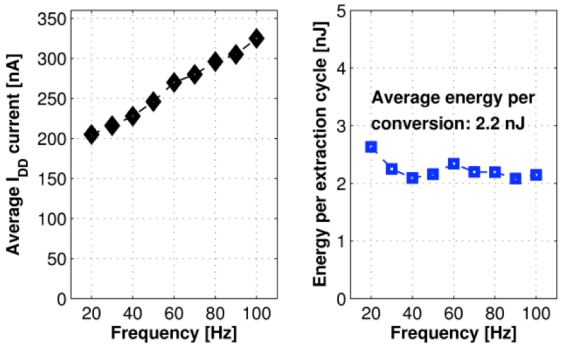

Fig. 15. (left) Measured average current I_{DD} drawn on V_{DD} for several input signal frequencies. (right). Energy required for a single energy extraction, calculated from the measured I_{DD} when SECE-RCI is enabled.

results for the total current drawn I_{DD} are show on the left of Fig. 15 whereas the dynamic energy required per energy extraction cycle is shown on the right of Fig. 15 and it is calculated from the difference between I_{DD} and the measured I_{DDq} of 166 nA (at $V_{DD} = 2.7$ V). The average value of the dynamic energy per conversion is 2.2 nJ, and is small, typically less than 3%, with respect to the available energy on a piezoelectric transducer ($0.5 C_P V_{Pmax}^2$) with C_P in the order of some tens of nF.

In order to estimate the minimum input power required by the converter, a third experiment has been performed starting from an operating condition (with RCI enabled) and decreasing the input power down to 296 nW ($f_P = 7$ Hz $V_{P0} = 500$ mV, $C_P = 47.4$ nF). In such conditions the converter

stops to provide energy to C_{ST} but it is able to sustain itself and to continue performing SECE with RCI at V_{DD} = 1.54 V.

The TWS has been validated through a fourth experiment: firstly, V_{DD} and V_{ST} have been connected together in order to emulate a classic single way storage (SWS) system; in a second time, the TWS technique has been enabled (i.e. V_{ST} and V_{DD} are independent). As previously discussed, in the start-up phase SECE and RCI can only be performed in the TWS system. The output voltage V_{ST} has been acquired with a Tektronix MSO2024 digital oscilloscope in both cases and the results are shown in Fig. 16. TWS, together with SECE and RCI, is considerably improving the energy extraction process with an increase of more than 6.5 times of the harvested energy after 1000 s with respect to SWS (which, further, does not benefit from SECE and RCI) under the same input conditions (piezoelectric transducer emulated with V_P = 2 V, f = 60 Hz, C_P = 47.4 nF). The gain of TWS over SWS is present only when V_{ST} < 1.4 V, because above this value SECE is activated also for SWS. However, this power management policy allows a quicker charging of the output from discharged states during start-up than with SWS, which becomes quite evident when C_{ST} is a large capacitor, e.g. a supercapacitor in the mF range. In the latter case the start-up phase of a SWS can take up to several minutes or hours [30][37] with supercapacitors and weak and irregular vibrations. In this latter case, activating SECE in the initial phases significantly boost efficiency. In addition, the efficiency of SECE is quite independent from the output load condition [34][41], which results in an almost constant efficiency throughout the whole charging process.

In a fifth experiment, the efficiency of the energy transfer from C_P to C_{ST} has been measured and Fig. 17 shows the results for several values of V_P spanning into the allowed range of operation of the IC. In this experiment C_{ST} = 66 µF and a Keithley 2601 SMU was used as a constant current load. The measured peak efficiency is 85.3% for V_P = 2.35 V. However, except for V_{P0} = 1 V, the efficiency is quite similar. The efficiency loss with V_{P0} = 1 V is mainly due to incorrect ZCS timing: the time for energy transfer from L_1 to C_{ST} is

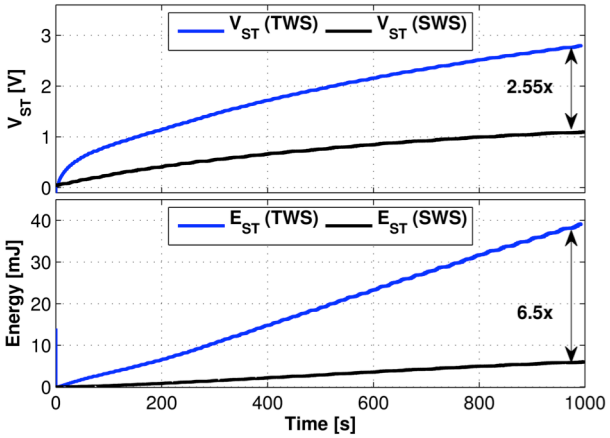

Fig. 16. Comparison of acquired V_{ST} voltage with C_{ST}=10 mF in two configurations (SWS and TWS) with the same input excitation: piezoelectric transducer emulated with V_{P0}=2 V, f=60 Hz, C_P=47.4 nF.

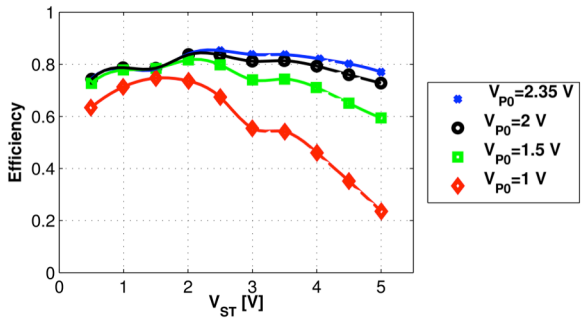

Fig. 17. Energy conversion efficiency for several values of V_{P0} at a frequency of 60 Hz with V_{DD} = 2.7 V externally supplied. Component values in Table II..

approximately proportional to the V_P / V_{ST} ratio and, as charging progresses, it becomes comparable with the delay of the ZCS comparator and with the time required for detecting a negative (i.e. discharging C_{ST}) current on L_1. However, this is a necessary trade-off for reducing the intrinsic power consumption for operating with very low input power levels.

The output power dependence from the equivalent load resistor is shown in Fig. 18. Data are obtained from the fifth experiment. The equivalent load resistance is evaluated by dividing the voltage V_{ST} by the current forced by SMU. The SMU current was chosen in order to obtain V_{ST} ranging from 500 mV (points on the left of Fig. 18) to 5 V (points on the right of Fig. 18), with steps of 500 mV. The dependency of output power from the load resistance is low, as expected from a SECE converter. In addition, two main effects can be observed. The first affects the output power (i.e. the energy transfer efficiency) for low value of load resistance and is caused by the increase of damping on the inductor L_1 current. This is due to the longer time needed for transferring the energy from L_1 to C_{ST} and to the smaller V_{GS} that turns on the M_{PB} p-channel MOSFET in Fig. 10 (part of switch S_{ST} in Fig. 7). On the other side, for higher load resistance (and thus V_{ST}) the main issue is due to the delay between the detection of the zero crossing of the inductor L_1 current and the turn-off of S_{ST}.

A sixth experiment has been used for the evaluation of the effectiveness of RCI and a comparison has been made with RCI enabled and disabled. After setting an operating point with V_{ST} = 1 V and then with V_{ST} = 2 V, the output power of the converter has been measured with RCI enabled and, at a

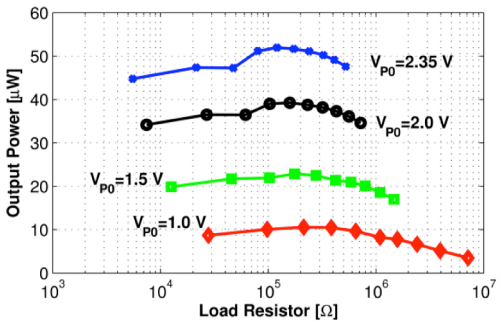

Fig. 18. Output power dependence on equivalent load resistance for different input voltage levels covering the allowed operating regions of the chip.

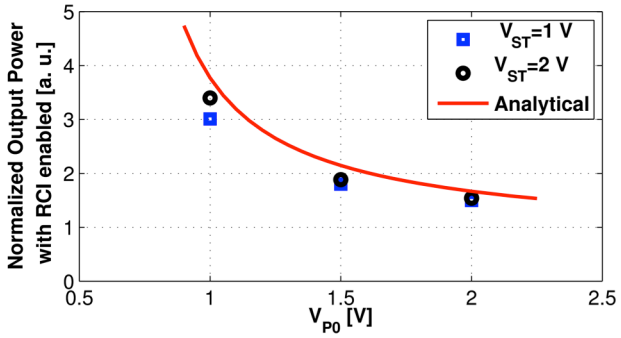

Fig. 19. Analytical performance improvement in output power of RCI and comparison with measured data on manufactured devices. For the analytical evaluation, $V_T \cong 1$ V and the other component values are listed in Table II.

later stage, with RCI disabled and for different values of piezoelectric open-circuit voltage V_{P0}. The output power has been measured with the same methodology as the efficiency in the previous paragraph. The ratios between output power with and without RCI are illustrated in Fig. 19 in which the theoretic value, computed as the ratio of (4) over (2) is also shown. As it can be seen, the output power increases up to three times and there is a satisfactory agreement with analytical values (red line) and measured points. The mismatch in this case is mainly due to the resistive losses on the RCI switches, which do not allow to perform a full voltage inversion.

A comparison of the experimental results obtained on the designed converter with other recent works on SECE converters is shown in Table III.

VI. Conclusion

A nano-power converter with an advanced energy storage power management policy and an input energy improvement scheme for piezoelectric energy harvesting has been presented. The IC draws a quiescent current as low as 160 nA and about 500 nA when actively extracting energy with an excitation of 60 Hz. The measured peak efficiency is 85.3% for $V_{P0} = 2.35$ V. The RCI scheme improves the extracted power of more than 200% for $V_{P0} = 1$ V and it is especially effective for weak vibrations. The proposed power management policy, the TWS, improves the overall converter performances during the start-up, significantly reducing the time required to charge an almost depleted supercapacitor. Moreover, TWS allows the load to drain all stored energy on C_{ST} if required, and still prevents the converter from being stopped by the load current requirement, as the conveter supply is on a different capacitor than C_{ST}. In this prototype, two separate inductors have been used respectively for SECE and RCI. However, a single inductor may be time multiplexed for performing both function at the expenses of an increased circuit complexity. The size of the active area is 0.95 mm^2 in a 0.32 µm microelectronic technology, and the circuit may be used as a functional block in a SoC for energy autonomous WSN.

TABLE III. COMPARISON OF INTEGRATED SECE IMPLEMENTATION.

Parameter	[41]	[16]	This Work
Technology	0.35 µm	0.35 µm + off-chip MOSFETs	0.32 µm
Year	2012	2013	2014
Quiescent current	1.76 µA[1]	330 nA[2]	160 nA
Maximum input voltage	20 V	>70 V	5 V
Maximum output voltage	5 V	3.3 V	5 V
Features	PSCE	MS-SECE, TWS (off-chip)	RCI, TWS
Peak Efficiency	85% at $V_P = 12.8$ V	61% at $V_P = 40$ V	85.3% at $V_P = 4.6$ V

[1] equivalent current estimated from reported power losses. [2] equivalent current estimated from reported power consumptions.

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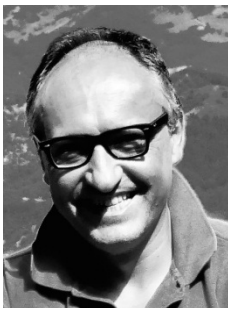

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