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ZVS Analysis of an Interleaved Current-Fed DAB for Bipolar and Unipolar DC Grids

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Abstract—This paper presents a comprehensive zero-voltage switching (ZVS) analysis of an interleaved current-fed dual active bridge (CF-DAB) converter under single-phase-shift control, targeting both bipolar and unipolar DC microgrids. Compared to conventional ZVS conditions, the presence of interphase inductors, either at the input or output bridges, enables an extended ZVS region, particularly under light-load conditions. This is important to increase the overall system efficiency, since in many applications, including DC microgrids, most of the time, such a converter operates at partial load. In addition, for unipolar DC microgrids and balanced bipolar systems, the interphase inductor currents may exhibit a DC offset or remain centered around zero, while under unbalanced load conditions, a DC offset is resulted. To cover both cases, analytical ZVS boundary expressions are derived for both scenarios: with and without DC offset. Experimental validation is conducted on a 300 W scaled-down prototype for the no-offset case, confirming that the CF-DAB can achieve reliable soft-switching over a wide voltage gain range with appropriate inductor design.

Index Terms—bipolar grids, current-fed dual active bridge (CF-DAB), interleaved inductors, soft-switching, unipolar grids, zero voltage switching (ZVS).

I. INTRODUCTION

DC microgrids have gained significant attention and adoption in recent years due to their suitability for a wide range of applications, including DC-powered buildings [1], all-electric ships [2], more-electric aircraft [3], and other emerging

technologies. These systems offer several advantages by supplying power directly in DC form, such as improved energy efficiency, reduced conversion losses, and seamless integration with renewable energy sources [4]. As interest in DC microgrids continues to grow, there is an increasing demand for advanced power electronic solutions capable of addressing the diverse requirements of these applications. One of the main requirements related to DC microgrids is isolation due to safety reasons and protection.

Among isolated DC-DC converters for DC microgrid applications, the dual active bridge (DAB) is widely adopted due to its soft-switching capability, bidirectional power flow, and galvanic isolation via a high-frequency transformer [5]. It achieves high efficiency through zero voltage switching (ZVS) during turn-on, significantly reducing switching losses. However, ZVS is limited under light-load and wide output voltage variations, leading to increased switching losses [6].

To address this, several studies have modified the magnetic components to extend the ZVS range and improve light-load performance [7]–[13]. Notably, [14] studied auxiliary inductors in a DAB under single-phase-shift (SPS) control, expanding the ZVS region and providing design guidelines for full-load ZVS. Despite its advantages, the conventional DAB remains constrained by a narrow voltage gain range and unipolar output operation [15].

A key challenge in advancing DC microgrids is the development of power electronic converters capable of supporting both unipolar and bipolar systems while maintaining high efficiency, reliability, and cost-effectiveness, including at light loads and partial conditions. Wide conversion ratio DC-DC converters are essential in meeting this need, as they ensure compatibility across diverse microgrid configurations and operating conditions. To this end, the authors in [16], [17] investigated an interleaved current-fed DAB (CF-DAB) that supports both

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unipolar and bipolar outputs. While several studies have investigated ZVS behavior in CF-DAB converters [18]–[22], to the best of the authors' knowledge, a comprehensive ZVS analysis of the interleaved CF-DAB under SPS control has not yet been reported. Therefore, this paper presents a detailed ZVS analysis of the interleaved CF-DAB operating under SPS modulation, providing insights into both bipolar and unipolar DC microgrid applications.

The rest of the manuscript is organized as follows: Section II presents the background and ZVS analysis of the conventional DAB. Section III describes the operation of the CF-DAB and provides analytical ZVS evaluation with and without DC offset cases in both bipolar and unipolar applications. Section IV details the experimental validation for the case without DC offset, and finally, Section V concludes the paper.

II. BACKGROUND ON DAB ZVS REGIONS

Fig. 1(a) depicts the DAB converter consisting of two symmetrical active bridges connected by an HF transformer with a $k : 1$ turns ratio. The two H-bridges (input and output bridges) allow full bidirectional power transfer, while the HF transformer enables galvanic isolation with reduced size, weight, volume, and cost. The leakage inductances L_d acts as an energy storage device, favoring soft-switching operation conditions. The simplest way to control the converter is to provide a phase-shift d between the two square wave voltages v_a and v_b (i.e., duty cycle $\delta = 0.5$), with the switching period serving as the normalization base. Being v_a and v_b periodic waveforms (with amplitudes V_a and V_b , respectively), the phase-shift can be limited to $-0.25 \leq d \leq +0.25$, where phase shift polarity determines the polarity of the power flow.

Fig. 1(b) shows the leakage inductance current in a general case ($V_{dc} \neq V_o$) over half of the switching period T_{sw} . Thanks to topology and modulation symmetry, the leakage inductor current i_L can be deduced over a half period and can be solved for two different states $0 < t < dT_{sw}$ and $dT_{sw} < t < T_{sw}/2$. Hence, the leakage inductor currents $i_L(0)$ and $i_L(dT_{sw})$ shown in Fig.1(b) can be expressed as:

$$i_L(0) = \frac{V_a}{4f_{sw}L_d}[G(1-4d)-1], \quad (1)$$

$$i_L(dT) = \frac{V_a}{4f_{sw}L_d}[G+4d-1], \quad (2)$$

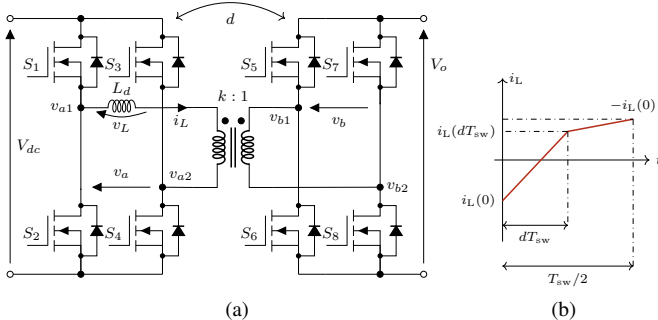


Fig. 1. (a) Dual-active-bridge converter; (b) leakage inductor current.

having switching frequency f_{sw} and voltage gain $G = kV_b/V_a$.

A. Ideal Boundary Conditions of the ZVS Region

The ZVS condition is fundamentally triggered when, during turn-on intervals, the anti-parallel diode enters conduction before the switch. This effectively eliminates turn-on switching losses by exposing the switch to the diode forward voltage rather than the full V_{dc} shortly before its conduction. This condition translates into having $i_L(0) \leq 0$ for the input bridge and $i_L(dT_{sw}) \geq 0$ for the output bridge. In light of (1) and (2), the following boundary conditions of the ZVS region can be determined for both input and output bridges:

$$G \leq \frac{1}{1-4d}, \quad (3)$$

$$G \geq 1-4d. \quad (4)$$

From (3) and (4) it is clear that at any moment at least one bridge is working under the ZVS commutation. When both conditions are met, a complete soft-switching turn-on action can be achieved. From Fig. 2, the shaded region in case $G < 1$ refers to the input ZVS, i.e., all the switches on the input side work under the ZVS, and on the contrary, the $G > 1$ refers to the output ZVS. The remaining area labeled as ZVS represents conditions in which both the input and output side power switches work under the ZVS region. It stands out that only in the case of $G = 1$ it is possible to achieve FL ZVS at all values of d . Hence, the majority of applications (e.g., smart transformers) are based on the choice of the transformer ratio k to ensure $G \approx 1$.

III. OPERATING PRINCIPLE OF AN INTERLEAVED CF-DAB

The CF-DAB topology shown in Fig. 3 operates similarly to a conventional DAB under SPS control but includes two interphase inductors, L_1 and L_2 , forming a two-leg interleaved buck structure on the secondary side. These inductors connect each converter leg's middle point to the split DC link, effectively distributing the output voltage across capacitors C_1 and C_2 . In this work, both interphase inductors are assumed to be equal, i.e., $L_1 = L_2 = L$, allowing the output current I_o to split between the two legs. The output current that flows through the interleaved inductors is defined as $I_o = I_- - I_+$, where I_+ and I_- represent the currents flowing

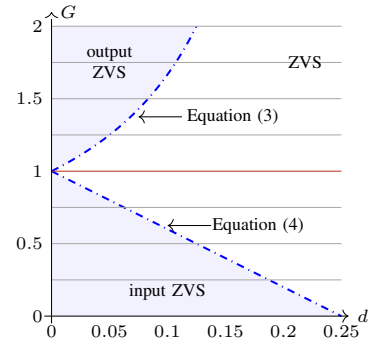


Fig. 2. Ideal case ZVS region in the G vs d plane for the conventional DAB.

through the upper and lower DC rails, respectively, as shown in Fig. 3. This configuration supports a wide voltage gain due to the current-fed nature of the topology and is compatible with both unipolar and bipolar DC microgrids. In particular, bipolar grids utilize the $\pm V_o/2$ ports (indicated as green in Fig. 3), while unipolar grids connect to the $+V_o/2$ port (indicated as purple in Fig. 3).

In bipolar operation with balanced loads, the upper and lower DC rail currents are equal, $I_+ = I_-$, resulting in zero current at the midpoint, i.e., $I_o = 0$. Consequently, no DC offset appears in the interleaved inductor currents. However, under unbalanced conditions where $I_+ \neq I_-$, a net midpoint current arises, $I_o \neq 0$, introducing a DC offset in the interleaved inductors. Since both inductors are assumed equal ($L_1 = L_2 = L$), each inductor carries an offset of $I_o/2$. Whereas, in unipolar operation, if the load is connected between the midpoint and the lower DC rail, the upper DC rail current becomes zero ($I_+ = 0$), leading to $I_o = -I_-$. Conversely, if the load is connected between the upper DC rail and the midpoint, the lower DC rail current is zero ($I_- = 0$), resulting in $I_o = I_+$. In both cases, a nonzero DC offset current of either $+I_o$ or $-I_o$ flows through the interleaved inductors, depending on the load connection.

In summary, depending on the load conditions, the interphase inductors in the CF-DAB can exhibit either no DC offset or a positive/negative DC offset, in both bipolar and unipolar applications. Although the converter operates similarly to a conventional DAB, the presence of ripple due to switching actions and offset currents in the interphase inductors influences the conventional ZVS boundaries described in (3) and (4). As a main contribution, this paper presents a detailed ZVS analysis of the CF-DAB under SPS control, considering both zero and nonzero DC offset cases.

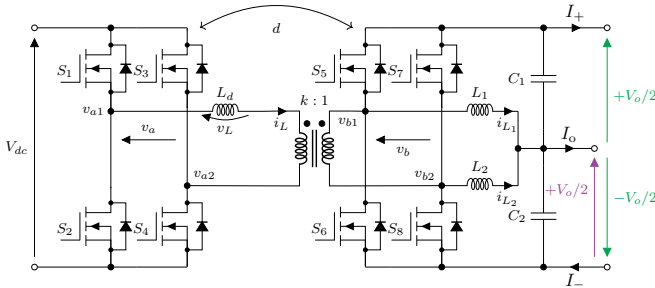


Fig. 3. Interleaved current-fed dual-active-bridge converter.

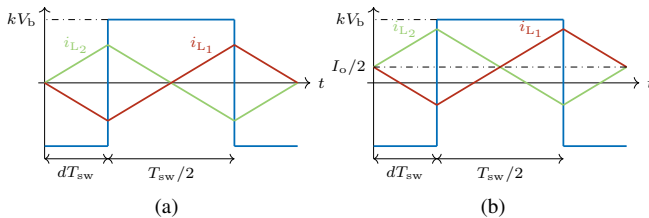


Fig. 4. Voltage and current waveforms of the interphase inductors: (a) zero DC offset; (b) positive DC offset.

A. ZVS Analysis of the CF-DAB without the DC offset case

As shown in Fig. 4(a), the interphase inductor currents i_{L1} and i_{L2} over half of the switching period T_{sw} , exhibiting no DC offset current ($I_o = 0$). The circuit can be equivalently modeled using a single inductor with an effective inductance of $L_1 + L_2 = 2L$. The resulting inductor current i'_L captures the combined ripple behavior of i_{L1} and i_{L2} . The peak amplitude of this triangular ripple can be analytically expressed as:

$$\hat{i}_L = \frac{kV_b}{8f_{sw}(L)}. \quad (5)$$

On applying Kirchhoff's Current Law (KCL), the leakage inductor current of the output bridge $i_L(dT_{sw})$ defined in (2) modifies as:

$$i_L(dT_{sw}) = \frac{V_a}{4f_{sw}L_d}[G + 4d - 1] + \hat{i}_L, \quad (6)$$

that by considering the parameter $\beta = 2L/L_d$, the output side leads to the following ZVS criterion:

$$G \geq (1 - 4d) \frac{\beta}{1 + \beta}. \quad (7)$$

From (7), under no-load conditions ($d = 0$), the ZVS criterion simplifies, allowing the calculation of ΔG_o , which quantifies the effective extension of the conventional ZVS range on the output bridge [14]. This extension is given by:

$$\Delta G_o = 1 - G = \frac{1}{1 + \beta}, \quad (8)$$

where ΔG_o represents the additional ZVS margin achieved due to the interleaved output structure.

Fig. 5 illustrates the extended ZVS region for various values of β . The ZVS condition for the input bridge remains identical to that of a conventional DAB, determined by (3). In contrast, for the output bridge, due to the presence of interleaved inductors, the ZVS region expands toward the low-power operating range (i.e., smaller values of d), as quantified by the increase in ΔG_o . This expansion reduces the input ZVS area at light load while keeping the maximum d at a fixed position. However, reducing the β can increase the switch current RMS, as discussed in [14]. Notably, as $\beta \rightarrow +\infty$, the ZVS condition (7) converges to that of the conventional SPS case given in (4). Moreover, if the

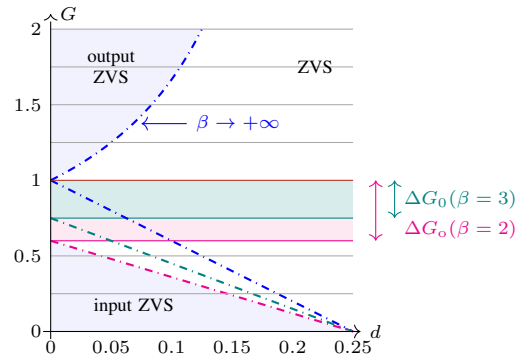


Fig. 5. Without DC offset case ZVS region in the G vs d plane for the CF-DAB.

interphase inductors are instead connected on the input side, the leakage inductor current $i_{L}(0)$ is altered, which in turn enlarges the ZVS region of the input bridge. Therefore, the CF-DAB operating in zero DC offset case offers a clear advantage in enabling wide voltage gain operation while achieving ZVS on both bridges, even under light-load conditions, with the trade-off of higher switch current RMS.

B. ZVS Analysis of the CF-DAB with the DC offset case

As mentioned, the interphase inductors exhibiting a DC offset can be either positive ($I_o > 0$) or negative ($I_o < 0$), depending on the load connection. Fig. 4(b) depicts the inductor currents i_{L_1} and i_{L_2} under a positive DC offset condition. In this case, since $L_1 = L_2 = L$, the peak amplitude of the triangular ripple can be formulated as:

$$\hat{i}_L = \frac{kV_b}{8f_{sw}L} + \frac{I_o}{2} \ , \quad (9)$$

Notice that when $I_o = 0$, (9) simplifies into (5). On applying KCL, the leakage inductor current of the output bridge $i_L(dT_{sw})$ defined in (2), modifies as:

$$i_L(dT_{\text{sw}}) = \frac{V_a}{4f_{\text{sw}}L_d}[G + 4d - 1] + \hat{i}_L, \quad (10)$$

that by considering the parameters $\beta = L/L_d$, the output bridge ZVS boundary now splits into two distinct conditions: one for the lower switches, G_L^{sw} , and one for the upper switches, G_U^{sw} . This results in the following ZVS criterion:

$$G_L^{sw} \geq (1 - 4d - \alpha) \frac{2\beta}{1 + 2\beta} \ , \quad (11)$$

$$G_U^{sw} \geq (1 - 4d + \alpha) \frac{2\beta}{1 + 2\beta} \ , \quad (12)$$

where α is defined as:

$$\alpha = \frac{2f_{\text{sw}}L_{\text{d}}I_{\text{o}}}{V_{\text{a}}} . \quad (13)$$

As shown in Fig. 6(a), which corresponds to the case of $\beta \rightarrow \infty$ and $I_o > 0$, the ZVS region of the input bridge remains defined by the conventional boundary. In contrast, the output bridge ZVS region splits into two distinct boundaries, denoted as G_{TL}^{SW} and G_{TU}^{SW} . The separation between these boundaries is

governed by the parameter α , which increases with the output current I_o . As α increases, the region between G_L^{sw} and G_U^{sw} widens, indicating a broader operating range where only partial ZVS is achieved. Specifically, satisfying the condition G_L^{sw} ensures that the lower switches (S_6 and S_8 from Fig. 3) operate under ZVS, while the upper switches (S_5 and S_7 from Fig. 3) experience hard switching.

Similarly, Fig. 6(b) corresponds to the case of $\beta \rightarrow \infty$ and $I_o < 0$. The ZVS region of the input bridge remains the same as the conventional boundary. However, the roles of the two output bridge ZVS boundaries are reversed, with $\alpha < 0$ representing the negative DC offset current.

In general, as $|\alpha|$ increases, the separation between G_L^{sw} and G_U^{sw} also increases, expanding the region where only partial ZVS occurs. To ensure full ZVS on the output bridge, both boundary conditions G_L^{sw} and G_U^{sw} must be met. When $\alpha = 0$, corresponding to the zero DC offset case, the two boundaries coincide and resemble the ZVS boundary defined in (7). However, it should be noted that for a given phase shift d , the output current I_o also becomes fixed, which in turn determines the value of α and thus the separation between the two ZVS boundaries. Consequently, at lower d values, the reduced output power limits the maximum attainable DC offset I_o , thereby narrowing the region between G_L^{sw} and G_U^{sw} . This constraint is not reflected in Fig. 6 and will be addressed in detail in future work.

Fig. 7(a) and (b) correspond to the cases of $\beta = 1.5$ with $I_o > 0$ and $I_o < 0$, respectively. The input bridge ZVS remains unaffected due to the absence of interphase inductors. Whereas, the output bridge ZVS changes, with the boundary splitting into two as a result of the DC offset. As β decreased, both ZVS boundaries are shifted downward at lower d values, reducing the input ZVS region and narrowing the gap between G_L^{sw} and G_U^{sw} compared to the $\beta \rightarrow \infty$ case. However, reducing the β can increase the switch current RMS, similar to the zero DC offset case. Therefore, proper design guidelines must be followed to ensure wide voltage gain operation while maintaining lower switch current RMS and reliable ZVS conditions. A similar analysis can be extended to the case where the interleaved inductors are connected to the input bridge. In that scenario, the leakage inductor current $i_L(0)$ is modified accordingly, leading to partial ZVS on the input bridge switches at particular operating conditions, as discussed in [14].

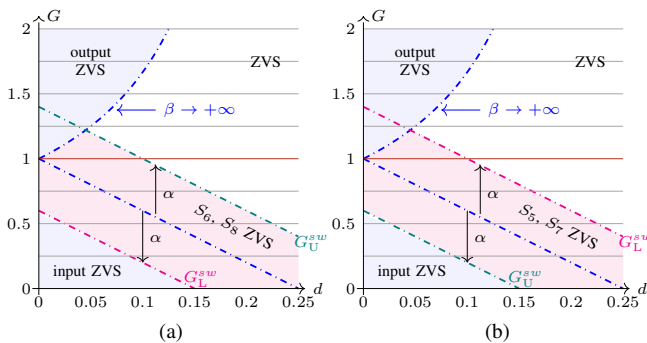


Fig. 6. ZVS region in the G vs d plane for $\beta \rightarrow \infty$: (a) positive DC offset; (b) negative DC offset.

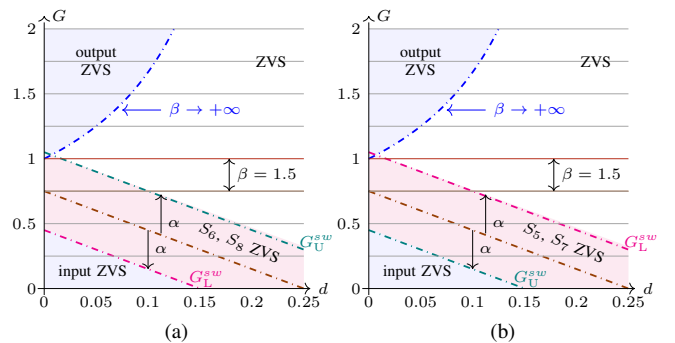


Fig. 7. ZVS region in the G vs d plane for $\beta = 1.5$: (a) positive DC offset; (b) negative DC offset.

IV. EXPERIMENTAL VALIDATION

The experimental validation has been conducted for the zero DC offset case using the setup shown in Fig. 8, with parameters listed in Table I. The load connected between the upper and lower DC rails case has been considered. A single interphase inductor is connected between the two legs of the secondary-side switches, replicating the equivalent behavior described in Section III-A.

Figs. 9 and 10 present the experimental waveforms of the converter operating without the interphase inductor. In Fig. 9, the top plot shows the primary and secondary side voltages v_a and v_b of the transformer, while the bottom plot displays the corresponding leakage inductor current i_L . A small phase shift of $d = 0.05$ is introduced between v_a and v_b , with the voltage gain of $G = 0.5$. Under these conditions, the absence of the interphase inductor results in the loss of ZVS on the output bridge.

Fig. 10 shows the drain-source voltage v_{ds} and gate-source voltage v_{gs} waveforms for a single switch on the primary side S_1 (top) and secondary side S_5 (bottom), respectively. Due to the symmetrical structure of the converter, only one switch per side is shown. It can be observed that the primary-side switch S_1 achieves ZVS, while the secondary-side switch S_5 fails to do so, as seen during the turn-on, the switch is exposed to maximum voltage V_o instead of zero voltage, which is clearly visible in Fig. 10 bottom zoomed plot. These results confirm the theoretical prediction that, under the given operating conditions, ZVS is not

TABLE I
EXPERIMENTAL SETUP PARAMETERS

Parameters	Symbol	Value	Unit
Input voltage	V_{dc}	200	V
Output voltage	V_o	100	V
Switching frequency	f_{sw}	100	kHz
Leakage inductor	L_d	81.7	μH
Voltage gain	G	0.5	-
Transformer turns ratio	k	1:1	-
Interphase inductor	$2L$	118.5	μH
Transformer magnetizing inductor	L_m	775	μH
Operating phase shift	d	0.05	-

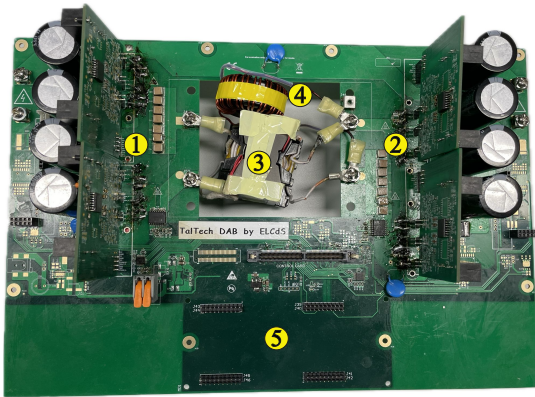


Fig. 8. Experimental setup of CF-DAB: (1) input bridge; (2) output bridge; (3) high-frequency transformer; (4) interphase inductor; (5) input pins for gate signals.

possible to achieve on the output bridge of a conventional DAB, particularly at light load.

Figs. 11 and 12 show the experimental results when an interphase inductor is introduced between the secondary-side legs. In Fig. 11, the top and middle plots display the primary

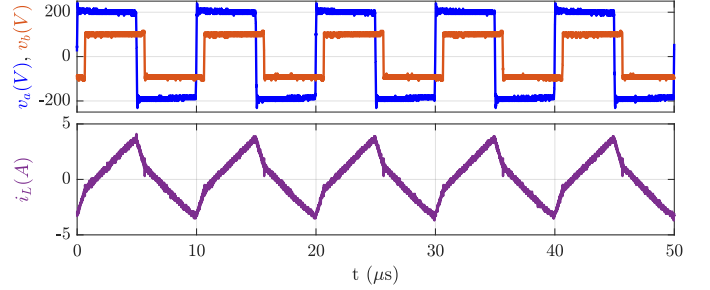


Fig. 9. Primary and secondary side voltages (top) and the leakage current (bottom) of the transformer in case of conventional DAB.

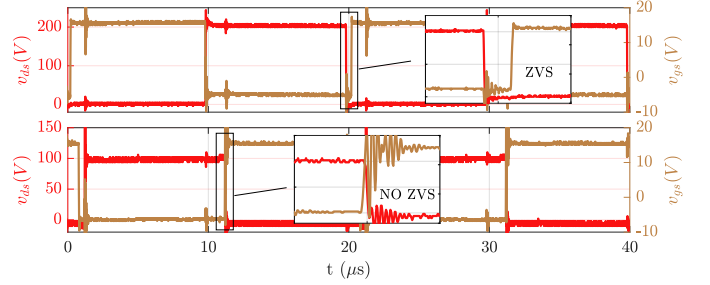


Fig. 10. Drain-source voltage and gate source voltage: primary side switch S_1 (top) and secondary side switch S_5 (bottom) in case of conventional DAB.

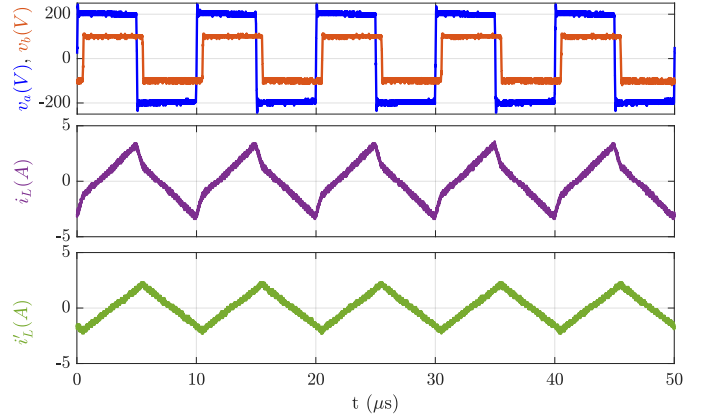


Fig. 11. Primary and secondary side voltages (top), leakage current (middle) of the transformer, and interphase inductor current (bottom).

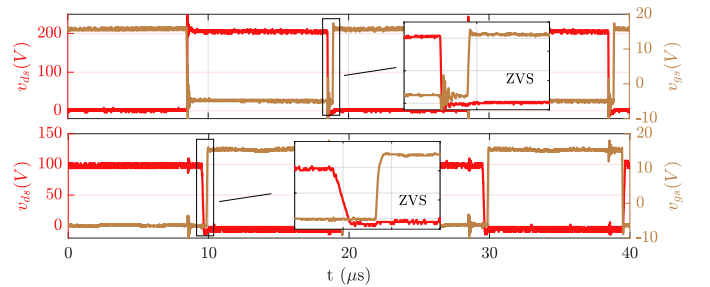


Fig. 12. Drain-source voltage and gate source voltage: primary side switch S_1 (top) and secondary side switch S_5 (bottom) in case of CF-DAB.

and secondary transformer voltages, v_a and v_b , along with the corresponding leakage inductor current i_L . The bottom plot presents the interphase inductor current i_L^i . The converter is operated under the same conditions as in the no-interphase case; however, the introduction of the interphase inductor introduces the design parameter β .

In practice, the magnetizing inductance L_m of the transformer appears in parallel with the interphase inductor $2L$, and those values are provided in Table I. As a result, the total equivalent inductance is calculated to be $102.7 \mu\text{H}$, leading to an effective $\beta = 1.25$, which satisfies the ZVS condition (7) for the output bridge operating under phase shift of $d = 0.05$ and voltage gain $G = 0.5$. The triangular shape of the interphase inductor current i_L^i confirms balanced operation with zero DC offset.

Fig. 12 displays the drain-source v_{ds} and gate-source v_{gs} voltages of the primary-side switch S_1 (top) and secondary-side switch S_5 (bottom). As seen in the zoomed view of the top plot, the input bridge continues to operate under ZVS, similar to the previous case. However, with the interphase inductor in place, ZVS is successfully achieved on the output bridge, as evidenced by the secondary-side switch S_5 turning on during the zero voltage. These results experimentally validate the theoretical analysis presented in Section III-A, confirming that the interphase inductor effectively extends the ZVS region on the output bridge.

V. CONCLUSION

This paper presented a comprehensive ZVS analysis of the CF-DAB converter operating under SPS control, with a focus on both bipolar and unipolar DC grid applications. A key contribution of this work is the recognition that the presence or absence of DC offset in the interphase inductors depends on the load configuration. Specifically, both bipolar and unipolar modes can exhibit either zero or nonzero DC offset, respectively, which significantly influences the ZVS behavior of the converter.

Analytical expressions were derived for the ZVS boundaries in both zero and nonzero offset cases. In the zero-offset case, a unified ZVS boundary is obtained, enabling full soft-switching depending on the inductor sizing parameter β . In contrast, when a DC offset is present, the ZVS boundary splits into two separate conditions for the upper and lower switches, resulting in only partial ZVS within a certain operating range. Experimental validation was conducted for the zero DC offset case, with the load connected between the upper and lower DC rails, confirming the theoretical predictions and demonstrating effective soft-switching.

However, the presence of interleaved inductors may increase the RMS current in the switches, leading to a trade-off between soft-switching and conduction losses. Future work will focus on optimizing the design to balance ZVS performance with efficiency. Moreover, experimental validation for the DC offset case will be conducted to complete the analysis.

REFERENCES

- [1] E. L. Carvalho, A. Blinov, A. Chub, P. Emiliani, G. de Carne, and D. Vinnikov, "Grid integration of dc buildings: Standards, requirements and power converter topologies," *IEEE OJ. Power Electron.*, vol. 3, pp. 798–823, 2022.
- [2] S. Fang, Y. Wang, B. Gou, and Y. Xu, "Toward future green maritime transportation: An overview of seaport microgrids and all-electric ships," *IEEE Trans. Vehicular Tech.*, vol. 69, no. 1, pp. 207–219, 2020.
- [3] H. Hussaini, T. Yang, Y. Gao, C. Wang, M. Urrutia, and S. Bozhko, "Optimal droop control design using artificial intelligent techniques for electric power systems of more-electric aircraft," *IEEE Trans. Transport. Elect.*, vol. 10, no. 1, pp. 2192–2206, 2024.
- [4] S. Rivera, R. Lizana F., S. Kouro, T. Dragičević, and B. Wu, "Bipolar dc power conversion: State-of-the-art and emerging technologies," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 2, pp. 1192–1204, 2021.
- [5] S. Cuoghi, R. Mandrioli, L. K. Pittala, V. Cirimele, and M. Ricco, "Dual-active-bridge model and control for supporting fast synthetic inertial action," *Energies*, vol. 15, no. 6, Mar. 2022.
- [6] Y. Yan, H. Gui, and H. Bai, "Complete zvs analysis in dual active bridge," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1247–1252, Feb. 2021.
- [7] J. Riedel, D. G. Holmes, B. P. McGrath, and C. Teixeira, "Maintaining continuous zvs operation of a dual active bridge by reduced coupling transformers," *IEEE Trans. Ind. Electron.*, vol. 65, no. 12, pp. 9438–9448, Dec. 2018.
- [8] S. Yin, S. Debnath, R. Wojda, P. Marthi, and M. Saeedifard, "Impact of the transformer magnetizing inductance on the performance of the dual-active bridge converter," in *Proc. IEEE 22nd Workshop Control Model. Power Electron.*, Nov. 2021, pp. 1–7.
- [9] X. Chen, G. Xu, H. Han, D. Liu, Y. Sun, and M. Su, "Light-load efficiency enhancement of high-frequency dual-active-bridge converter under sps control," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 12 941–12 946, Dec. 2021.
- [10] M. Kheraluwala, R. Gascoigne, D. Divan, and E. Baumann, "Performance characterization of a high-power dual active bridge dc-to-dc converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov.-Dec. 1992.
- [11] G. Xu, L. Li, X. Chen, W. Xiong, X. Liang, and M. Su, "Decoupled eps control utilizing magnetizing current to achieve full load range zvs for dual active bridge converters," *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 4801–4813, May 2022.
- [12] E. L. Carvalho, R. Cardoso, C. A. Felipe, C. M. De Oliveira Stein, L. V. Bellinaso, L. Michels, and D. Vinnikov, "Extended zvs-on/zcs-off range for cf-dab converter under dcm operation for residential energy storage systems," *IEEE Access*, vol. 11, pp. 119 231–119 243, 2023.
- [13] E. L. Carvalho, C. A. Felipe, L. V. Bellinaso, C. M. d. O. Stein, R. Cardoso, and L. Michels, "Asymmetrical-pwm dab converter with extended zvs/zcs range and reduced circulating current for ess applications," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12 990–13 001, 2021.
- [14] L. K. Pittala, R. Barbone, R. Mandrioli, V. Cirimele, M. Ricco, and G. Grandi, "Insights on dab converter with auxiliary inductors," in *Proc. Int. Conf. on Clean Electrical Power (ICCEP)*, 2023, pp. 458–463.
- [15] R. De Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, 1991.
- [16] E. L. Carvalho, R. Mandrioli, L. K. Pittala, A. Blinov, A. Chub, and D. Vinnikov, "Universal interlinking converter for prosumer dc buildings: Operation with different dc grid types," in *Proc. IEEE 7th Int. Conf. DC Microgrids (ICDCM)*, 2025, pp. 1–6.
- [17] E. L. Carvalho, R. Mandrioli, L. K. Pittala, I. Bianchini, A. Blinov, A. Chub, and D. Vinnikov, "Universal interlinking converter for prosumer dc buildings: Operation under normal and abnormal ac grid conditions," in *Proc. IEEE 7th Int. Conf. DC Microgrids (ICDCM)*, 2025, pp. 1–5.
- [18] F. Peng, H. Li, G.-J. Su, and J. Lawler, "A new zvs bidirectional dc-dc converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, 2004.
- [19] Y. Shi, R. Li, Y. Xue, and H. Li, "Optimized operation of current-fed dual active bridge dc-dc converter for pv applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6986–6995, 2015.
- [20] Q. Gu, B. Xie, R. Li, Z. Zhu, and Y. Zhang, "A zvs implementation method of a current-fed dual active bridge converter within the full load range," in *Proc. IEEE Appl. Power Electron. Conf. Exp. (APEC)*, 2024, pp. 2059–2062.
- [21] G. Xu, M. Zhang, X. Chen, L. Li, Z. Lu, and M. Su, "Dual-coupled-inductor-based dab dcx converter with full load range zvs," *IEEE Trans. Ind. Electron.*, vol. 72, no. 1, pp. 525–535, 2025.
- [22] D. Sha, X. Wang, and D. Chen, "High-efficiency current-fed dual active bridge dc-dc converter with zvs achievement throughout full range of load using optimized switching patterns," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1347–1357, 2018.