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Reliability Assessment of 650-V Schottky p-GaN HEMTs Under Reverse Conduction Stress

This is the final peer-reviewed author’s accepted manuscript (postprint) of the following publication:

Published Version:
Millesimo, M., Fiegna, C., Smerzi, S.A., Iucolano, F., Cioni, M., Russo, A., et al. (2025). Reliability Assessment of 650-V Schottky p-GaN HEMTs Under Reverse Conduction Stress. IEEE TRANSACTIONS ON ELECTRON DEVICES, 72(8), 4259-4266 [10.1109/TED.2025.3579457].

Availability:
This version is available at: https://hdl.handle.net/11585/1032555 since: 2025-12-15

Published:
DOI: http://doi.org/10.1109/TED.2025.3579457

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(Article begins on next page)

09 July 2026

This is the post-print peer-review accepted manuscript of:

M. Millesimo *et al.*, "Reliability Assessment of 650V Schottky pGaN HEMTs Under Reverse Conduction Stress," *IEEE Transactions on Electron Devices*, Vol. 72, No. 8, pp. 4259-4266, August 2025, DOI: 10.1109/TED.2025.3579457.

The published version is available online at:

https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=11043139

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Reliability Assessment of 650V Schottky pGaN HEMTs Under Reverse Conduction Stress

M. Millesimo, C. Fiegna, S. A. Smerzi, F. Iucolano, M. Cioni, A. Russo, S. Bevilacqua, A. N. Tallarico, *Senior Member, IEEE*

***Abstract*— GaN-based high-electron mobility transistors (HEMTs) can operate efficiently in reverse conduction mode without requiring an intrinsic antiparallel diode, reducing power losses and enabling higher switching frequencies. This study investigates degradation mechanisms in Schottky p-GaN gate HEMTs (SP-HEMTs) under reverse conduction mode on devices featuring different gate geometries. It assesses threshold voltage shift (ΔV_{TH}), on-resistance drift (ΔR_{ON}), and device lifetime across a range of temperatures (10 °C to 175 °C) and negative drain-to-source voltages (V_{DS}). Results reveal two distinct degradation mechanisms: the first occurring in the AlGaN barrier at the source-side gate edge, and a second, a long-term process at the metal/p-GaN Schottky junction, which leads to irreversible breakdown. Activation energy for both mechanisms has been determined using current deep-level transient spectroscopy (I-DLTS), providing insights into the temperature and voltage dependencies of mechanisms affecting SP-HEMTs reliability.**

***Index Terms*— degradation mechanisms, reliability, Schottky pGaN high-electron mobility transistors (HEMTs), reverse conduction mode.**

I. INTRODUCTION

GAN-BASED HEMTs have shown significant potential to penetrate the field of power electronics, positioning themselves as a promising alternative to traditional Silicon-based devices [1]-[3]. The remarkable electrical properties of GaN, associated with those of the AlGaN/GaN heterojunction, enable the fabrication of power devices with significant performance advantages, particularly in high-power and high-frequency applications. A key advantage of this technology is its intrinsic ability to operate in reverse conduction mode without requiring a freewheeling diode [4]. This conduction regime is also referred as self-commutating reverse conduction (SCRC) [5]. The absence of the intrinsic antiparallel diode reduces power losses due to absence of reverse recovery charge, and minimizes parasitic output capacitance, thus enabling faster switching operation [5]-[6].

This feature is especially advantageous in power converters

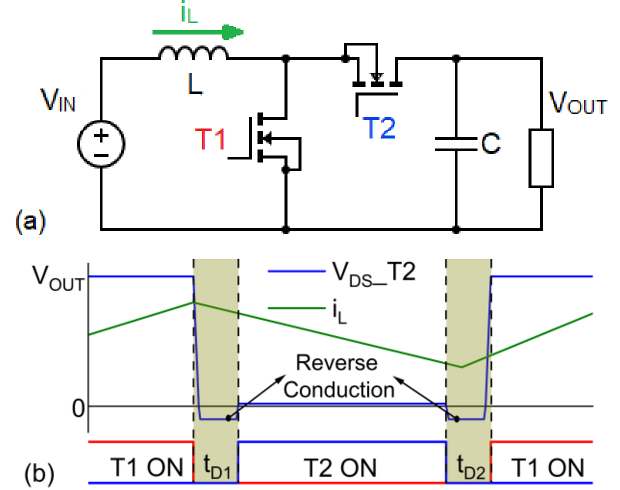

Fig. 1. (a) Schematic of a synchronous DC/DC boost converter, and (b) typical current/voltage waveforms experienced by the switch T2, which operates in reverse conduction mode during the dead times t_{D1} and t_{D2}.

based on hard-switching topology, such as DC/DC boost converters (Fig. 1 (a)). For instance, during the dead time t_{D1}, when the transistor T1 turns off, the energy stored in the inductor forces the current to flow in the reverse direction (from source to drain) through the secondary switch (T2) (Fig. 1b), placing T2 in reverse conduction mode, i.e. with gate-to-source voltage (V_{GS}) lower than threshold voltage (V_{TH}) and negative drain-to-source voltage (V_{DS}). The same phenomenon occurs when T2 switches off (t_{D2}), forcing the device to sustain high surge inductor current resulting in a relatively high negative V_{DS} and, consequently, high gate-to-drain voltage (V_{GD}) [7].

The mechanisms enabling the reverse conduction operation of Schottky p-GaN gate HEMTs have been explored through TCAD simulations [8]. Under a relatively small negative V_{DS}, the V_{GD} remains lower than V_{TH}, the P-i-N (pGaN/AlGaN/GaN) diode is pushed into forward operation, while the Schottky/p-GaN diode prevents hole injection from the metal into the pGaN valence band (i.e. electrons from the pGaN valence band to the metal). At higher negative V_{DS} values ($V_{GD} > V_{TH}$), the gate Schottky diode becomes increasingly

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This research was funded by the European Union–NextGenerationEU, within the framework of the Italian National Recovery and Resilience Plan (PNRR), Mission 4, Component 2, Investment 1.4, under Project CN00000023 “Sustainable Mobility Center (MOST)”. The views and opinions expressed are solely those of the authors and do not necessarily reflect those of the European Union or the European Commission, which cannot be held responsible for them.

reverse-biased, leaking holes that increase the two-dimensional hole gas (2DHG) density, which, in turn, leads to the formation of the two-dimensional electron gas (2DEG) under the gate region.

Although extensive research has focused on the reliability of Schottky p-GaN gate HEMTs under various conditions [9], few studies have investigated the reliability and stability of such devices in reverse conduction mode [5]-[8], [10]-[11], even though this analysis is essential for defining the safe operating area (SOA) of SP-HEMTs in power electronics applications under reverse conduction mode.

Recent findings [11], using TCAD simulation, have demonstrated that the reverse conduction regime induces an electric field peak in the AlGaN barrier at the source-side gate edge, which increases with negative V_{DS} but remains below AlGaN's critical field. The highest electric field, however, is observed at the Schottky/p-GaN interface, identifying this region as the most vulnerable to damage and breakdown under reverse conduction mode.

In [8], a fully recoverable positive threshold voltage shift is reported in the case of devices stressed with V_{DS} = -5.5 V and V_{GS} = 0 V (reverse conduction mode) at T = 150 °C. Additionally, time-dependent breakdown (TDB) analysis under various negative V_{DS} conditions revealed Weibull-distributed time-to-failure (TTF) values, allowing for device lifetime estimation.

This study presents a comprehensive reliability analysis of p-GaN gate HEMTs under reverse conduction mode, identifying degradation mechanisms that impact key transistor parameters, including threshold voltage, on-resistance (R_{ON}), and device lifetime. The analysis has been carried out over a wide temperature range (10 °C to 175 °C) and varying negative V_{DS} conditions (-17 V to -20 V) on devices with different gate geometries. Finally, current deep-level transient spectroscopy (I-DLTS) has been employed to determine the activation energy of degradation mechanisms affecting SP-HEMTs under reverse conduction mode.

II. Experimental Details

The devices under test (DUTs) are 650 V Schottky p-GaN gate HEMTs featuring a 10 fingers layout, a gate length (L_G) of 1.4 µm, and total gate widths (W_G) of 1 mm, 2 mm, 4 mm, and 8 mm, obtained by adjusting the gate width per finger accordingly. Figure 2(a) and (b) illustrate the typical I_D–V_{DS} and I_G–V_{DS} characteristics, respectively, under reverse drain-to-source voltage at V_{GS} = 0 V for all four gate geometries explored in this study.

The DUTs degradation under reverse conduction mode, in terms of ΔV_{TH} and ΔR_{ON}, has been experimentally assessed using the typical constant-voltage stress (CVS) and adopting the conventional measure/stress/measure (MSM) technique. During the stress phase, V_{DS} is forced at -19 V, V_{GS} = 0 V, while the substrate is grounded. The stress is periodically interrupted to monitor gate leakage (I_G), V_{TH} and R_{ON} drift by measuring the $I_D(I_G)$-V_G characteristics, sweeping V_{GS} from -6 V to 6 V with V_{DS} = 100 mV. V_{TH} is then extrapolated at a fixed drain

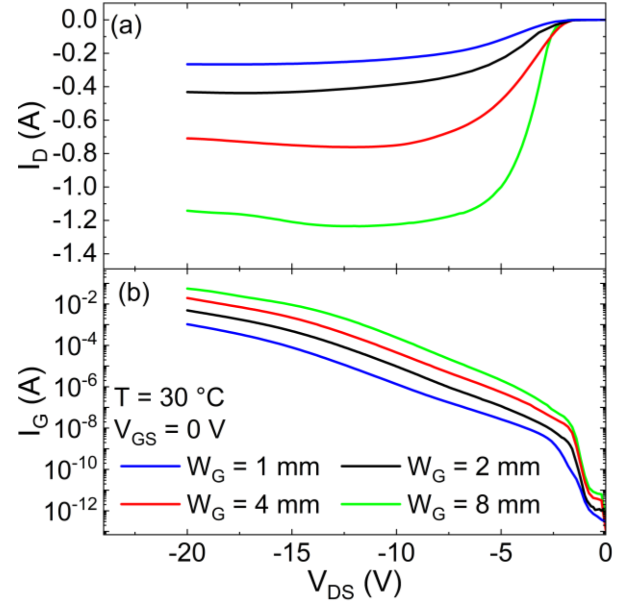

Fig. 2. I_D-V_{DS} (a) and I_G-V_{DS} (b) characteristic in reverse conduction mode (V_{GS} = 0V and negative V_{DS}) for devices with different W_G at T = 30 °C.

current level of 0.1 mA/mm, while R_{ON} is calculated at a gate overdrive voltage (V_{GS} - V_{TH}) of 3 V to separate the contribution of ΔV_{TH} from ΔR_{ON}. In this way, ΔR_{ON} can be purely ascribed to degradation phenomena occurring along the access regions of the power transistor. For each stress condition or device geometry, four devices have been tested, and the results in Section III represent the corresponding arithmetic mean.

To assess the TDB (or TTF) in reverse conduction mode, the gate leakage I_G is monitored by means of the on-the-fly (OTF) technique. This method involves stressing the devices with a relatively high negative V_{DS} (e.g., -19 V) and V_{GS} = 0 V, interrupting the stress every 5 seconds to monitor I_G in the ON-state (i.e., V_{GS} = 5 V and V_{DS} = 0 V) for 100 ms. The TTF is defined as the time at which I_G during the 100 ms ON-state characterization exceeds a specified threshold current of 1 mA/mm. Figs. 3(a) and 3(b) show I_G monitored during the reverse conduction stress phase (V_{DS} = -19 V, V_{GS} = 0 V) using the CVS test. In Fig. 3(a), the CVS test is performed without interruption, while in Fig. 3(b), the test is periodically interrupted to conduct I_G measurements at V_{GS} = 5 V (Fig. 3(c)) using the OTF technique. The tests have been conducted at T = 150 °C on DUTs with W_G = 4 mm. Notably, interrupting the stress phase every 5 s for 100 ms (OTF) does not impact the gate current dynamics (Fig. 3(b)), thus excluding any potential recovery mechanism. The OTF technique is required because, under negative V_{DS} (V_{GS} = 0 V), I_G is much higher than in the ON-state (V_{GS} = 5 V, V_{DS} = 0.1 V), therefore, it is rather insensitive to variations associated to localized breakdown spots, and thus, it is unsuitable for failure analysis. Notably, even after (localized) gate breakdown (Fig. 3(c)), the device can still operate in reverse conduction mode without experiencing an uncontrollable increase in current (Fig. 3(b)). A more detailed TDB analysis is presented in Section IV.

Finally, deep-level transient spectroscopy accounting for the gate leakage dynamics during reverse conduction stress has

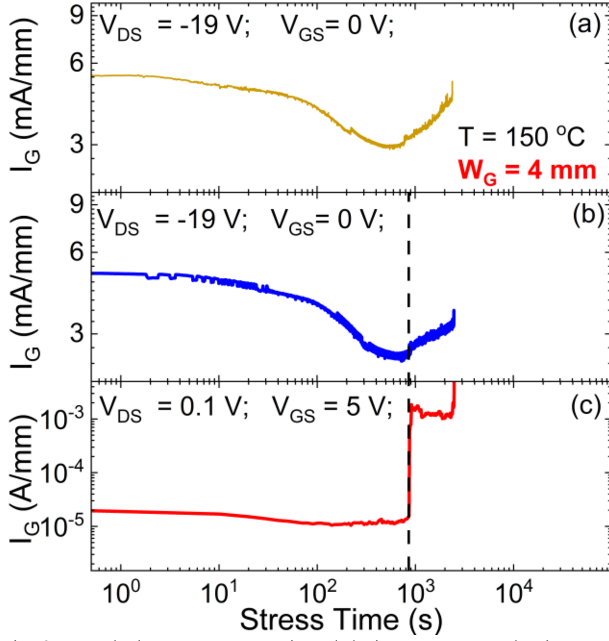

Fig. 3. Gate leakage current monitored during reverse conduction stress phase using the CVS test: (a) without interruption and (b) with the OTF approach. (c) Reports I_G monitored during the 100 ms ON-state characterization (OTF), repeated every 5 s of reverse conduction stress reported in (b). The DUTs feature $W_G = 4$ mm and the test temperature is 150 °C.

been performed to determine the activation energy associated with physical mechanisms responsible for stress-induced gate degradation. Details and results of the analysis are provided in Section V.

III. Device Performance Degradation Analysis

Figure 4 shows the I_G-V_{GS} characteristics of a device with $W_G = 4$ mm in its initial state (fresh), and after 3 s and 1 ks of stress at V_{DS} = - 19 V and T = 150 °C. Notably, after 3 s of stress, the gate leakage at negative V_{GS} (-6 V) is increased by approximately three orders of magnitude, while for positive V_{GS}, it remains almost unaffected. This suggests degradation of the AlGaN barrier, potentially due to defect creation and/or

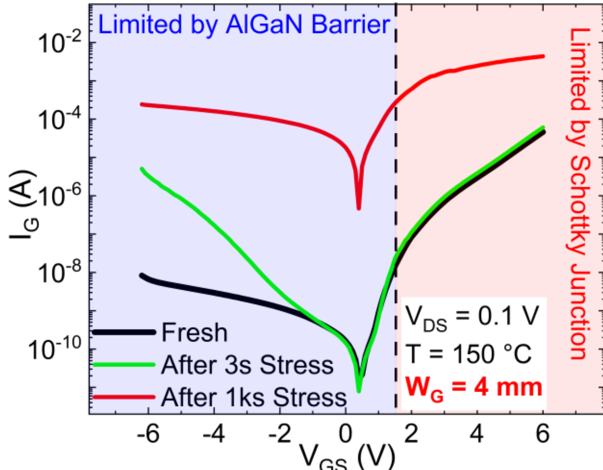

Fig. 4. I_G–V_{GS} characteristic for fresh device (black line), after 3 s of stress (green line), and after 1 ks of stress (red line). The reverse conduction stress phase is performed with $V_{DS} = -19$ V and $V_{GS} = 0$ V

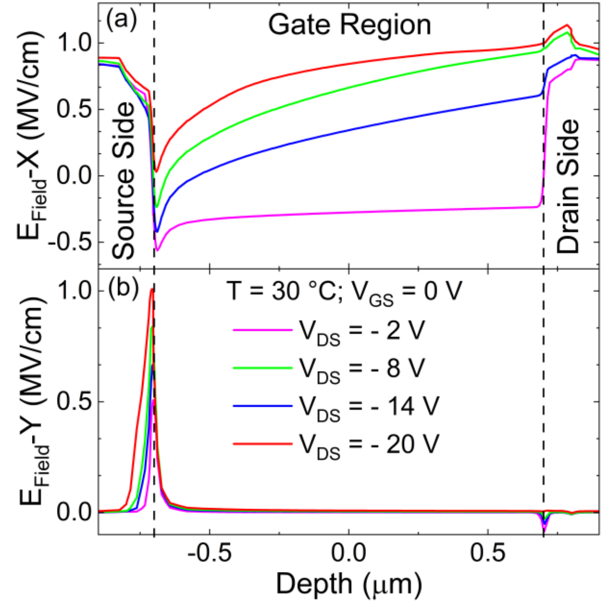

Fig. 5. TCAD simulated X- (a) and Y-component (b) of the electric field monitored at the interface between the GaN channel region and the AlGaN barrier at $V_{DS} = -2$ V, -8 V, -14 V, and -20 V, with $V_{GS} = 0$ V.

charge trapping. For $V_{GS} < 0$ V, I_G is mainly limited by trap-assisted tunneling (TAT) of electrons through the AlGaN barrier [12]. In this bias condition, the channel (2DEG) under the gate region is not formed (enhancement-mode), so I_G is ascribed to an edge component, i.e., electrons tunneling through the AlGaN barrier from the 2DEG of the access regions to the p-GaN layer, eventually reaching the gate metal [13]. Furthermore, the results obtained from TCAD simulations, as illustrated in Fig. 5, reveal the presence of a pronounced electric field peak at the source-side gate edge of the AlGaN/GaN interface when the device operates in reverse conduction mode. This observation is consistent with previously reported findings in [11], further corroborating the existence of such a phenomenon. Consequently, the combination of this localized electric field and the experimentally observed increase in gate leakage current for $V_{GS} < 0$ V (depicted by the green curve in Fig. 4) strongly indicates an edge-localized degradation of the AlGaN barrier.

Observing I_G after 1 ks of stress reveals an increase in current even for $V_{GS} > V_{TH}$. In this regime, the channel is formed, the metal/p-GaN Schottky diode is reverse-biased, and the p-i-n diode is forward-biased, making the gate leakage area-dependent. This observation suggests that, at longer stress times, defects creation within the Schottky junction depletion region may occur. As sufficient defects accumulate, forming a percolation path, the reverse-biased Schottky junction loses its insulating properties, leading to device failure.

Figures 6(a) and 6(b) show the gate leakage current, normalized with respect to fresh value ($I_{GN} = I_{Gi}/I_{G0}$), measured after each stress phase. The measurements were obtained using the MSM approach, which involves a fully I-V characterization from V_{GS} = -6 V to V_{GS} = +6 V. In Fig. 6(a), the current is measured at V_{GS} = 5 V, while in Fig. 6(b), it is measured at V_{GS} = -6 V. These values represent the bias conditions in which the

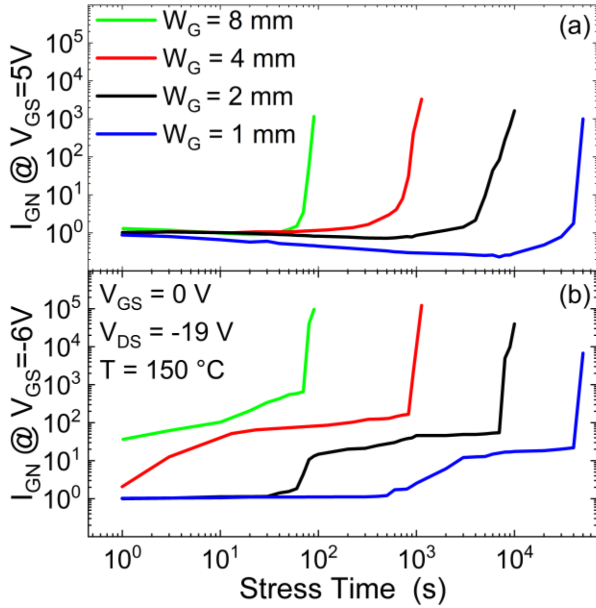

Fig. 6. Gate leakage, normalized with respect to the fresh value, monitored with (a) $V_{GS} = 5$ V and (b) $V_{GS} = -6$ V over the stress time. Results are shown for devices featuring W_G of 1 mm (blue line), 2 mm (black line), 4 mm (red line) and 8 mm (green line). The test temperature is 150 °C.

gate leakage is driven by the Schottky junction and the AlGaN barrier, respectively. Tests have been performed at 150 °C on devices with different gate widths: 1 mm (blue), 2 mm (black), 4 mm (red), and 8 mm (green). Notably, the wider W_G, the shorter the time at which both I_{GN} (at 5 V and -6 V) increase. Moreover, for all W_G values, I_{GN} at $V_{GS} = -6$ V starts increasing before it does at $V_{GS} = 5$ V, suggesting that degradation of the AlGaN barrier precedes that of the Schottky junction. Although both I_{GN} components exhibit W_G-dependent behavior, consideration of the electric field distribution in reverse conduction mode (Fig. 5) indicates that the AlGaN barrier (I_G @ $V_{GS} = -6$ V) experiences degradation primarily at the source-side gate edge, where an electric field peak appears. With increasing W_G, the gate edge lengthens, increasing the likelihood of degradation. Conversely, in the case of I_G increase associated with the Schottky junction (I_G @ $V_{GS} = 5$ V), edge- or area- degradation might occur, although TCAD simulations reveal a nearly uniform high electric field along the metal/pGaN interface [11]. Further considerations on this aspect are discussed in Section IV.

Same tests have been performed at temperatures ranging from 40 °C to 150 °C on devices with $W_G = 2$ mm. The I_{GN} at $V_{GS} = 5$ V and at $V_{GS} = -6$ V over stress time, as a function of T, are shown in Figs. 7(a) and 7(b), respectively. For all tested temperatures, an increase in gate leakage limited by the AlGaN barrier is observed prior to the increase limited by the Schottky junction. I_{GN} at $V_{GS} = -6$ V shows T-dependence, with higher T leading to a shorter time at which the gate leakage increases, emphasizing the role of thermal energy in the degradation process. Conversely, no clear temperature dependency is observed for I_{GN} monitored at $V_{GS} = 5$ V, possibly due to the MSM technique, which requires a relatively long measurement phase (~ 5 s), allowing for possible temperature-dependent recovery mechanisms. The T-dependency of the time-dependent Schottky junction breakdown will be further analyzed in section IV using the OTF technique.

In Figs. 8(a) and 8(b), the ΔR_{ON} and ΔV_{TH} induced by reverse conduction stress are reported as functions of T, extracted from the measurements of Fig. 7. Notably, after an initial drift, ascribed to temperature-dependent charge trapping in pre-existing defects, R_{ON} shows no significant degradation over stress time for all tested T, suggesting that reverse conduction mode produces negligible degradation in the access regions of the power transistor.

In the case of ΔV_{TH}, three distinct phases are observed in Fig.

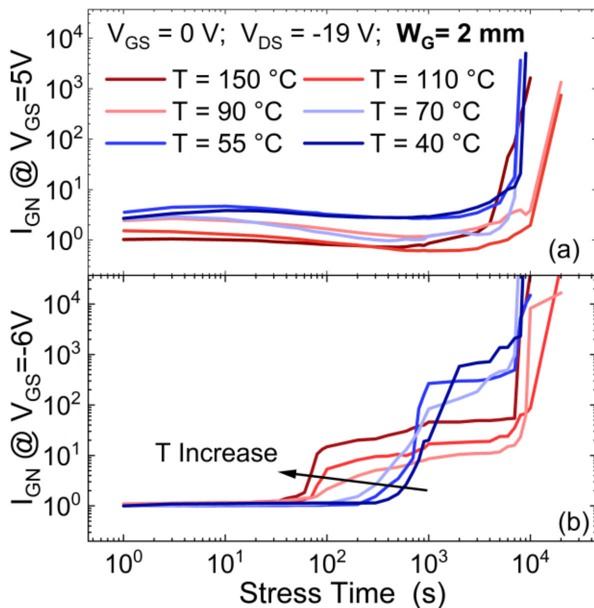

Fig. 7. Gate leakage, normalized with respect to the fresh value, monitored at (a) $V_{GS} = 5$ V and (b) $V_{GS} = -6$ V over the stress time. The DUTs feature with $W_G = 2$ mm and the temperature ranges from 40 °C to 150 °C.

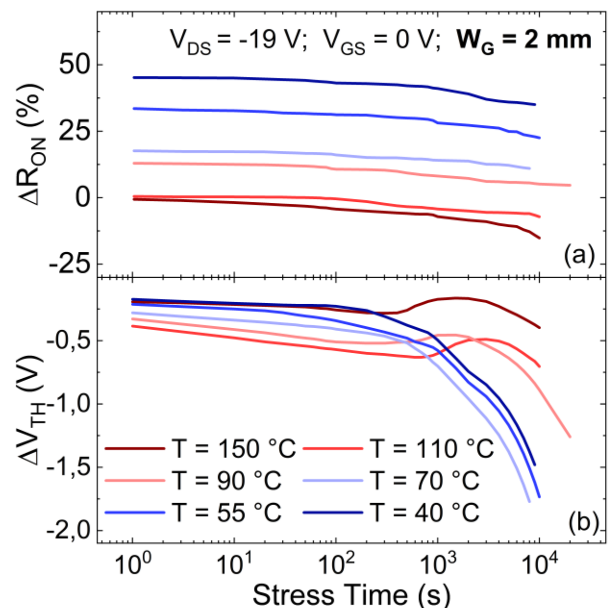

Fig. 8. (a) ON-resistance and (b) threshold voltage shift over the stress time, as a function of different temperatures. The DUTs feature a $W_G = 2$ mm and the stress phase is performed with $V_{DS} = -19$ V and $V_{GS} = 0$ V.

8(b): (i) an initial small, nearly T-independent, negative shift; (ii) a positive ΔV_{TH} for T > 90 °C; and (iii) a final large negative shift observed for all T. The temperature and stress-time dependence reported in phase (i) and (ii) are consistent with those reported under forward bias gate stress [14]. Specifically, phase (i) is attributed to hole trapping in pre-existing defects near the valence band within the AlGaN barrier, where holes from the 2DHG are trapped via temperature-independent elastic tunneling. The positive ΔV_{TH} shift in phase (ii) is associated to electron (from 2DEG) trapping in newly created defects in the AlGaN barrier. Here, holes generated by impact ionization in the high-field depletion region of the Schottky junction are accelerated, acquiring kinetic energy, toward the AlGaN barrier, releasing their energy to the lattice, which, combined to phonons energy, can induce defects creation. In particular, as the temperature increases, less energy is required to create or activate a defect. Therefore, although the energy of hot holes decreases at higher temperatures due to increased energy dissipation through hole-phonon scattering, the energy released can still be sufficient to create a defect in the AlGaN barrier [14]. In contrast, at lower temperatures, a higher energy, possibly beyond what can be provided by hot holes alone, is required. Finally, phase (iii) corresponds to defects creation in the Schottky junction depletion region, supported by the increased gate leakage limited by the Schottky junction (Fig. 7(a)). As reported in [15], a leaky Schottky junction in p-GaN HEMTs reduces the threshold voltage. Degradation of the Schottky junction facilitates hole injection from the metal into the 2DHG, increasing 2DEG density and reducing V_{TH}. These findings suggest that the physical mechanisms underlying ΔV_{TH} in p-GaN HEMTs under reverse conduction mode are similar to those occurring under forward gate stress.

IV. Time-Dependent breakdown Analysis

Time-dependent breakdown tests using the OTF technique have been performed at various negative V_{DS} and T = 150 °C on devices with different W_G. The Weibull distributions of the TTF values are shown in Figs. 9 (a), (b), (c) and (d) for devices with W_G of 8 mm, 4 mm, 2 mm and 1 mm, respectively. The shape parameter (β) of the Weibull distribution is similar (~2.5) for all tested V_{DS} and W_G. Additionally, the same tests have been carried out at T = 40 °C on devices with W_G = 4 mm, with the corresponding Weibull plot shown in Fig.10. In this case, β is slightly higher (~3.2) compared to the case at T = 150 °C. Since β > 1 independently of T, this indicates wear-out mechanisms leading to TDB. From the Weibull plots, TTF values corresponding to a 1% failure rate (i.e., 1% of devices failed) have been extracted to generate the lifetime plot, as illustrated in Fig 11. The field-accelerated model used to fit the relationship between TTF and V_{DS} data follows the E-model, i.e., exponential, a model commonly applied to area-dependent gate breakdown in p-GaN HEMTs [16]-[17]. The gate lifetime shows a clear dependence on W_G, with wider gate structures exhibiting shorter lifetimes (or smaller absolute V_{DS} values at 10-year lifetime). In particular, the maximum negative V_{DS} that ensures a 10-year lifetime is -11.5 V, -9 V, -7,5 and -6V for

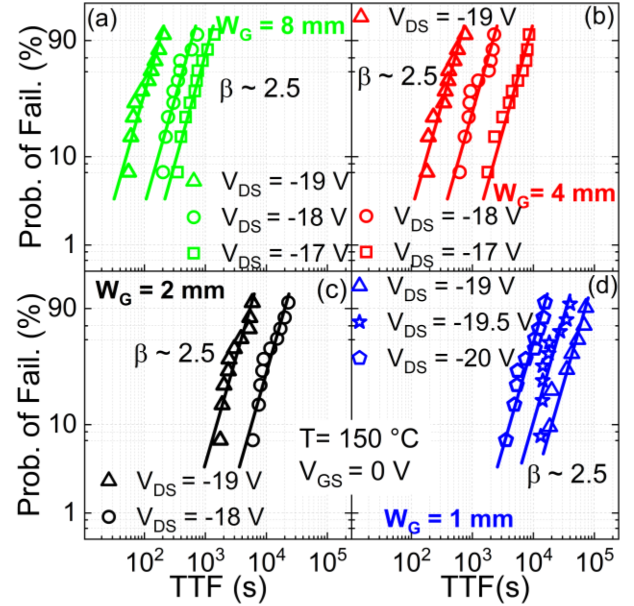

Fig. 9. Weibull plot of the Time-to-Failure values at different V_{DS} stress in the case of devices featuring W_G of (a) 8 mm, (b) 4 mm, (c) 2 mm and (d) 1 mm. The test temperature is 150 °C using OTF approach.

devices featuring W_G of 1 mm, 2 mm, 4 mm and 8 mm, respectively. It is worth highlighting that edge- or area-dependent failure mechanisms in Schottky pGaN gate HEMTs also occur under forward gate bias stress [17]. The gate lifetime shows a negative T-dependence: the lower T, the longer gate lifetime. This contrasts with studies on area-dependent breakdown in Schottky junctions under gate forward stress[16], where impact ionization in the high-field depleted region drives defect creation, and higher temperatures, by suppressing hot-carrier effects, delay irreversible gate failure. The opposite T-dependence found here, suggests that, in the case of reverse conduction stressing, breakdown may occur in the device perimeter or that impact ionization plays a limited role in the failure process. Moreover, as discussed in Section III, the temperature-dependent degradation of the AlGaN barrier (which is negative) precedes that of the Schottky junction. As the temperature increases, the insulating properies of the

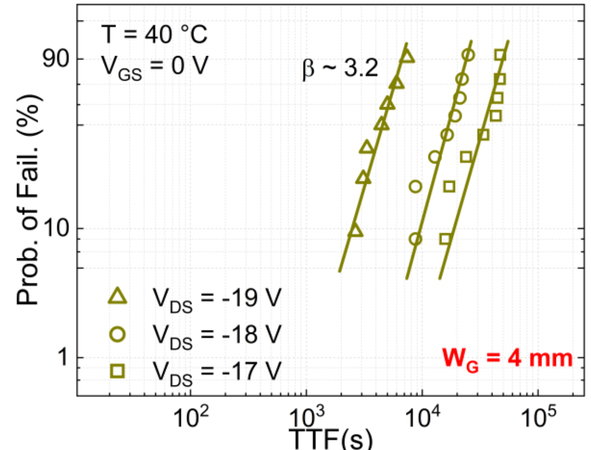

Fig. 10. Weibull plot of the Time-to-Failure values at different V_{DS} stress in the case of devices featuring W_G = 4 mm. The test temperature is 40 °C, the OTF approach has been used.

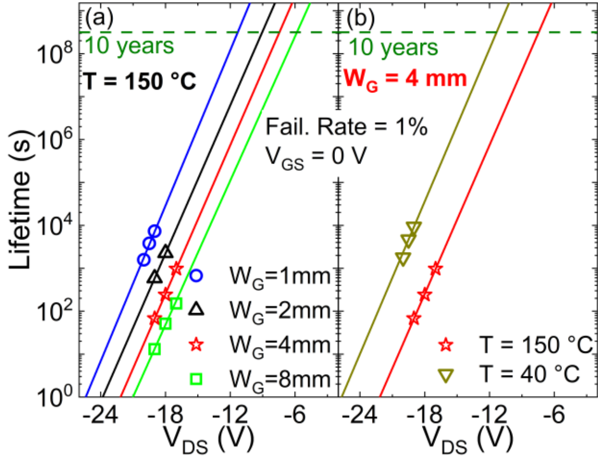

Fig. 11. (a) Lifetime plot of devices featuring different W_G at T = 150 °C. (b) Lifetime plot of devices with W_G = 4 mm in the case of T=150 °C and T = 40 °C. The TTF values are extrapolated from Weibull plots considering a failure rate of 1%.

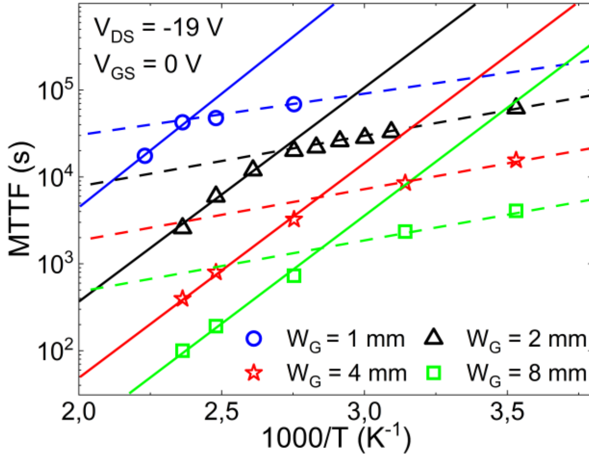

Fig. 12. Temperature dependence (1000/T) of the Mean Time-to-Failure in the case of devices featuring W_G: 8mm (green), 4 mm (red), 2 mm (black) and 1 mm (blue).

AlGaN barrier degrade more quickly (Fig. 6 (b)), facilitating the injection of charge carriers from the 2DEG into the p-GaN region. This, in turn, may contribute to the irreversible breakdown of the Schottky junction. Further analyis based on electron microscopy is needed to spatially locate the damage.

To further investigate the T-dependence of TTF, tests have been conducted at V_{DS} = -19 V across a temperature range from 10 °C to 175 °C on devices with different W_G. The mean time-to-failure (MTTF) is plotted against the inverse of the temperature in Fig 12. MTTF is calculated as the arithmetic mean of the TTF values from 10 devices. Notably, W_G-dependence is consistently observed across all temperatures. Moreover, two distinct temperature dependencies are identified: a stronger dependence at higher T and a weaker dependence at lower T. The underlying reasons for this behavior are discussed in section V.

V. Current Deep-Level Transient Spectroscopy

Fig. 13 presents the gate current monitored during the reverse conduction stress phase, normalized to the final measured value prior to breakdown, for several devices with W_G = 4 mm and T = 10 °C. Two distinct transient behaviors can be observed: an initial increasing trend followed by a decreasing one. For clarity, the faster (first) current transient and the slower (second) one will be referred to as CT1 and CT2, respectively. Current transients related to charging/discharging and/or trapping/detrapping processes are typically modeled as a sum of stretched exponential functions (one for each transient), described by the following equation [18]:

$$I_{fit}(t) = 1 + \sum_{i=1}^{N} f_i(t) = 1 + \sum_{i=1}^{N} A_i e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \quad (1)$$

where N=2 in this case, A_i is the transient amplitude, which corresponds to the amount of stored or released charge; τ_i is the charge capture or emission time constant; and β_i is a stretching factor defining the slope of the transient. Accurate estimation of these parameters provides valuable insights into the underlying physical mechanisms driving the current transients. However, when multiple transients are close to each other (with similar τ values), their interactions can lead to inaccuracies in parameters estimation. To address this issue, a mathematical approach based on the analysis of the derivative, combined with a genetic algorithm to minimize the mean square error of the fitting law, was proposed in [18]. In this work, the same methodology has been applied to model current transients across the explored temperature range (from 10 °C to 175 °C) for devices with varying gate widths. As shown in Fig. 13, the approach effectively reproduces the measured current behavior. To mitigate potential data dispersion, for each temperature and device geometry, the stretched exponential used in the analysis is derived from the arithmetic mean of the parameters extracted from multiple device currents (blue line in Fig. 13).

Figures 14 (a), (b), (c) and (d) show the results of the transient modeling at different temperatures for devices with W_G of 8 mm, 4 mm, 2 mm and 1 mm, respectively. It is worth noting that both transients show clear temperature dependence, suggesting the presence of thermally activated physical processes. The stretching parameters and amplitudes of both transients (reported in Fig. 15 (a) and (b), respectively) exhibit

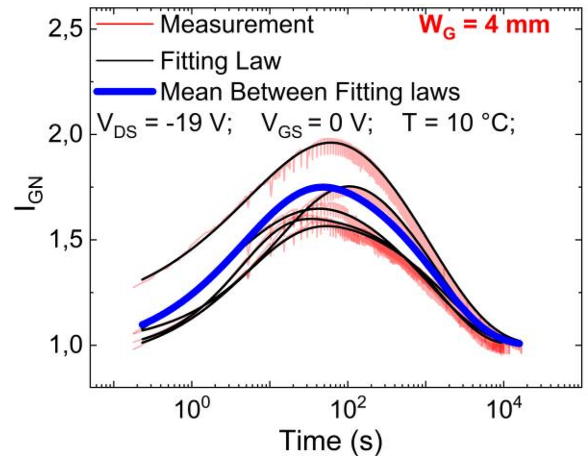

Fig. 13. Normalized I_G monitored during the reverse conduction stress phase (red lines) for several devices with W_G = 4 mm and T = 10°C. The red lines represent the experiments, the black ones the corresponding fitting, while the blue one is reconstructed by considering the mean value of each fitting parameter derived from the black curves.

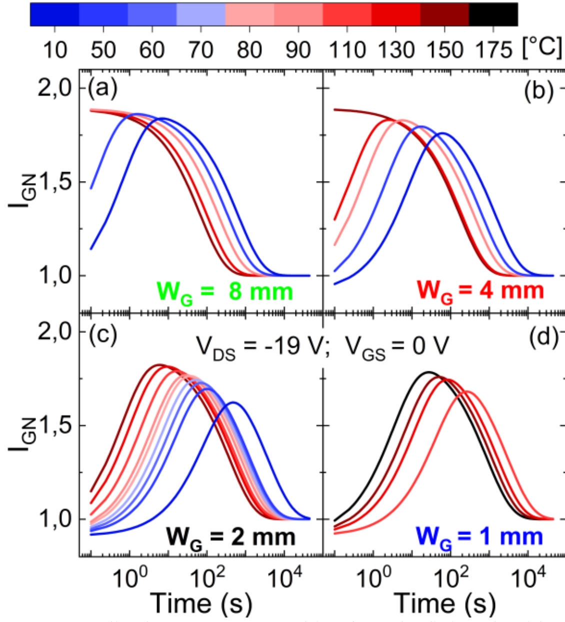

Fig. 14. Normalized gate current, resulting from the fitting algorithm, at different temperatures for devices featuring W_G of (a) 8mm, (b) 4mm, (c) 2 mm and (d) 1 mm.

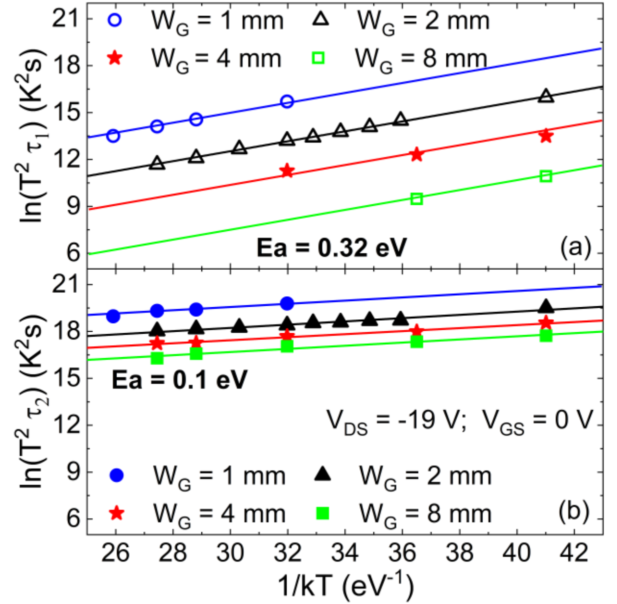

Fig. 16. Arrhenius plot of the characteristics time constants of the physical mechanisms underneath (a) CT1 and (b) CT2.

no dependence neither on T nor on W_G. In contrast, the time constants τ_1 and τ_2, corresponding to the CT1 and CT2, respectively, show clear dependencies on both temperature and W_G, as illustrated by the Arrhenius plots in Fig. 16. Notably, the observed dependence on W_G suggests a correlation with defect generation mechanisms rather than with the intrinsic properties of the traps themselves, as the characteristic traps time, i.e., the time associated with charge trapping and detrapping, is generally independent of gate edge length or area. However, defect generation is highly sensitive to the initial defectivity of the material. As the gate area increases, the probability of having regions with a higher concentration of pre-existing defects also increases, thereby reducing the time required for additional defect generation. This facilitates the formation of percolation paths through the interaction between newly generated and pre-existing defects. Such behavior is consistent with the well-established observation that time-to-failure decreases with increasing device area, as predicted by percolation theory [19]. Through this analysis, the activation energy of the degradation processes occurring under reverse conduction has been determined. In particular, CT1 exhibits an activation energy of 320 meV (Fig. 16 (a)), which can be attributed to defects-related processes in the AlGaN barrier layer [20]. This correlation is supported by our findings, where, as shown in Fig. 6(b), the gate leakage component related to the AlGaN layer is the first parameter to degrade. Notably, CT1 is absent at T = 150 °C for devices with W_G values of 8 mm and 4 mm (Figs. 14 a and b, respectively), as the gate current driven by the AlGaN barrier has already increased after 1 s of stress. To observe CT1 in devices with W_G of 8 mm and 4 mm, either a lower temperature or a shorter sampling time (in the microsecond range) is required. On the other hand, CT2 features an activation energy of 100 meV (Fig. 16 (b)), which can be associated with Nitrogen vacancies in Mg-doped GaN layers [21]. As a result, the activation energy supports defects creation in the Schottky depletion region (Mg-doped GaN).

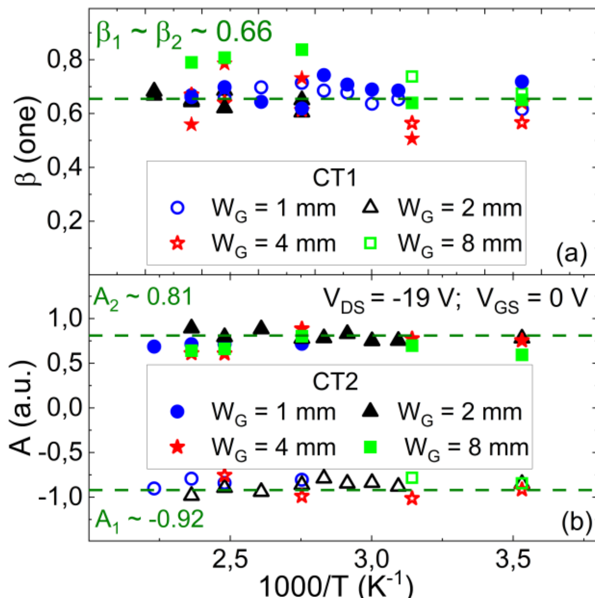

Fig. 15. Temperature dependence of the (a) stretching parameter β and (b) amplitude A for the two current transients CT1 and CT2.

Due to the higher activation energy (major temperature dependence) of CT1 compared to CT2, the transient responses of the two become closer to each other at lower temperatures, i.e., the difference between their respective time constants is reduced. Consequently, the two current transients begin to interact, leading to a reduction of the transient peak, as illustrated in Fig. 14. This interaction likely contributes to the observed alteration in the temperature dependence of the MTTF (Fig. 12), potentially attributable to the varying influences of these competing mechanisms on the final gate failure.

VI. Conclusions

This study provides a detailed analysis of the degradation mechanisms in Schottky p-GaN gate HEMTs under reverse conduction mode, focusing on the effects of temperature, gate geometry, and applied drain-to-source voltage. Results revealed two distinct degradation processes, each correlated with specific structural regions of the device gate. The initial degradation occurs at the source-side gate edge within the AlGaN barrier and is driven by a localized electric field peak. Prolonged stress leads to defect formation at the metal/p-GaN Schottky junction, resulting in irreversible time-dependent breakdown.

The application of current deep-level transient spectroscopy (I-DLTS) enabled the identification of thermally activated degradation processes, with activation energies suggesting defect formation in the AlGaN layer and nitrogen vacancies in Mg-doped P-GaN layer.

The time-dependent breakdown analysis further confirms that device lifetime is significantly affected by temperature and gate width, demonstrating an W_G-dependent failure mechanism linked to breakdown at the Schottky junction. Moreover, it has been demonstrated that reverse conduction conditions do not significantly affect the on-resistance, while the threshold voltage undergoes similar degradation mechanisms to those observed under forward gate bias stress. This further confirms that the gate region is the most affected under reverse conduction mode.

This comprehensive assessment of degradation and failure mechanisms offers critical insights into the limitations and reliability of SP-HEMTs when operating in reverse conduction mode. These results are particularly important for designers of power circuits, as understanding the failure modes under this operating regime can significantly improve the design and durability of power electronics that rely on these transistors. By recognizing how temperature, gate geometry, and applied voltages influence device lifetime and performance, engineers can optimize circuit designs to ensure greater reliability and efficiency in high-power applications.

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