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Modular Multilevel Converter with Interleaved Submodule based on Current-Fed Dual Active Bridge

Marzio Barresi
DEIB
Politecnico di Milano
Milano, Italy
marzio.barresi@polimi.it

Riccardo Mandrioli
Dept. of Electrical, Electronic, and Information Engineering
University of Bologna
Bologna, Italy
r.mandrioli@unibo.it

Mattia Ricco
Dept. of Electrical, Electronic, and Information Engineering
University of Bologna
Bologna, Italy
mattia.ricco@unibo.it

Samuele Grillo
DEIB
Politecnico di Milano
Milano, Italy
samuele.grillo@polimi.it

***Abstract*—This paper proposes a novel architecture for a solid-state transformer (SST)-based modular multilevel converter (MMC) incorporating a dual active bridge (DAB) stage within each submodule (SM). The proposed converter features interleaved SMs that concurrently interface with the converter AC side and serve as the input-side bridges of embedded current-fed DAB (CF-DAB) converters. By integrating the CF-DAB topology directly into the MMC SMs, the proposed design achieves higher power density, reduced component count, and improved scalability for medium- to high-voltage DC applications, while also enabling a distributed architecture. The interleaved structure among SMs facilitates ripple current minimization, extends the soft-switching operating range, and increases the number of effective voltage levels. This paper provides a comprehensive analysis of the converter operating principles, modulation strategies, and coordinated control between the MMC and CF-DAB stages. The validity and performance of the proposed concept are demonstrated through detailed simulation results.**

***Index Terms*—current-fed, dual active bridge, interleaving, modular multilevel converter, solid-state transformer**

I. Introduction

Modular multilevel converters (MMCs) have become the de facto standard for medium- and high-voltage applications due to their superior voltage scalability, modularity, and high-quality output waveforms with low harmonic distortion [1]–[3]. Originally developed for high-voltage direct current transmission and flexible AC transmission systems, MMCs are now increasingly being adopted in emerging applications based on solid-state transformer (SST) architectures. These include medium-voltage (MV) motor drives, the integration of renewable energy sources and energy storage systems into MV grids, electric vehicle fast charging stations, and MV DC distribution networks [4]–[8]. SST-based MMCs address one of the key limitations of conventional MMC topologies, namely, the absence of intrinsic galvanic isolation, which poses challenges in applications requiring safe and reliable interconnection between medium- and low-voltage domains.

In these SST-oriented configurations, isolated DC–DC converter topologies such as the dual active bridge (DAB) are commonly cascaded with MMCs to provide the required galvanic isolation and enable power flow between different voltage levels or energy domains [9]. While this multi-stage approach enables functional decoupling and voltage adaptation, it also introduces additional design complexity in terms of control, sizing, component count, and energy buffering [10].

This paper proposes a novel converter architecture that integrates current-fed DAB (CF-DAB) stages directly into the submodules of an MMC (see Fig. 1). The resulting topology forms an interleaved submodule structure that inherently provides galvanic isolation, harmonic distortion reduction, a larger soft switching region, and a shorter bill of materials [11]–[13]. In the proposed configuration, each submodule simultaneously functions as a standard MMC cell and as the primary-side bridge of a CF-DAB. The interleaved arrangement increases the effective voltage level count and enables high-frequency ripple cancellation, improving dynamic performance and reducing the need for bulky filtering components. Additionally, the interleaving inductors behave like an auxiliary inductor extending the DAB soft switching region [14]. The proposed solution requires eight switches per submodule rather than ten, reducing the bill of materials and submodule complexity.

By embedding the CF-DAB within the MMC structure, the proposed converter achieves seamless power conversion from a high-voltage DC input to a galvanically isolated low-voltage or medium-voltage DC output, all within a unified modular architecture. This integration significantly reduces the overall system footprint and complexity, while preserving the scalability of the MMC architecture with respect to power and voltage levels. Moreover, sources or energy storage systems can be appropriately allocated across the converter submodules (SMs), enabling a modular and fully distributed architecture.

The paper details the operating principles of the proposed converter, including its modulation scheme, power flow control, and dynamic behavior. Analytical modeling is complemented by comprehensive simulation results, demonstrating the effectiveness and feasibility of the proposed concept. The rest of the manuscript is organized as follows. Section II reviews the foundational topologies on which the proposed power conversion system is based, namely the interleaved MMC and the CF-DAB. Section III then introduces the proposed system architecture, outlines the control strategy, and discusses its advantages and limitations. Numerical validation of the proposed approach is presented in Section IV. Finally, conclusions are summarized in Section V.

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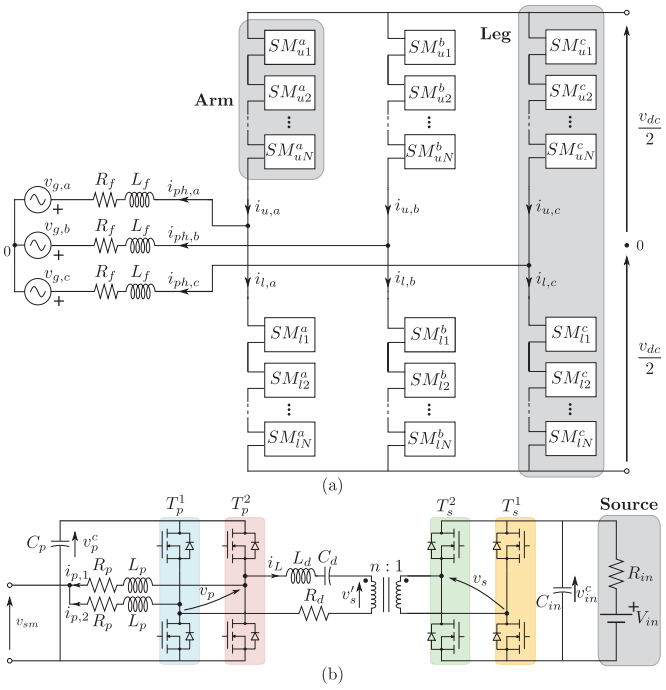

Fig. 1. Three-phase MMC with interleaved submodule based on integrated DAB. (a) Converter schematic; (b) submodule schematic.

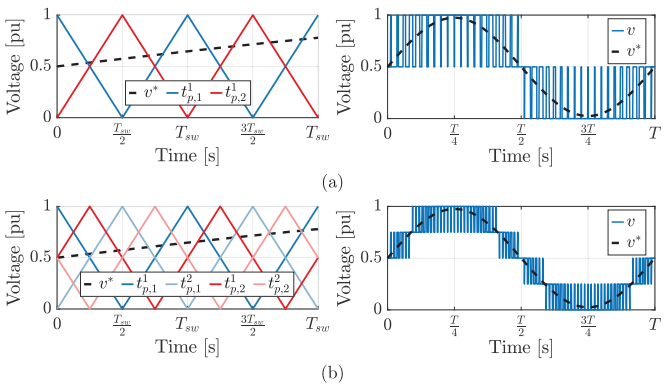

Fig. 2. Carrier signals of the submodules and corresponding output arm voltage under open-circuit conditions for $N = 2$; (a) conventional MMC; (b) MMC employing interleaved SMs.

II. Background

A. Interleaved MMC

The proposed power conversion system is shown in Fig. 1. It consists of three legs, each comprising two arms, commonly referred to as the upper and lower arms. Each arm consists of N series-connected SMs based on an interleaved topology and a current-fed DAB converter. The interleaved SMs can generically be composed of m half-bridge (HB)-legs; in this work, $m = 2$ HB-legs are considered.

Focusing on the primary side of the DAB, which interfaces with the AC grid, the interleaving concept for the MMC has been previously investigated in [11], [12], from which the following equations can be derived. Neglecting zero-sequence voltage components, the per-arm voltages for each k-phase (with $k \in a, b, c$) are given by:

$$\begin{cases} v_{u,k} = -v_{g,k} - R_f(i_{u,k} - i_{l,k}) - L_f \dfrac{d\,(i_{u,k} - i_{l,k})}{dt} + \dfrac{v_{dc}}{2} \\ v_{l,k} = v_{g,k} + R_f(i_{u,k} - i_{l,k}) + L_f \dfrac{d\,(i_{u,k} - i_{l,k})}{dt} + \dfrac{v_{dc}}{2} \end{cases} , \quad (1)$$

where $v_{u,k}$ and $v_{l,k}$ are the upper and lower arm voltages, respectively; $v_{g,k}$ is the grid voltage; v_{dc} is the DC-side voltage; $i_{u,k}$ and $i_{l,k}$ are the upper and lower arm currents, respectively; L_f is the output filter inductance; and R_f is its resistance.

The arm voltages are defined by the activation or bypass of the converter SMs, and can therefore be expressed as:

$$v_{u,k} = \sum_{i=1}^{N} v^k_{sm,u,i} \ , \qquad v_{l,k} = \sum_{i=1}^{N} v^k_{sm,l,i} \ , \qquad (2)$$

where $v^k_{sm,u,i}$ and $v^k_{sm,l,i}$ denote the output voltage of the i-th SM in the upper and lower arms of the k-th phase, respectively. For a generic SM, considering that it consists of $m = 2$ HB-legs, the output voltage (neglecting superscripts and subscripts related to arm and phase for notational simplicity) is given by:

$$v_{sm} = \frac{1}{2}\left[\sum_{m=1}^{2} g^m_p v^c_p + L_p \sum_{m=1}^{2} \frac{di_{p,m}}{dt} + R_p \sum_{m=1}^{2} i_{p,m}\right] \ , \quad (3)$$

where L_p and R_p are the primary-side inductance and resistance of the inductors integrated in the interleaved SMs; $i_{p,m}$ is the current flowing through the m-th HB-leg; and g^m_p is the gate signal of the m-th HB-leg. The sum of $i_{p,m}$ corresponds to the upper ($i_{u,k}$) or lower ($i_{l,k}$) arm current. The value of g^m_p is 1 when the upper switch of the m-th HB-leg is ON. From (3), the advantage of adopting an interleaved structure becomes evident, as it enables improvement of the converter output voltage quality. Specifically, each SM can generate $m+1$ voltage levels while each arm will present $N\,m+1$ voltage levels.

Considering $N = 2$ converter SMs, a comparison of open-circuit arm voltages with the conventional MMC can be made, as shown in Fig. 2. In a conventional MMC, each SM consists of a single HB-leg (e.g., T^1_p in Fig. 1(b)) and is controlled by a single carrier signal—for example, $t^1_{p,1}$ and $t^1_{p,2}$ for the two SMs. The resulting open-circuit output arm voltage will thus consist of $2+1$ levels, as illustrated in Fig. 2(a). Since the SMs are based on HB converters, only positive voltage levels can be generated. Conversely, in the proposed SM topology (Fig. 1(b)), each SM is controlled by two carrier signals—one per HB-leg. For the first SM, these are $t^1_{p,1}$ and $t^2_{p,1}$; for the second SM, $t^1_{p,2}$ and $t^2_{p,2}$. In this manner, each SM can produce $2+1$ levels, yielding a total of $4+1$ levels, as depicted in Fig. 2(b). Also in this case, only positive voltage levels can be generated. It is worth noting that the same output voltage levels could theoretically be achieved in a conventional MMC by incorporating an additional SM based on an HB converter and a DC capacitor. However, the proposed approach only requires the addition of one HB-leg to each conventional SM, thereby reducing overall converter volume and weight.

Finally, by substituting (3) into (2), and then into (1), the relationship between the interleaved SM inductance L_p and resistance R_p and the arm inductance L_{arm} and resistance R_{arm} in a conventional MMC is established as:

$$L_p = \frac{m}{N} L_{arm} \ , \quad R_p = \frac{m}{N} R_{arm} \ . \qquad (4)$$

This enables the same design criteria used for the conventional MMC to be applied to the interleaved configuration, ensuring equivalent average dynamic performance.

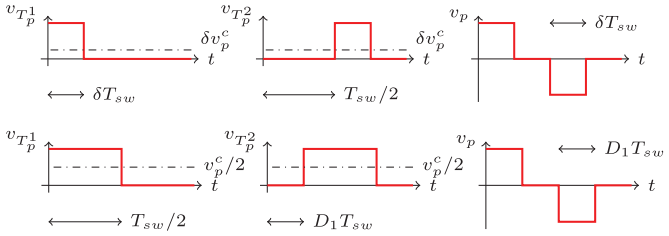

Fig. 3. H-bridge voltage v_p equivalence in case of modified SPS (top) and DPS (bottom) considering $\delta = D_1$.

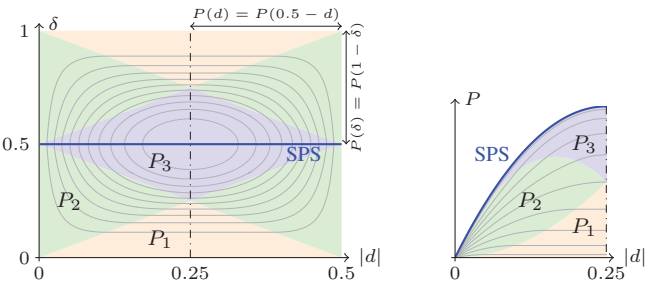

Fig. 4. Power contour plot as function of the phase shift d and duty-cycle δ (left). Normalized power as a function of the phase shift d for various values of duty-cycle δ (right). Power regions: orange P_1, green P_2, and blue P_3.

B. Current-fed DAB under modified SPS

Still with reference to Fig. 1 schematic, the interleaved submodule can be considered as a current-fed H-bridge for a DAB. Such topology is usually controlled by means of the so-called modified single-phase shift (SPS) modulation, by adjusting the leg duty cycle δ (associated with the sine wave to be modulated) and the outer phase shift d (which enables power exchange between the two sides of the converter); note that the time delay between input and output bridge is dT_{sw} where T_{sw} is the submodule switching period and $d \in [0; 0.25]$. Different from the conventional SPS whose duty cycle is fixed to 0.5 and the power is regulated solely using the outer phase shift d as per:

$$P = \frac{v_p^c v_{in}^c n}{f_{sw} L_d} d(1 - 2d) \ , \tag{5}$$

the modified SPS introduces a further degree of freedom δ modifying (5) as:

$$P = \frac{v_p^c v_{in}^c n}{f_{sw} L_d} \begin{cases} \delta^2 & \delta \leq d & P_1 \\ d(2\delta - d) & d \leq \delta \leq 0.5 - d & P_2 \\ d - 2d^2 - (0.5 - \delta)^2 & 0.5 - d \leq \delta & P_3 \end{cases} . \tag{6}$$

The symbol L_d is the DAB transfer inductance, $f_{sw} = 1/T_{sw}$ is the switching frequency, n is the transformer turn ratio, v_p^c represents the voltage across the submodule capacitor C_p, and v_{in}^c is the secondary-side voltage; parasitic resistances R_p and R_d visible in Fig. 1(b) are considered negligible. Notice that the symmetry plane $\delta = 0.5$ ensures that $P(\delta) = P(1 - \delta)$ as per [13]. Power regions in (6) are equivalent to the ones given by the popular dual-phase shift (DPS) which, likewise modified SPS, presents two degrees of freedom in the form of the outer phase shift d and the inner one D_1 [15], [16]. Such equivalence can be verified at a glance from Fig. 3 where voltage v_p is equivalent in both cases. In fact, region P_1 is the modified SPS counterpart of the so-called DPS independent surface because phase shift d invariant [15]. Power regions described in (6) are visualized in Fig. 4. For a given power level P, the outer phase shift d is selected accordingly to the duty cycle δ, allowing to control at the same time power flow and submodule voltage v_{sm}. The main drawback of the modified SPS is related to the need for DC blocking capacitors C_d to suppress transients given by the continuous variation of the duty cycle. Similar issues appear in DPS as well for control with rapid dynamics. All the other considerations related to DPS keep on holding also in the case of the proposed converter.

III. Proposed Topology

The proposed topology takes advantage of both topologies discussed in Section II to achieve an interleaved MMC whose submodules are constituted by current-fed DAB under variable duty cycle modulation. As visible from Fig. 1, the submodule input stage integrates the interleaved MMC submodule as well as the current-fed DAB primary into a unique solution without the need for a back-to-back cascaded connection as typically done in conventional MMCs. In this way, the proposed design not only simplifies the physical implementation, enabling a more compact converter layout by requiring one fewer HB leg per SM, but also doubles the number of voltage levels generated by the MMC arms for the same number of SMs.

A. Operating constraints of the proposed converter

The proposed topology inherently ensure smaller bill of material but presents some limitations due to the modified SPS introduced in Subsection II-B. Specifically, to maintain full control on the MMC arm voltage and power processed by each DAB it is paramount that the converter does not operate in the region P_1 (i.e., the independent surface). In other words, the relationship:

$$d_{\text{max}} = \delta_{\text{min}} \leq \delta \leq \delta_{\text{max}} = 1 - d_{\text{max}} \ , \tag{7}$$

must hold regardless from the processed power and the instantaneous value of the AC voltage. Symbol d_{max} is the maximum outer phase shift while δ_{min} and δ_{max} are the minimum and maximum leg duty cycle, respectively. Equation (7) poses an effective limitation in the value of each submodule amplitude modulation index m_a that must be smaller than $1 - 2d_{\text{max}}$ [13]; having $m_a \in [0; 1]$. Typical DAB designs set $d_{\text{max}} = 0.15$ as a typical maximum outer phase shift value leading to $\delta_{\text{min}} = 0.15$, $\delta_{\text{max}} = 0.85$, and $m_a = 0.7$. Duty cycle limitation lead also into the DAB maximum power threshold:

$$P_{\text{max}} = \frac{v_p^c v_{in}^c n}{f_{sw} L_d} d_{\text{max}}^2 \ , \tag{8}$$

which must be taken into account during the design of L_d.

B. Converter control strategy

The overall control strategy is depicted in Fig. 5. The converter control strategy aims to define the reference arm voltages ($v_{u,k}^*$, $v_{l,k}^*$) as well as the CF-DAB power references ($P_{d,u,k,j}^*$, $P_{d,l,k,j}^*$). The reference arm voltages regulate active and reactive power exchange with the grid, while also managing internal energy balancing within the converter [17].

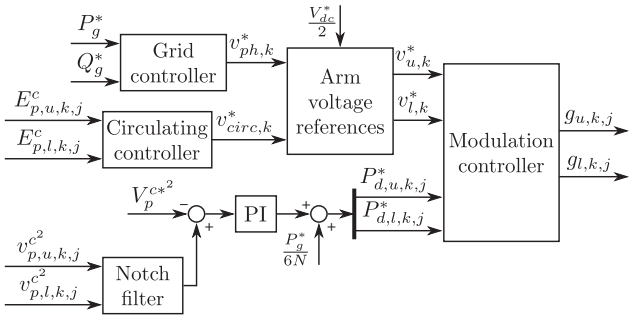

Fig. 5. Overall converter control scheme.

The reference arm voltages are given by:

$$\begin{cases} v_{u,k}^* = -v_{ph,k}^* + v_{circ,k}^* + \dfrac{V_{dc}^*}{2} \\ v_{l,k}^* = v_{ph,k}^* + v_{circ,k}^* + \dfrac{V_{dc}^*}{2}. \end{cases} \tag{9}$$

Here, $v_{ph,k}^*$ is the reference phase voltage component used to manage power flow with the AC grid by regulating the output converter currents $i_{ph,k}$, and $v_{circ,k}^*$ is the reference circulating voltage component used to handle internal converter energy imbalances through the control of circulating currents $i_{circ,k}$. The zero-sequence component V_{dc}^* is included to ensure that each converter arm synthesizes only positive voltages, as required by the HB-based submodules. The output converter currents $i_{ph,k}$ and the circulating currents $i_{circ,k}$ are defined as:

$$i_{ph,k} = i_{u,k} - i_{l,k}\ , \qquad i_{circ,k} = \frac{i_{u,k} + i_{l,k}}{2}\ . \tag{10}$$

The reference phase voltage component $v_{ph,k}^*$ is defined by employing a well-known control strategy in the dq reference frame, which is synchronized with the grid voltage. Given the active (P_g^*) and reactive (Q_g^*) power references, the corresponding dq components of $i_{ph,k}$ are generated and regulated via proportional-integral (PI) controllers. The reference circulating voltage component $v_{circ,k}^*$ is generated by the circulating current controller, which is designed to prevent energy imbalances among the DAB primary-side capacitors ($E_{p,u,k,j}^c$, $E_{p,l,k,j}^c$). The AC component of the circulating current $i_{circ,k}$ regulates the energy of the capacitors within the same converter leg, while its DC component balances the energy across different converter legs. The zero-sequence voltage V_{dc}^* is defined as NV_p^c, where V_p^c is the rated voltage of the CF-DAB primary-side DC link.

The power managed by each CF-DAB integrated into an SM is regulated by controlling the square of the primary-side voltage to its rated value via a PI controller [17]. To mitigate the influence of voltage ripple caused by single-phase power oscillations, the primary-side capacitor voltages ($v_{p,u,k,j}^c$, $v_{p,l,k,j}^c$) are filtered using a notch filter. To enhance dynamic response, a feedforward term is included, as illustrated in Fig. 5. Then, the reference signals ($v_{u,k}^*$, $v_{l,k}^*$, $P_{d,u,k,j}^*$, $P_{d,l,k,j}^*$) are fed to a modulation controller implemented for each SM. This controller regulates the CF-DAB to manage the active power exchanged with the source connected to the corresponding SM by adjusting the phase shift between the primary- and secondary-side bridges of each DAB, according to (6). The leg duty cycle δ is calculated by dividing the reference voltage $v_{u,k}^*$ or $v_{l,k}^*$ by the nominal DC bus voltage V_{dc}^*. Once the modulating signals and phase shifts are determined, the gate signals ($g_{u,k,j}$, $g_{l,k,j}$) for the converter submodules are generated.

IV. Case Study

This section presents the converter operation in the case of connection to an AC grid. Specifically, a 100 kW MMC connected to a 400 V grid is considered. The system parameters are reported in Table I and Table II. The MMC comprises $N = 2$ interleaved SMs based on CF-DABs. In each CF-DAB, a source is integrated and modeled as a constant voltage in series with a resistance.

The rated voltage of the primary side of the CF-DAB, V_p^c, is selected considering the constraints imposed by the adopted SPS modulation. Taking into account the maximum allowable duty cycle, $\delta_{\max}$, the reference arm voltages derived from (9) must satisfy the following condition:

$$m_a + \frac{1}{2} < \frac{\gamma \hat{V}_g}{NV_p^c} + \frac{1}{2} < \delta_{\max} = 0.85 \tag{11}$$

where $\hat{V}_g$ denotes the peak value of the grid phase voltage, and γ is a design margin factor accounting for active/reactive power control, internal energy balancing through circulating voltage injection, and capacitor voltage oscillations. Therefore, $\gamma \hat{V}_g$ represents the maximum amplitude of the combined reference voltages $v_{ph,k}^*$ and $v_{circ,k}^*$. By rearranging (11), the required minimum value for V_p^c is:

$$V_p^c > \frac{2\gamma \hat{V}_g}{N\,(2\delta_{\max} - 1)}. \tag{12}$$

A unitary transformer turns ratio is adopted between the primary and secondary sides of the DAB. The transformer inductance is sized according to (8), assuming a switching frequency of $f_{sw} = 10$ kHz. To prevent the rise of a DC component in the DAB inductor current, a DC blocking capacitor C_d is included. Its value is determined so that $Z_c = Z_L/100$, where $Z_c = 1/(2\pi f_{sw} C_d)$ is the capacitor impedance and $Z_L = 2\pi f_{sw} L_d$ is the inductor impedance, thereby ensuring negligible interference with power transfer at the switching frequency.

TABLE I
MMC SYSTEM PARAMETERS

Description	Symbol	Value	Unit
Rated plant power	S_n	100	kW
Rated grid phase voltage (rms)	v_g	230.9	V
Rated grid frequency	f_g	50	Hz
Filter resistance	R_f	5	mΩ
Filter inductance	L_f	250	μH
Number of SM per arm	N	2	–
Margin coefficient	γ	1.2	–

TABLE II
CF-DAB PARAMETERS

Description	Symbol	Value	Unit
Rated CF-DAB power	P_d	8.3	kW
Equivalent resistance (switch + transformer)	R_d	35	mΩ
Transformer inductance	L_d	97.2	μH
Transformer turns ratio	n	1	-
Primary-side rated voltage	V_p^c	600	V
Primary-side inductance	R_p	50	mΩ
Primary-side resistance	L_p	500	μH
Primary-side capacitance	C_p	5	mF
Source rated voltage	V_{in}	600	V
Source resistance	R_{in}	100	mΩ
Source capacitance	C_{in}	200	μF
DC-blocking capacitance	C_d	260	μF
Maximum duty cycle	$\delta_{\max}$	0.85	-
Minimum duty cycle	$\delta_{\min}$	0.15	-
Switching frequency	f_{sw}	10	kHz

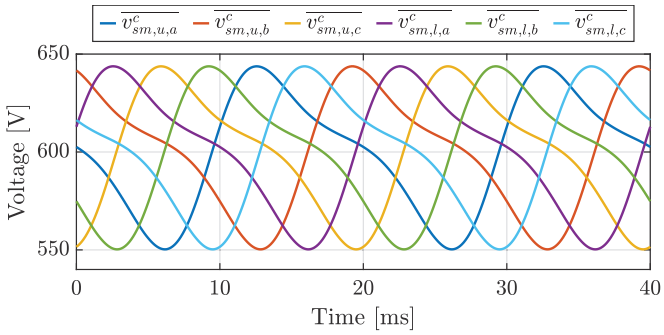

Fig. 6. Average primary-side SM voltages.

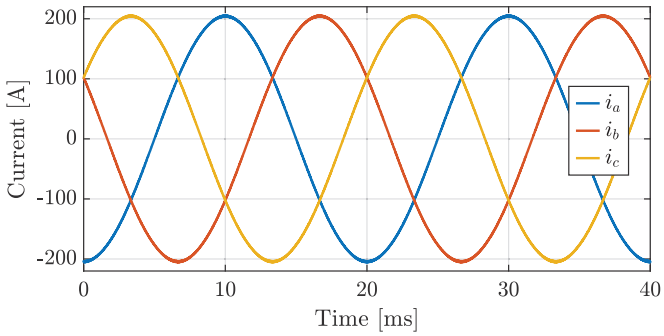

Fig. 7. Converter three-phase output currents.

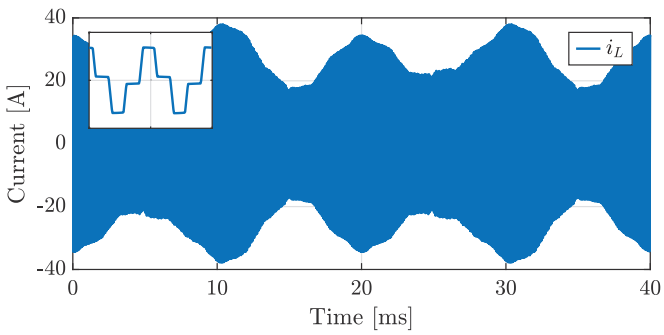

Fig. 8. CF-DAB inductor current.

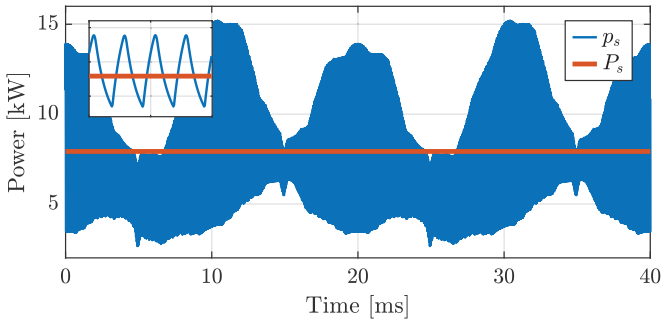

Fig. 9. CF-DAB source instantaneous and active power.

A. Simulation results

To demonstrate the validity of the proposed power conversion system, numerical simulations were performed at the rated power of 100 kW. Waveforms of the main variables are shown in Figs. 6-9.

As illustrated in Fig. 6, the voltages of the primary-side CF-DAB capacitors are all regulated at their rated value, $V_p^c = 600$ V. The converter successfully exchanges the rated power while maintaining low harmonic distortion, as evident from Fig. 7. Although based on only two SMs, the interleaved operation enables the converter to achieve an effective $4 + 1$ voltage level output, thereby improving output current quality. Specifically, the total harmonic distortion of the three-phase output current is as low as 0.31%.

Fig. 8 displays the DAB inductor current i_L over two fundamental periods. As is visible in the zoomed frame, the current assumes the DAB typical piecewise waveform. The additional zero-level with respect to conventional SPS is due to the DPS-like behavior. Moreover, the modified SPS modulation introduces a 100 Hz periodicity visible in the current envelope due to the continuous variation of the duty cycle δ. Similar considerations can be drawn in the power plot visible in Fig. 9, where the 100 Hz oscillation is visible as well. Such considerations are consistent with what is anticipated in [13]. The overall active power is consistent with the reference value P_d of about 8.3 kW.

V. Conclusion

This paper proposes a novel power conversion system based on a MMC with integrated CF-DAB stages embedded within each SM, featuring interleaved operation. The proposed topology inherently provides galvanic isolation and enables direct interfacing with sources or energy storage systems at the SM level, thereby achieving a distributed architecture. Additionally, the interleaved operation facilitates high-frequency ripple cancellation and increases the effective number of voltage levels, which reduces filtering requirements.

Compared to a conventional MMC employing back-to-back SMs with separate DAB stages, the proposed design doubles the number of voltage levels generated by the MMC arms for the same number of SMs, as demonstrated in the case studied here with interleaved submodules composed of two legs. Furthermore, the architecture requires one fewer HB leg per SM, resulting in a more compact converter without compromising the inherent scalability of the MMC.

Future work will focus on experimental validation and expanding the operating range of the CF-DAB to achieve a higher modulation index, thereby enhancing system flexibility and utilization.

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