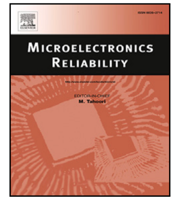
Microelectronics Reliability 168 (2025) 115664

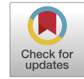
Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Research Paper



Optimization of the drain-side configuration in ESD-protection SCR-LDMOS for high holding-voltage applications

L. Zunarelli [a], S. Rotorato [a], E. Gnani [a], S. Reggiani [a],*, R. Sankaralingam [b], M. Dissegna [b], G. Boselli [b]

[a] ARCES and DEI, University of Bologna, Bologna, Italy
[b] Texas Instruments Inc., Dallas, TX, USA

ARTICLE INFO

Keywords:
Electrostatic discharge
Thermal failure
Holding voltage
TLP I-V
TCAD simulations
SCR-LDMOS

ABSTRACT

A conventional silicon-controlled rectifier integrated into a laterally diffused MOSFET (SCR-LDMOS) is studied through 2D TCAD simulations in order to obtain the maximum holding voltage without increasing the area consumption or degrading the power-to-failure robustness. A reference device with 150V trigger voltage, 3V holding voltage and an approximate thermal breakdown at 30 mA/μm is adopted. Different configurations of the drain-side region are compared, with the best solution showing a 5x improvement on the holding condition without a significant variation on the other figures of merit.

1. Introduction

Emerging applications, such as automotive electronics, power management, analog multiplexers, driver integrated circuits, are playing an increasingly important role. In the development of the correlated smart power integrated circuits, the electrostatic discharge (ESD) protection is a major concern. ESD robustness should concern the most likely events, i.e., Human Body Model (HBM) and Charged Device Model (CDM), with stresses in the 1–100 ns duration range [1]. A few examples of relevant applications are the Local Interconnect Network (LIN) bus or the Controller Area Network (CAN) communication protocol, both designed for providing reliable highspeed data transmission in harsh environments [2]. They all require ESD protection cells with relatively high trigger voltages (V_t), as they should not activate at voltages below 100–150 V. On the other hand, the ESD cell should be characterized by a holding voltage (V_h) higher than the supply voltage of the protected circuit in order to guarantee latch-up immunity and reliability [3,4]. Actually, such buses show a wide range of operating voltages (4–40 V), giving rise to the need of a family of ESD cells providing adjustable V_h, which is shown to be difficult [5–7]. To this purpose, BCD technology with high power capabilities and integration feasibility between analog and digital devices is considered the prominent solution.

The key element to withstand V_t as large as 150 V with ideal area efficiency is the LDMOS device. Considering robustness requirements of maximum second-breakdown failure current (I_{T2}) as large as 25–50 mA/μm, the integration of the silicon-controlled rectifier (SCR) in the LDMOS device is the key choice for on-chip ESD protection [8,9]. The self-protection capability of SCR-LDMOS devices is still considered very attractive, with layout-adjustable triggering voltages and the highest failure current levels per area. There is still an open issue regarding their low V_h, as a number of interesting approaches have been shown to increase it, but most of them require additional area or eventually decrease the power-to-failure robustness. Among them, 2D stacked structures have been proposed in [10], leading to unavoidable proportional increase of the chip area with the stacking number. An SCR-LDMOS device implementing an additional surface gated PIN diode has been proposed in [6], with a significant modification of the reference structure, giving rise to complex trade-offs between V_h, I_{T2} and area. Segmented 3D emitter layouts were studied in [11,12], yielding significant undesired reductions of I_{T2}. Finally, the electron or ion irradiation was proposed as a key tool for off-line optimization of the device parameters without any further area consumption in [13].

In [14], a novel SCR-LDMOS with a buried-oxide isolation was proposed providing large V_h with the adoption of a p-implant layer (PIL) in the LDMOS pbody and an n-implant layer (NIL) under the drain-side region. In [15], a lateral super-junction LDMOS was proposed with both p-n-p and n-p-n arranged drain-side configurations. In both cases, the n/p area ratio of the SCR structure showed to be relevant in improving both I_{T2} and V_h.

In this paper, the previously proposed drain-side configurations are applied to a conventional SCR-LDMOS with 150 V off-state breakdown, featuring a p-epi/n-buried bulk isolation and an STI oxide along the drift region. 2D TCAD results and physical interpretations show how

* Corresponding author.
E-mail address: susanna.reggiani@unibo.it (S. Reggiani).

https://doi.org/10.1016/j.microrel.2025.115664
Received 21 November 2024; Received in revised form 9 February 2025; Accepted 26 February 2025
Available online 13 March 2025
0026-2714/© 2025 The Authors. Published by Elsevier Ltd. This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/).

it is possible to exploit and optimize the drain-side configuration to profitably improve the contribution of the vertical current flow through the n-buried layer at very large current levels, leading to a significant improvement of V_h without influencing area and I_{T2}.

2. Reference device and TCAD simulation set-up

The schematic representation of the reference SCR-LDMOS is shown in Fig. 1 along with the equivalent circuit. The simulated structure is a modification of the power LDMOS device with the additional p+ diffusion into the drift region as in [8]. 2D simulations have been carried out using the commercial TCAD tool SDevice by Synopsys [16]. All simulations have been conducted using the drift–diffusion transport model coupled with the heat-transfer equation. Among the physical models, UniBo bulk mobility, Shockley–Read–Hall and Auger thermal generation–recombination and UniBo impact-ionization generation–recombination models have been selected with default parameters. Specifically, the UniBo models were adopted due to their validation over extended temperature ranges, the overall methodology was demonstrated to nicley describe the high-injection regimes during ESD [17,18]. The TCAD setup of an LDMOS device used in previous works was adopted as a starting point, featuring an extended calibration against experiments both in pulsed TLP and DC configurations [19]. The device geometry was directly derived from its layout; the description of the doping profiles was obtained from spreading resistance profiling data, secondary ion mass spectrometry measurements, and process simulation results. The 2D domain was extended under the n-buried bulk isolation ("NBL" in Fig. 1) of about 25 μm in the p-type semiconductor substrate in order to correctly solve the thermoelectrical problem at high current levels. A few investigations have been carried out on test devices with separated source and body contacts to further check the simulation deck, and a calibration of the thermal resistances at the contacts has been performed to correctly account for the self-heating effects [20]. The same 2D domain and thermal boundary conditions have been assumed in the SCR-LDMOS structures analyzed in this work. The drift length is directly related to the breakdown condition, thus to the onset of avalanche leading to the snapback. The snapback condition by itself is given by the triggering on of the NPN BJT, which is associated to the collector-emitter resistance, i.e., with the value of R_{NPN} (Fig. 1): the SCR-LDMOS structure features the same PIL layer as in [20], the p-substrate is connected to the cathode through the PIL region; no modifications of the cathode structure are addressed in this work. The SCR integrated in the anode region features an STI interposed between the n+ and p+ wells at the surface, an additional NIL layer and a deep n-well isolation ("NIL" and "DeepN" regions in Fig. 1, respectively) realized by using doping profiles provided in the same 0.15 μm BCD technology. The NBL results connected to the anode through the DeepN region. The transmission-line pulse (TLP) is known as the testing technique assisting in the designing and qualification of the integrated ESD solutions [21]. It has been simulated here by applying current pulses to the anode contact with 100ps rise time and 100ns pulse length, emulating the standard TLP characterization with grounded cathode and substrate. Increasing current pulses are applied to the structure and the voltage at the end of the pulse is extracted to create the TLP I-V curve: a careful choice of the current levels was adopted in order to obtain a nice description of the triggering, snapback, holding and failure regimes. The TCAD transient simulations can be helpful to understand both standard TLP and very-fast TLP (VF-TLP) I-V curves by simply extracting the voltage at 100 ns and 1 ns, respectively. The accurate description of the thermoelectrical dynamics allows to monitor the maximum temperature during the current pulses and use it to define a failure criterium when the internal temperature is larger than 1200 K [22]. The reference SCR-LDMOS structure shows an ESD window with V_t of 153 V, V_h of 3 V and I_{T2} close to 30 mA/μm. In Fig. 2, the simulated TLP I-V curve of the reference device is shown, compared with experiments on a conventional SCR-LDMOS realized in the 0.15 μm BCD technology. A qualitative good agreement is shown; discrepancies can be ascribed mostly to the limited TCAD doping calibration of the SCR structure and to 3D effects.

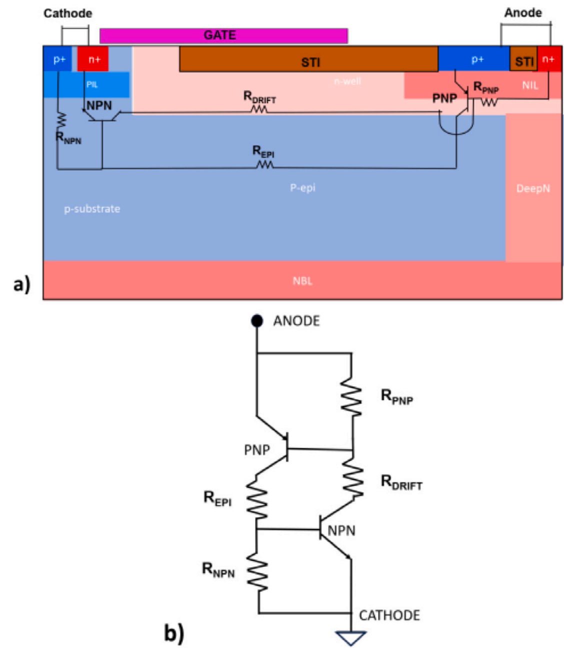


Fig. 1. (a) Schematic 2D cross-section and b) equivalent circuit of the reference SCR-LDMOS under investigation. The PIL and NIL regions are adopted to properly control the snapback onset and the consequent V_h. In the anode region, the STI is interposed between the n+ and p+ wells.

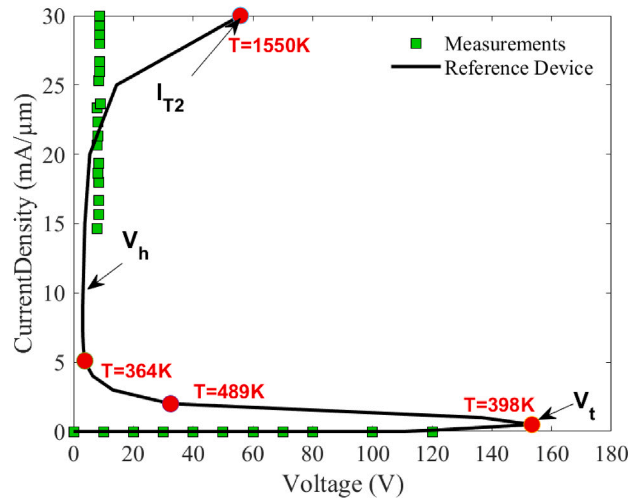


Fig. 2. TLP I-V characteristics: measurements on a conventional SCR-LDMOS (dots) are compared with TCAD simulations carried out on the reference structure. Labels indicate the maximum temperature (T_{max}) reached in the TCAD simulations. T_{max} > 1200K is adopted as the thermal-failure criterion following [22].

It is worth pointing out that 2D simulations are expected to give reliable estimations of the intrinsic holding voltage and failure current concerning with the specific inner cross-section geometry and structure, assuming a homogeneous current density in the device. 3D approaches are usually required at a further step of design. The presence of the SCR at the drain side prevents the LDMOS from premature power-to-failure, forming the parasitic PNP BJT that turns on in the holding regime. The 2D plots of the current density and lattice temperature at the failure condition are reported in Fig. 3. The current density is

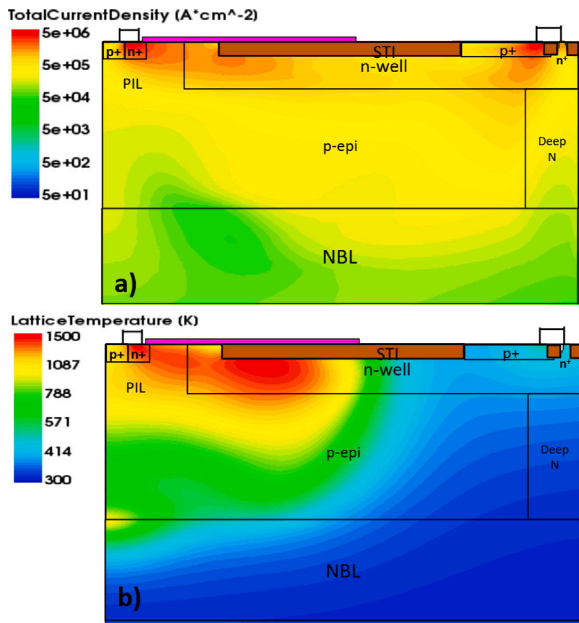


Fig. 3. 2D plot of the current density (a) and lattice temperature (b) at the onset of thermal runaway (I = 30 mA/µm).

well spread, giving rise to two main hot spots along the current path in the drift region under the STI and at the cathode region, causing the significant voltage increase up to about 50 V (Fig. 2). The current crowding experienced at the cathode contact gives rise to failure.

As far as the low V_h is concerned, it is known that the value is fixed by the contribution of the integrated resistive paths, namely, the drift region (R_{Drift}), the p-type epitaxial layer (R_{EPI}) and the respective collector regions [8]. Their contribution to V_h is correlated to the current density flowing at the surface of the device. At large injection currents, an important role is thus played by the lateral n-well isolation ("DeepN" in Fig. 1), leading to an additional vertical NPN BJT with the n-buried layer as emitter, which can be switched on in parallel to the lateral one. This contribution could be essential to guarantee high I_{T2} with high V_h. Thus, layout modifications of the anode region are proposed here to optimize the lateral/vertical contributions. Current density, electric field, impact-ionization generation and self-heating are determined along with the TLP I-V characteristics through TCAD simulations, allowing for a preliminary optimization and a deep understanding of the proposed structures.

3. Proposed test structures

Four layout modifications of the drain-side SCR configuration are presented in the following. Several simulation runs have been carried out for each proposed set-up with the aim of gaining a deep understanding of the physical behavior and spanning the full range of gain in terms of SOA with main attention to V_h and I_{T2}. The first layout change deals with the removal of the STI between the n+ and p+ well, leading to a larger pn junction area in the anode (PN-A). As a consequence of the lateral junction extension, the emitter-base R_{PNP} needs to be increased by suppressing the NIL region (Fig. 4). The second and third configurations follow the analysis proposed in [15] by implementing an additional p+ well at the right (PNP-A) or an n-p-n arrangement (NPN-A) in the drain-side region. The two different configurations, along with the corresponding equivalent circuits, are shown in Figs. 5 and 6. A further approach is finally proposed addressing mainly the vertical contribution given by the p-epi/n-isolation junction when aligned to the anode p-n-p configuration (VAPNP-A) as explained by

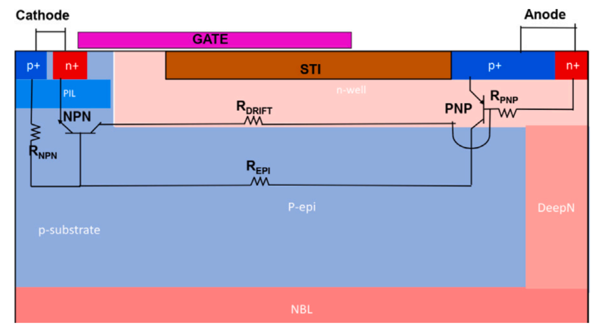


Fig. 4. Schematic 2D cross-section of the proposed PN-A SCR-LDMOS. The STI and NIL in the anode region are removed to enlarge the PNP active region (increasing the BJT gain, β_{PNP}) and increase the base-emitter resistance, R_{PNP}, leading to the proper control of the SCR onset.

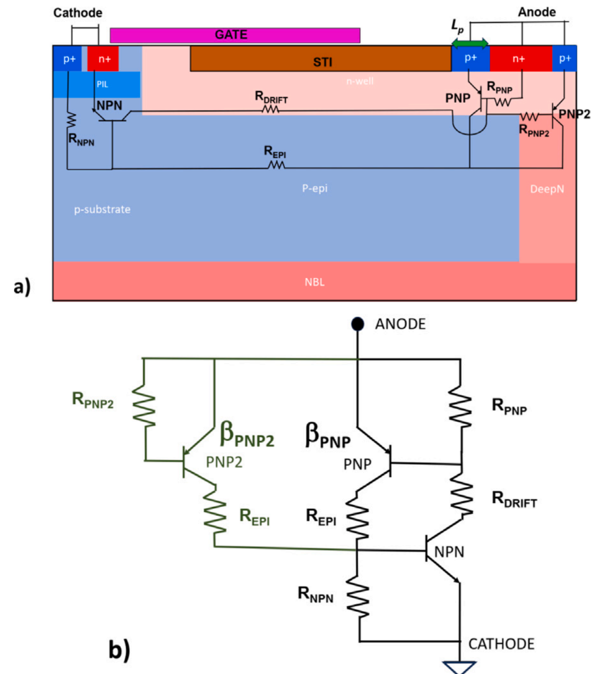


Fig. 5. (a) Schematic 2D cross-section and b) equivalent circuit of the proposed PNP-A SCR-LDMOS. The overall length of the anode region is kept constant, but the length of the left p+ well, L_p, is modified to maximize V_h. The second PNP BJT is characterized by a different active area and base region giving rise to a lower gain, β_{PNP2}) and smaller base-emitter resistance, R_{PNP2}.

the schematic view in Fig. 7. In Fig. 8, the simulated TLP I-V curves of the four different structures are reported along with the reference one. The reported cases correspond to the best results, as far as V_h and I_{T2}, obtained by changing the p+/n+ area ratio at the surface without changing the device pitch. Very similar failure conditions are obtained, as illustrated also in Fig. 9, where the maximum internal temperature is reported as a function of the TLP current pulse up to 1300 K. The latter comparison points out that all structures nicely compare as far as the largest currents are concerned, while showing relevant differences in the self heating experienced in the snapback and holding regimes.

3.1. Analysis of the role of the PN junction

By removing the STI, a larger active area of the PNP BJT is obtained, with a consequent increase of the bipolar gain β_{PNP} (Fig. 4): the larger current density at the anode side in the snapback regime gives rise to a

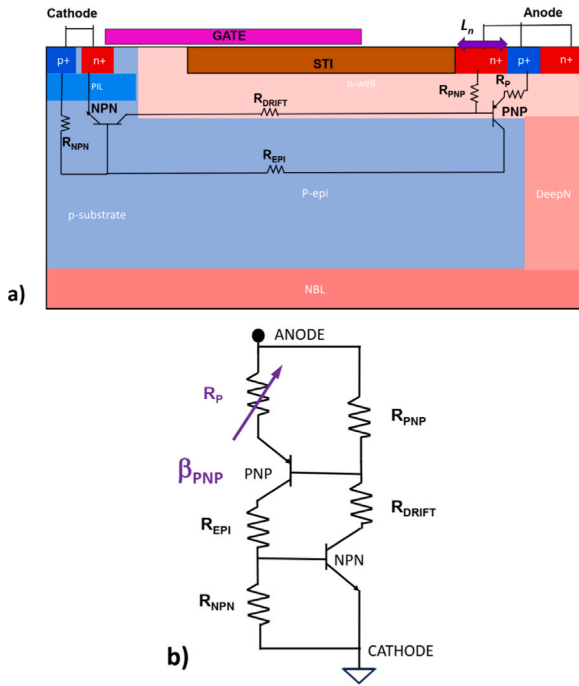


Fig. 6. (a) Schematic 2D cross-section and b) equivalent circuit of the proposed NPN-A SCR-LDMOS. The overall length of the anode region is kept constant, but the length of the left n+ well, L_n, is modified to maximize V_h through the voltage drop across R_p.

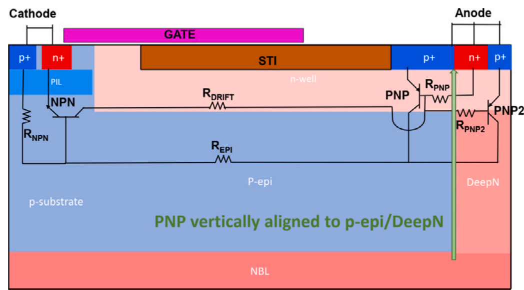


Fig. 7. Schematic 2D cross-section of the proposed VAPNP-A SCR-LDMOS. The overall length of the anode region is kept constant and the surface PNP structure is realized aligned to the p-epi/n-isolation (DeepN) junction below. The same equivalent circuit as in Fig. 5 is assumed.

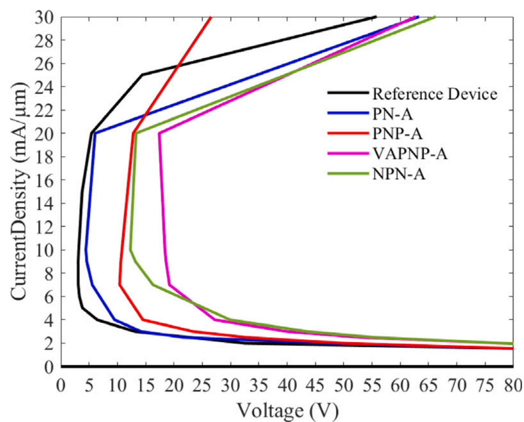


Fig. 8. TLP I-V characteristics of the different proposed devices, corresponding to the different configurations, compared with the reference one up to thermal failure.

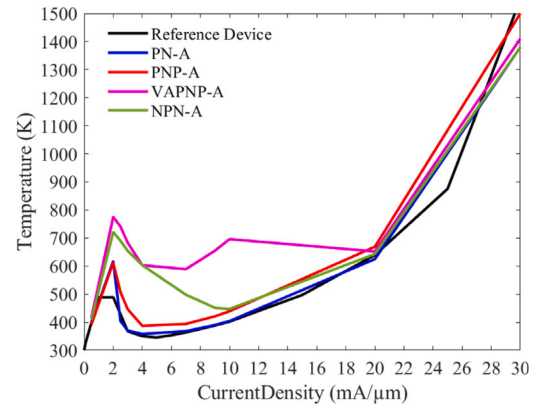


Fig. 9. Maximum internal temperature as a function of the TLP current pulses. A first peak at low current is experienced in the snapback condition. The significant increase at large currents indicates the onset of the thermal runaway.

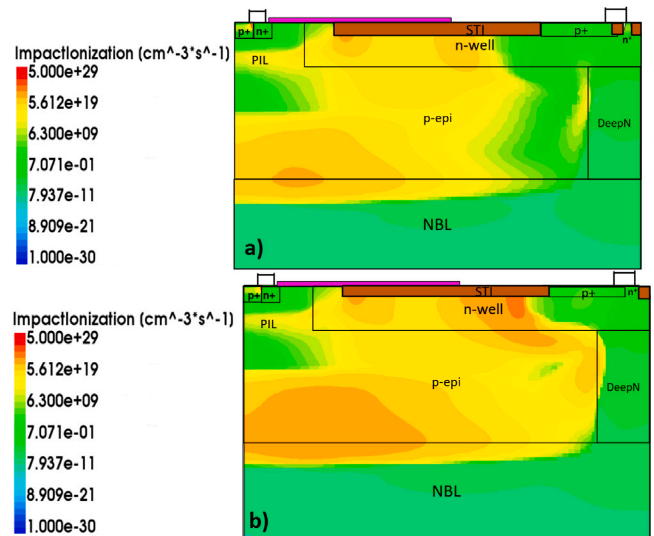


Fig. 10. 2D plots of impact ionization generation at the TLP pulse of 2 mA/μm (corresponding to the snapback regime) in (a) reference device and (b) PN-A structure, where the STI and NIL are replaces by a larger PN junction.

larger impact-ionization generation at the surface. This would lead to a strong snapback and a low V_h, which can be avoided by increasing R_{PNP}. The larger active area induces also a partial injection of current in the vertical path of the device and a beneficial impact-ionization generation in the buried layer, as shown in Fig. 10, leading to a slight increase in V_h. While V_h shows an increase, the I_{T2} value was not found to have any dependency on the proposed change, as the maximum temperatures reached in the PN-A device are similar to those in the reference one (Fig. 9).

3.2. Comparison between the PNP-A and NPN-A schemes

In line with the PN-A configuration, the role of the SCR is further addressed in the PNP-A scheme. In addition to the SCR BJT turning on at V_h, a second parallel PNP BJT is integrated, with the area of the n+ drain larger than the p+ wells, illustrated by the equivalent circuit in Fig. 5. The additional p+ well is included on the right by reducing the length of the left-side p+ well (L_p) with respect to the reference device. TCAD simulations have been carried out to determine the role played by the additional bipolar transistor, the p+ and n+ areas and the differently distributed impact-ionization generation in the key TLP

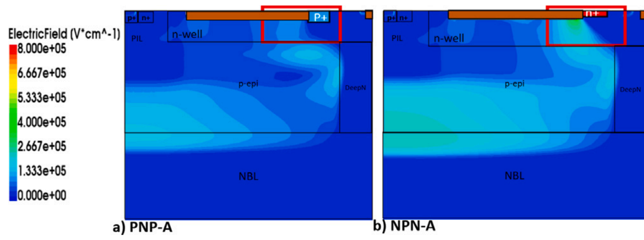


Fig. 11. Electric field distribution at 2 mA/μm for the (a) PNP-A and (b) NPN-A configurations. A critical electric field peak at the silicon surface in the n-well is visible in case (b).

Table 1
Different PNP and NPN drain-side geometries, with L_p and L_n the length of the left-side p+ and n+ well, respectively. The drain-side area and whole device pitch are kept fixed.

Device topology	V_t (V)	V_h (V)	I_{T2} (mA/μm)
Reference device	153	3	30
PNP-A (L_p = 1.5 μm)	140	7	30
PNP-A (L_p = 0.5 μm)	150	10	30
NPN-A (L_n = 1.3 μm)	157	/	2
NPN-A (L_n = 0.5 μm)	153	12	30

regimes. The study clearly shows that there is an increasing trend of V_h with decreasing left-side p+ well area (Table 1), confirming that the role played by the left-side BJT is that of feeding back the lateral NPN BJT activating the SCR, while the triggering of the second BJT ("PNP2" in Fig. 5) takes place at larger current pulses and feeds mostly the vertical path leading to better robustness. In the NPN-A drain-side arrangement, a different mechanism is expected to improve V_h, i.e., the increase of the resistance in series to the emitter of the PNP BJT, R_P, leading to an additional voltage drop as shown in Fig. 6. However, when implementing the n+ well close to the STI, a relevant self heating might be experienced in the snapback regime due to the Kirk effect at the end of the drift region. Thus, the temperature peak at small TLP current easily exceeds the failure criterion, as reported in Table 1. The comparison of the electric field distribution at a TLP current of 2 mA/μm for the PNP-A and NPN-A devices is shown in Fig. 11, proving that in the NPN-A case a critical surface electric field is experience at the left-side n-well which is significantly reduced in the PNP-A configuration.

3.3. The role of the vertical alignment in the VAPNP-A case

The improvement of the PNP-A case is further enhanced by inducing impact-ionization generation along the vertical junction between p-epi and lateral n-well isolation ("DeepN") at large current levels: in this way the role played by the vertical feedback increases and triggers the SCR at a larger V_h but also modulates the device conductivity at larger current. In order to obtain such a gain, the vertical paths of the two PNP BJTs are aligned as shown in Fig. 7. The latter situation is clearly visible in Fig. 12: the impact-ionization generation at 2 mA/μm (snapback condition) and 10 mA/μm (holding regime) are compared, showing the relevant contribution added by the vertical junction. Thus, by controlling the turn on of the vertical paths, several advantages are obtained. The improvement of the holding voltage and the stability of the failure current obtained in the VAPNP-A configuration are compared with the other proposed devices in Fig. 13. As a final outcome, V_h is improved from 3 V (reference device) to 15 V of the VAPNP-A configuration. Moreover, the proposed optimizations show us that the PNP arrangement is compatible with the adoption of further improvements as it provides a reduction of the surface field in snapback conditions. The increase of vertical contributions to the impact-ionization generation in the holding regime is a key contribution to the overall SOA robustness.

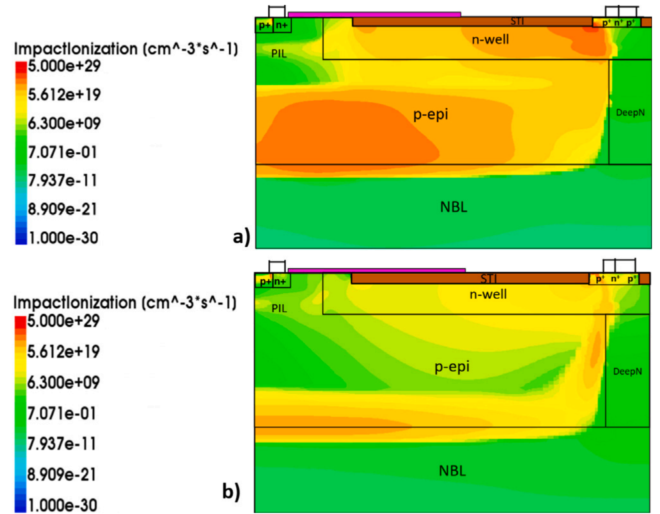


Fig. 12. 2D plots of the impact-ionization generation for the VAPNP-A at (a) 2 mA/μm (snapback regime) and (b) 10 mA/μm (holding regime).

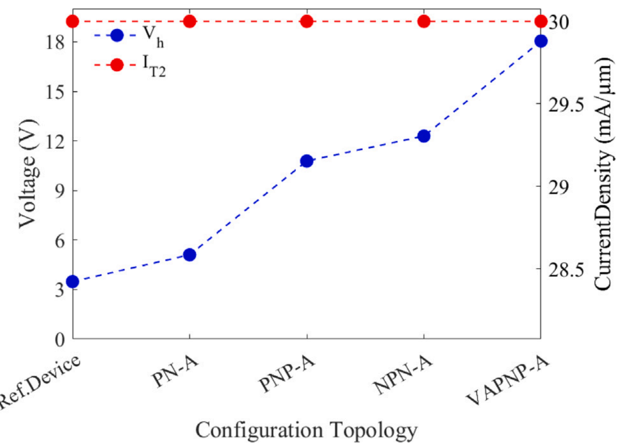


Fig. 13. Simulated holding voltage (left scale) and failure current (right scale) vs. different proposed configurations.

4. VF-TLP and SCR turn-on dynamics

As a further analysis, some elements concerning with the VF-TLP I-V curves are discussed here. The same transient simulations analyzed for the standard TLP study in the above Section can be used to extract the VF-TLP characteristics by monitoring the voltage at 1 ns after the rising time for each current pulse. In Fig. 14, the simulated VF-TLP I-V curves of the four different structures are reported along with the reference one. The reported data are extended to the maximum pulse current of 30 mA/μm, allowing to extract V_h at 1 ns and compare it to the corresponding 100-ns value over an extended range of stresses. A significant shift of about 30–40 V is observed for V_h in very fast conditions for all structures, which might be ascribed to the lower temperature ($T_{\max}$ never exceeds 400 K for all structures) and, eventually, to a slow triggering of the SCR action under fast conditions. Defining the turn-on time of the SCR-LDMOS device as the time needed for the voltage to drop to 150% of V_h at I = 10 mA/μm, the PN-A and PNP-A structures show turn-on times of about 1.5 ns, while for the NPN-A and VAPNP-A cases it is of about 3 ns. As V_h at 1 ns are significantly lower than V_t, the VF-TLP results show that the proposed ESD devices should be able to protect from CDM events.

It is worth pointing out that the wide ESD window of the SCR-LDMOS solution for HV applications has an expected drawback in

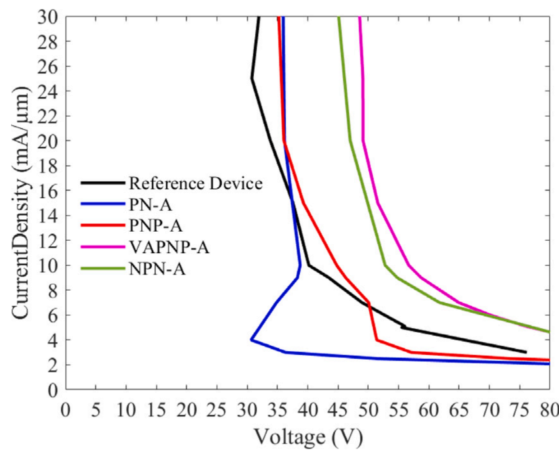


Fig. 14. VF-TLP I-V characteristics of the different proposed devices, corresponding to the different configurations, compared with the reference one up to thermal failure.

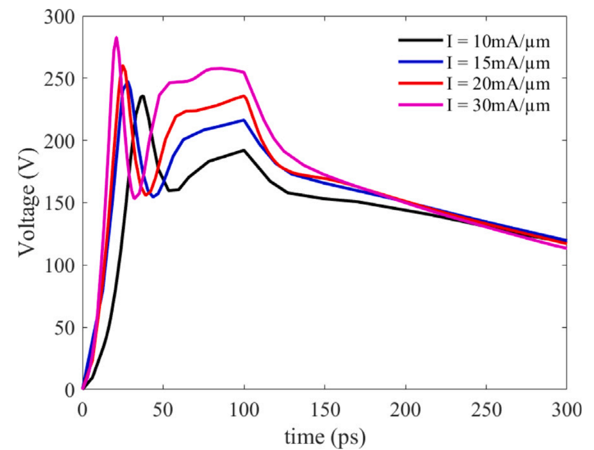


Fig. 15. Transient voltage curves for different TLP current pulses applied to the VAPNP-A SCR-LDMOS. The applied ideal current pulses are all characterized by a rise time of 100 ns.

the high voltage overshoot associated with the turn-on time of the SCR structure. The simulated voltage waveforms, corresponding to the chosen rise time of 100 ps, allow us to monitor the peak voltage reached during the rising of the signal, which can be the cause of anticipated gate oxide failure. It is clear that before the device switches on, the voltage increases well above V_t for fast rise times, due to delayed conductivity modulation. In Fig. 15, the voltage time response of the VAPNP-A structure is reported for several current pulses. The curves show two distinct overshoots during the 100ps rise time, and an overall duration of overvoltage regime ($V > V_t$, with $V_t = 160$ V for the VAPNP-A case) lower than 200 ps for the reported stress cases. Similar results are observed for the other structures, even if the maximum extension of the two overshoot peaks is experienced by the VAPNP-A case. The first peak giving rise to the large voltage overshoot, which causes the SCR triggering through impact-ionization generation in the n-well/p-epi junction, provides the base currents for the lateral npn and pnp transistors. In devices where part of the current is driven vertically towards the bottom, the experienced overshoot tends to be larger (VAPNP-A shows a max voltage at 30 mA/μm that is about 20 V larger that the reference case). The curves show a slight increase of the first voltage peak with the increase of the current pulse: the SCR triggering is delayed until a minimum charge has been injected in the device. The second voltage increase is mostly related to the inductive contribution (roughly, a plateau proportional to dI/dt) and linearly increases with the current pulse [23].

5. Conclusions

In this paper, a conventional SCR-LDMOS device in BCD technology is adopted as a reference ESD protection device with high robustness but low holding voltage. A number of layout modifications are proposed to improve the holding voltage without reducing the robustness of the device. Starting from the contribution given by the SCR PN junction, the lateral and vertical impact-ionization generations are improved with PNP and NPN arrangements. The configurations are tested through 2D TCAD simulations providing the relevant physical understanding. An optimal PNP drain-side configuration with a vertical alignment to the p-epi/nwell isolation has been identified as the best choice for improving the holding voltage with respect to the reference device, reaching 18 V. A preliminary analysis of the very-fast TLP characteristics and of the dynamic voltage overshoot during the triggering of the SCR-LDMOS under a very fast rising time are presented, showing critical voltage peaks exceeding the triggering voltage. Additional investigations on the device structure might further improve the performance starting from this result.

CRediT authorship contribution statement

L. Zunarelli: Conceptualization, Methodology, software, investigation, Writing-review. **S. Rotorato:** Conceptualization, Software, investigation, Writing-review. **E. Gnani:** Validation, Review. **S. Reggiani:** Conceptualization, Methodology, validation, Writing – original draft, Supervision. **R. Sankaralingam:** Conceptualization, Validation, Review. **M. Dissegna:** Conceptualization, Validation, Review. **G. Boselli:** Conceptualization, Methodology, Writing-review, Supervision, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The authors do not have permission to share data.

References

[1] P. Galy, Electro static discharge (ESD) one real life event: Physical impact and protection challenges in advanced CMOS technologies, in: 2014 International Semiconductor Conference, CAS, 2014, pp. 31–34, http://dx.doi.org/10.1109/SMICND.2014.6966382.

[2] S. Bub, M. Mergens, A. Hardock, S. Holland, A. Hilbrink, Automotive high-speed interfaces: Future challenges for system-level HV-ESD protection and first- Time-right design, in: 2021 43rd Annual EOS/ESD Symposium, Vol. 43, EOS/ESD, 2021, pp. 1–10, http://dx.doi.org/10.23919/EOS/ESD52038.2021.9574746.

[3] J. Salcedo, J. Liou, J. Bernier, Design and integration of novel SCR-based devices for ESD protection in CMOS/BiCMOS technologies, IEEE Trans. Electron Devices 52 (12) (2005) 2682–2689, http://dx.doi.org/10.1109/TED.2005.859662.

[4] C.R. Zhan, P. Besse, J.-P. Laine, A. Salles, High-performance bi-directional SCR developed on a 0.13 um SOI-based smart power technology for automotive applications, in: 2017 39th Electrical Overstress/Electrostatic Discharge Symposium, EOS/ESD, IEEE, 2017, pp. 1–7, http://dx.doi.org/10.23919/EOSESD.2017.8073448.

[5] H. Xiaozong, L. Fan, L. Zhiwei, A holding voltage adjustment technique of SCR for ESD protection, in: 3rd International Conference on Intelligent Energy and Power Systems, 2017, pp. 72–76.

[6] W. Song, R. Chen, Z. Tong, F. Hou, F. Du, Z. Liu, H. Liu, Robust silicon-controlled rectifier with high-holding voltage for on-chip electrostatic protection, IEEE Trans. Electron Devices 69 (2) (2022) 696–703.

[7] Y. Liu, Y. Wang, X. Jin, J. Yang, Y. Peng, J. Luo, A novel robust SCR with high holding voltage for on-chip ESD protection of industry-level bus, Solid-State Electron. 208 (2023) 108762, http://dx.doi.org/10.1016/j.sse.2023.108762.

[8] S. Pendharkar, R. Teggatz, J. Devore, J. Carpenter, T. Efland, C.-Y. Tsai, SCR-LDMOS. A novel LDMOS device with ESD robustness, in: 12th International Symposium on Power Semiconductor Devices & ICs. Proceedings (Cat. No. 00CH37094), IEEE, 2000, pp. 341–344.
[9] M. Shrivastava, H. Gossner, A review on the ESD robustness of drain-extended MOS devices, IEEE Trans. Device Mater. Reliab. 12 (4) (2012) 615–625.
[10] F. Ma, B. Zhang, Y. Han, J. Zheng, B. Song, S. Dong, H. Liang, High holding voltage SCR-LDMOS stacking structure with ring-resistance-triggered technique, IEEE Electron Device Lett. 34 (9) (2013) 1178–1180.
[11] L. Qian, M. Li, Y. Wang, H. Wu, T. Liu, J. Guo, W. Zhu, S. Hu, A novel segmented LDMOS-SCR structure with 8-kV HBM ESD robustness in CMS analog multiplexer, IEEE Trans. Electron Devices 69 (12) (2022) 6904–6909.
[12] X. Bao, X. Jin, An improved LDMOS-SCR design for high-voltage ESD, in: 2022 International EOS/ESD Symposium on Design and System, IEDS, IEEE, 2022, pp. 1–4.
[13] L. Zunarelli, L. Balestra, S. Reggiani, R. Sankaralingam, M. Dissegna, G. Boselli, TCAD study of the holding-voltage modulation in irradiated SCR-LDMOS for HV ESD protection, in: 2023 IEEE International Reliability Physics Symposium, IRPS, IEEE, 2023, pp. 1–6.
[14] S.-Y. Liu, W.-F. Sun, H.-W. Pan, H. Wang, Q.-S. Qian, A novel latch-up free SCR-LDMOS for power-rail ESD clamp in half-bridge driver IC, in: 2012 IEEE 11th International Conference on Solid-State and Integrated Circuit Technology, 2012, pp. 1–3, http://dx.doi.org/10.1109/ICSICT.2012.6466723.
[15] H.-W. Chen, S.-L. Chen, Y.-T. Huang, H.-H. Chen, ESD improvements on power N-channel LDMOS devices by the composite structure of super junctions integrated with SCRs in the drain side, IEEE J. the Electron Devices Soc. 8 (2020) 864–872, http://dx.doi.org/10.1109/JEDS.2020.3013442.
[16] Synopsys SDevice Version S-2021.06, June 2021, 2021.
[17] S. Reggiani, E. Gnani, M. Rudan, G. Baccarani, S. Bychikhin, J. Kuzmik, D. Pogany, E. Gornik, M. Denison, N. Jensen, G. Groos, M. Stecher, A new numerical and experimental analysis tool for ESD devices by means of the transient interferometric technique, IEEE Electron Device Lett. 26 (12) (2005) 916–918, http://dx.doi.org/10.1109/LED.2005.859685.
[18] Z. Pan, D. Schroeder, S. Holland, W.H. Krautschneider, Understanding and modeling of diode voltage overshoots during fast transient ESD events, IEEE Trans. Electron Devices 61 (8) (2014) 2682–2689, http://dx.doi.org/10.1109/TED.2014.2330365.
[19] S. Reggiani, G. Barone, E. Gnani, A. Gnudi, G. Baccarani, S. Poli, R. Wise, M.-Y. Chuang, W. Tian, S. Pendharkar, et al., Characterization and modeling of electrical stress degradation in STI-based integrated power devices, Solid-State Electron. 102 (2014) 25–41.
[20] S. Reggiani, G. Baccarani, E. Gnani, A. Gnudi, M. Denison, S. Pendharkar, R. Wise, S. Seetharaman, Explanation of the rugged LDMOS behavior by means of numerical analysis, IEEE Trans. Electron Devices 56 (11) (2009) 2811–2818, http://dx.doi.org/10.1109/TED.2009.2030836.
[21] J. Barth, K. Verhaege, L. Henry, J. Richner, TLP calibration, correlation, standards, and new techniques, IEEE Trans. Electron. Packag. Manuf. 24 (2) (2001) 99–108, http://dx.doi.org/10.1109/6104.930960.
[22] L. Zunarelli, S. Reggiani, E. Gnani, R. Sankaralingam, M. Dissegna, G. Boselli, TCAD investigation of power-to-failure evaluation for ultrafast events in BJT-based ESD protection cells, in: 2022 IEEE International Reliability Physics Symposium, IRPS, IEEE, 2022, pp. 6C–2.
[23] G. Notermans, H.-M. Ritter, S. Holland, D. Pogany, Dynamic voltage overshoot during triggering of an SCR-type ESD protection, IEEE Trans. Device Mater. Reliab. 19 (4) (2019) 583–590, http://dx.doi.org/10.1109/TDMR.2019.2952713.