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Modular Multilevel Converters Based on Interleaved Half-Bridge Submodules

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***Abstract*—This paper reports a novel modular multilevel converter with interleaved sub-modules (ISM-MMC). The ISM-MMC exhibit a higher scalability in current rating then conventional MMC structures with parallel devices. It can employ low-cost, low-current power switches rather than their bulky and expensive counterparts normally designed in classical MMCs. Another remarkable feature is that the number of the output voltage levels is synthetically multiplied by the number of interleaved SMs. The ISM-MMC is capable of bringing the known advantages of MMC to low voltage – high power applications making it a good candidate for the sector of ultra-fast chargers for electrical vehicles where typical power rating in excess of 1 MW is required for the low voltage supply. A proper modulation scheme is implemented and explained in this paper. A comparison with a classical MMC topology is also provided in terms of number of voltage levels, output voltage harmonic content, and number of components by fixing the number of SMs. Simulation results are given to demonstrate the feasibility of the proposed topology and the implemented modulation scheme. Despite this paper is dealing with a single-phase configuration, the extension to a three-phase scheme can be obtained in a straightforward manner.**

Keywords— modular multilevel converter (MMC), interleaved half-bridges, sub-modules, modular, modulation technique, ultra-fast ev chargers.

NOMENCLATURE

u , l	Upper and lower arm indicators
N	Number of submodules in each arm
K	Number of interleaved half-bridges inside each submodule
n , k	Ordinal number of submodule and interleaved half-bridge
$g_{k,n}$	Top switch gate signal in the k-th leg of the n-th submodule
ζ_n	Sum of the gate signals inside the n-th submodule
V_{dc} , V_d	Dc-link voltage and dc-link capacitor voltage
i , i_c	Output and circulating currents
i_u , i_l	Upper and lower arm currents
$i_{k,n}$	Current in the k-th leg of the n-th submodule
v_{SMn} , $v_{c,n}$	n-th total submodule and capacitor voltages
v_u , v_l	Upper and lower arm voltages
v	Output voltage
R_{arm}, L_{arm}	Internal resistance and inductance of equivalent arm inductor
R , L	Internal resistance and inductance of individual inductors in each of half-bridges

I. INTRODUCTION

Nowadays, high-power voltage source converters (VSCs) are widely adopted in the market over its counterpart, the current source converters. Multilevel VSC topologies are now attracting more interest from researchers and industry thanks to their improved output voltage harmonic content, higher efficiency, and increased input/output voltages [1]. Among the different multilevel VSC schemes, modular multilevel converters (MMCs) are surely more vastly applied thanks to their higher modularity, easier scalability, better reliability, fault tolerant operation, and higher quality output waveforms in comparison with the classical multilevel converters [2]. These advantages have led this topology to be the main choice in high-voltage direct-current (HVDC) applications and in medium-voltage (MV) motor drives [3]-[4].

Different MMC configurations have been already presented, such as single-star, single-delta, and double-star schemes [5]. Apart the different MMC configurations, several submodule (SM) topologies have been also proposed in the literature. The classical one consists of either a half-bridge (HB) or a full-bridge (FB) cell. However, in order to meet either the different application requirements (such as decreased capacitor voltage ripple or reduced circulating currents) or to increase the number of levels per each sub-module, multilevel configurations can be also adopted. Examples are the cascaded H-bridge, the H-bridge neutral-point clamped (NPC), the active NPC, the neutral-point piloted, the flying capacitor, and the clamp-double SM [2].

To control this kind of converters, different pulse width modulation schemes can be used [6]. Phase-shifted (PS) carrier and level-shifted (LS) carrier schemes are widely adopted. The latter can be distinguished in three kinds: phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD). Another way to control the MMC is to utilize the so-called nearest level control (NLC). The latter is widely adopted in case of high number of SMs thanks to the simple implementation and the absence of synchronization problems. In any case, all these modulation techniques need a proper capacitor voltage balancing algorithm in order to balance the energy stored in each submodule [7].

The interleaving concept is widely adopted in power converters to increase the output current and to reduce the current ripple, keeping the modularity [8]. The concept is still the parallel connection of several converters [9]. Some works have tried to increase the parallelism inside the single converter by adopting interleaved topologies. Authors in [10] propose an interleaved two-phase quasi three-level dc-dc MMC with coupled inductors. An interleaved dc-dc MMC is also presented in [11] for medium voltage large scale photovoltaic power plants. In [12] an interleaved stage ac-dc bidirectional power converter topology is suggested for medium voltage railway systems.

To the best of authors' knowledge, all the previous works have focused on interleaving either the converters or the legs, and no works are considering the interleaving concept at the submodule level. For this reason, a new interleaved sub-module topology is proposed in this paper. It allows increasing the total output current using a modular structure, improving the output waveform harmonic content, and employing typical low-current, low-cost commercial power switches. Along with the new topology, a proper modulation scheme is developed to control the converter. In particular, on one hand, a LS carrier modulation scheme is adopted to control the different SMs; on the other hand, an interleaved carrier scheme is implemented to drive the legs inside each SM.

Simulation results demonstrate the feasibility of the new MMC with the proposed SM topology. A comparison between the ISM-MMC and the classical MMC schemes is also accomplished in terms of number of voltage levels, output waveform quality, and number of components, making reference to a single-phase configuration.

The paper is structured as follows. Section II introduces the ISM-MMC topology. The modulation scheme and the capacitor voltage balancing algorithm are given in Section III. Simulation results and the comparison with the classical topology are provided in Section IV. Conclusions are finally drawn.

II. Proposed Topology

The standard, most popular and widely applied circuit configuration of a single-phase MMC is shown in Fig. 1. A dc source with constant dc voltage is applied to the dc terminals of the converter. In parallel to the dc source there are two series connected dc-link capacitors with common midpoint grounded, creating a reference voltage for single-phase MMC configuration. The voltages across these dc-link capacitors are assumed to be constant $V_{du} = V_{dl} = V_{dc}/2$. The output ac voltage is defined between the midpoint of the converter leg and the ground. The MMC employs two arm structure. The arm that is coupled with the positive dc bar is commonly named as the upper arm (u) and the arm linked with negative bar is referred to as the lower arm (l). Each arm consists of N series connected power submodules and an arm inductor. Every single SM is made up by a half-bridge leg joined in parallel with a capacitor. The output terminals of the submodule are the midpoint of the half-bridge leg and one of the sides of the capacitor (here low side is taken by default). The arm inductor has a purpose to limit the current spikes caused by the insertion or bypass of the SM's capacitor [13].

This arm inductor can be distributed between the arm submodules, without affecting the converter characteristics and eventually realizing configuration given in Fig. 2a with the submodule structure shown in Fig. 2b. The structure of ISM-MMC submodule is illustrated in Fig. 2c. It may be easily distinguished that the presented SM architecture can be directly derived from Fig. 2b by splitting one into K parallel connected and equally shared 'inductor – HB-leg' assemblies. It is straightforward that the current rating of these units can be K times lower with respect to the rated current of the submodule in Fig. 2b. Alternatively, the total rated current of the new SM can be K times higher than the classical HB-based SM, preserving properties of individual HB-legs.

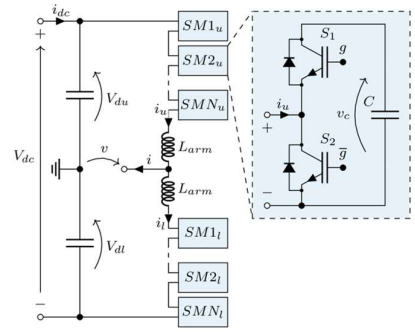

Fig. 1. Standard MMC configuration with half-bridge submodule.

The output current i and the circulating current i_c for both the configurations are defined as:

$$\begin{cases} i = i_u - i_l \\ i_c = \dfrac{i_u + i_l}{2} \end{cases} \tag{1}$$

where i_u and i_l are the upper and lower arm current, respectively. For the sake of comparison, the ac output, arm and submodule voltages of both configurations are defined in the same way as depicted in Fig. 2. The voltage of submodule n^{th} (v_{SMn}) is measured between the output terminals of the submodule and it is expressed as:

$$v_{SMn} = \frac{1}{K}\left[L\sum_{k=1}^{K}\frac{di_{k,n}}{dt} + R\sum_{k=1}^{K} i_{k,n} + \mathfrak{z}_n\, v_{c,n}\right] \tag{2}$$

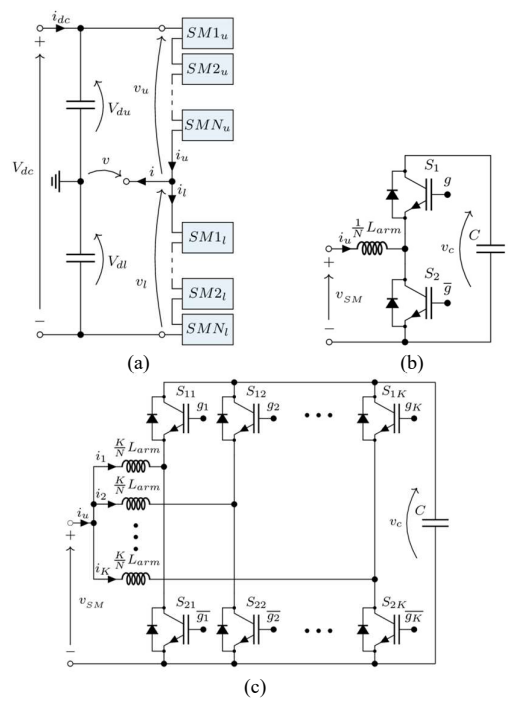

Fig. 2. Scheme of (a) the generic MMC structure, (b) half-bridge submodule with distributed arm inductor (with reference to Fig. 1) and (c) the proposed interleaved half-bridge submodule.

where K is the number of legs inside the submodule (K=1 in the case of the classical MMC Fig. 2b, K>1 in case of the interleaved configuration Fig. 2c) and n represents an ordinal number of the corresponding n^{th} SM of the upper or lower arm. Parameters L and R are the inductance and internal resistance of a leg inductor inside each SM, respectively. v_c is the SM

capacitor voltage and $\mathfrak{z}$ is the corresponding number of legs which the top switch is on and it can be evaluated as the sum of gate signals $g_{k,n}$ in n^{th} submodule:

$$\mathfrak{z}_n = \sum_{k=1}^{K} g_{k,n} \tag{3}$$

The latter can be either 0 or 1 in the classical half-bridge SM topology. $i_{k,n}$ is the current of the kth leg inside the nth interleaved SM. It is worth to note that i_k is equal to $i_{u,l}$ in case of classical MMC being the SM composed of only one HB-leg. Considering that the sum of the individual leg currents is equal to the arm current, (2) can be simplified as:

$$v_{SMn}|_{u,l} = \frac{1}{K}\left[L\frac{di_{u,l}}{dt} + Ri_{u,l} + \mathfrak{z}_n\, v_{c,n}\right] \tag{4}$$

The upper arm voltage v_u and the lower arm voltage v_l are measured between the midpoint of the converter's arm and the corresponding dc rails. Their value is given by:

$$v_{u,l} = \sum_{n=1}^{N} v_{SMn}|_{u,l} \tag{5}$$

where $v_{SMn}|_{u,l}$ is the nth submodule voltage of the upper or lower arm. Assuming balanced and constant dc-link capacitor voltages equal to $V_{dc}/2$, (6) can be easily derived:

$$\begin{aligned} \frac{V_{dc}}{2} - v_u &= v \\ -\frac{V_{dc}}{2} + v_l &= v \end{aligned} \tag{6}$$

where v is the output voltage. Substituting (4) and (5) into (6), the following equations can be found:

$$\begin{aligned} &\frac{V_{dc}}{2} - \frac{NL}{K}\frac{di_u}{dt} - \frac{NR}{K}i_u - \sum_{n=1}^{N}\frac{1}{K}\mathfrak{z}_{u,n}\, v_{cu,n} = v \\ &-\frac{V_{dc}}{2} + \frac{NL}{K}\frac{di_l}{dt} + \frac{NR}{K}i_l + \sum_{n=1}^{N}\frac{1}{K}\mathfrak{z}_{l,n}\, v_{cl,n} = v \end{aligned} \tag{7}$$

Adding and subtracting the two expressions in (7), while taking into account (1), two equations controlling the output and circulating currents are found:

$$\begin{aligned} \frac{NL}{2K}\frac{di}{dt} &= \frac{1}{2K}\sum_{n=1}^{N}\left[\mathfrak{z}_{l,n}\, v_{cl,n} - \mathfrak{z}_{u,n}\, v_{cu,n}\right] - \frac{NR}{2K}i - v \\ \frac{NL}{K}\frac{di_c}{dt} &= \frac{V_{dc}}{2} - \frac{1}{2K}\sum_{n=1}^{N}\left[\mathfrak{z}_{l,n}\, v_{cl,n} + \mathfrak{z}_{u,n}\, v_{cu,n}\right] - \frac{NR}{K}i_c \end{aligned} \tag{8}$$

By selecting the SM inductance L equal to K/N times the arm inductance L_{arm}, as shown in Fig. 2, the same equivalent inductance and resistance of the classical MMC topology is achieved:

$$\begin{aligned} L &= \frac{K}{N}L_{arm} \\ R &= \frac{K}{N}R_{arm} \end{aligned} \tag{9}$$

In the following discussion the concept of reduced current rating of the components, which compose a SM, will be examined in detail with reference to the standard MMC topology. This means that, for the sake of debate, the current ratings of the compared MMC configurations, as well as number of arm submodules will be preserved, while the current ratings of SM components, namely active switches, in these two converters will vary. Other possible comparative studies, such as identical number of HB-legs (series connected in the standard MMC and parallel connected in the ISM-MMC), similar characteristics of reactive components (inductors, capacitors) and so on, will be examined in future works. By taking advantage of a proper modulation for driving interleaved HB-legs of each SM, the output characteristics of the converter can be significantly improved.

III. Modulation and Capacitor Voltage Balancing

There are generally two fundamental issues to be dealt with while selecting an appropriate modulation strategy for the standard MMC converter. Namely, the modulation of output voltages and balancing of the submodule capacitor energies within each converter arms [6].

Several researchers have been focused on the study of suitable modulation strategies for the standard MMC to handle the aforementioned issues. Among them the most widely employed modulation techniques can be classified as multilevel carrier-based PWM, staircase waveform modulation, and space vector modulation (SVM) [6]-[14]. Similarly, the modulation methods to deal with interleaved HB-legs have been well-reported in literature as well. Most of the attention in this regard has been drawn to a phase-shift in the operation of the parallel legs, generally achieved through phase-shifted PWM (PS-PWM) [15] or SVM [16]. Another trending modulation strategy to handle interleaving in VSCs is level-shifted PWM (LS-PWM) [17], [18].

For the ISM-MMC topology, a multilevel carrier-based PWM technique, precisely the LS-PWM, was selected to modulate output voltage and the phase-shifted PWM to commutate legs in each SM. Therefore, the modified modulation strategy for the new converter is a combination of LS-PWM and PS-PWM. Similarly to the classical LS-PWM, the hybrid modulation method employs its variations, such as phase disposition (PD), phase opposition disposition (POD), alternate phase opposition disposition (APOD) and other. The choice of the phase shift between level-shifted carries affects performance of the converter [6]. To introduce these differences for the ISM-MMC configuration, this section demonstrates modified PD and APOD methods. The detailed performance comparison is discussed in Section IV.

A. PD Level-shifted PWM

Fig. 3 depicts the modified PD LS-PWM method with reference to the ISM-MMC that has 2 submodules in each arm and 3 HB-legs in each submodule. Here all corresponding level-shifted carriers have the same phase angle and thus only differ in terms of a level offset. As it was previously stated carriers at different levels are responsible for inserting or bypassing the corresponding SMs in each arm. On the other hand, the carriers at one level are evenly shifted to operate the composing submodule HB-legs. The reference signals (u_{ref}, -u_{ref}) are in charge to modulate arm voltages. The corresponding to this modulation technique maximum number of output voltage levels can be calculated by:

$$Lev_{PD} = 2KN + 1 \tag{10}$$

In the case of the classical SM, K is equal to 1 and then the classical number of levels is achieved, i.e., $2N+1$.

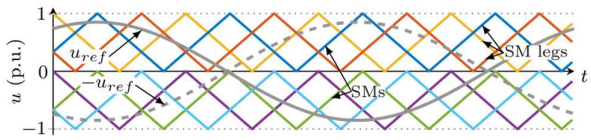

Fig. 3. Modified PD Level-shifted PWM

B. APOD Level-shifted PWM

Likewise, APOD LS-PWM can be implemented on the ISM-MMC. In this case, by alternating phase shifts of zero and π rad between adjacent level-shifted carriers that they are always in anti-phase, the APOD version of the modified LS-PWM is realized. The corresponding maximum number of output voltage levels is given by:

$$Lev_{APOD} = KN + 1 \tag{11}$$

In the classical SM K is equal to 1 and then the standard number of voltage levels is obtained, i.e., N+1.

C. Capacitor Voltage Balancing

The balancing of the capacitor voltages has been already well addressed in the literature [7], [19]. In this paper a classical approach based on a sorting algorithm with reassignment of the LS-PWM gate firing signals is adopted and it will not be discussed in detail. The only difference of the employed sorting approach with the classical one is that all driving signals of one submodule exchange with corresponding signals from another submodule.

IV. Simulation Results

In this section, numerical simulation results are presented to demonstrate operation behavior of the proposed MMC structure with interleaved HB-leg submodules. The comparison of working characteristics between standard and newly introduced topologies are made basing on the converter structures given in Fig. 2. A test *RL* load has been connected to the ac side of the converters. Circuital parameters are summarized in Table I. In all simulation results that are presented here, the modulation index m has been kept at its maximum value equal to 1 (in per unit) within linear range (sinusoidal modulation without overmodulation) and default sorting frequency has been chosen 1 kHz unless otherwise is specified.

Table I. Main System Parameters

Description	Labels	Parameters
number of SM in each arm	N	2
number of legs in each SM (std./interleav.)	K	1 and 3
dc voltage	V_{dc}	240 V
arm inductor	R_{arm}, L_{arm}	563.3 mΩ, 2.6 mH
capacitor in each SM	C	4 mF
RL load	R_o, L_o	10 Ω, 1.8 mH
fundamental frequency	f	50 Hz
switching frequency	f_{sw}	4 kHz
sorting frequency	f_{sort}	1 kHz

Fig. 4 presents a comparison of ac output voltages in case of the classical MMC (top) and ISM-MMC (bottom), modulated via APOD (left) and PD (right) LS-PWM. It is evident that number of voltage levels has been drastically increased passing from standard topology to the new one. Moreover, that number can be further boosted by applying PD LS-PWM over its APOD version. Given the number of submodules (N) and number of legs in each submodule (K), listed in Table I, (9) and (10) can be easily verified by Fig. 4. The effect of number level difference between variations of LS-PWM for classical MMC architecture has been well addressed in [6] thus, it is not analyzed in detail in this paper. However, for the sake of comparison, Fig. 5 depicts ac output voltage spectra for the case of ISM-MMC, modulated via APOD (top) and PD (bottom) LS-PWMs. One can notice a cumulative effect of the commutating legs, shifting switching harmonics and its multiples to a higher frequencies range with reduced magnitude. Specifically, first switching harmonics appear around 12 kHz in the case of APOD LS-PWM and around 24 kHz for PD LS-PWM, while the carriers' frequency is set to 4 kHz.

Likewise, Fig. 6 illustrates ac output current for the compared cases. Although, the change of current profile is well visible, switching from APOD to PD in conventional MMC structure, however, that change is blurry for the ISM-MMC. Since the output current profile and its harmonic spectrum is strongly affected by the test load, it has not been examined further and shown only in the sake of completeness of the comparison.

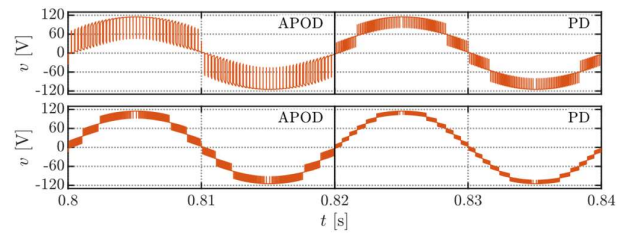

Fig. 4. Output voltage in case of standard MMC (top) and MMC with interleaved HB-leg SMs (bottom), modulated via APOD and PD LS-PWM

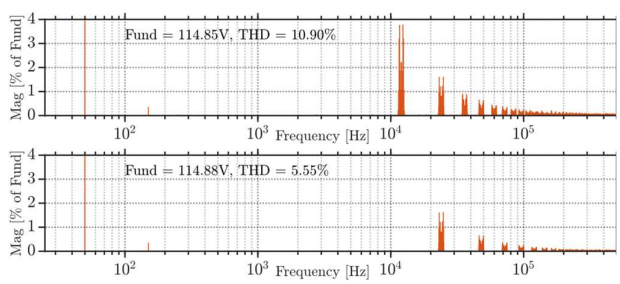

Fig. 5. Output voltage spectra in case of MMC with interleaved HB-leg SMs, modulated via APOD (top) and PD (bottom) LS-PWM

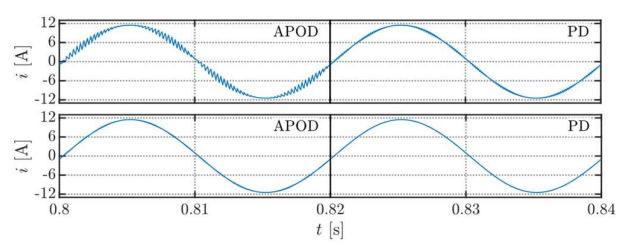

Fig. 6. Output current in case of standard MMC (top) and MMC with interleaved HB-leg SMs (bottom), modulated via APOD and PD LS-PWM

Upper arm voltage (purple) and current (green) in case of standard MMC (top) and MMC with interleaved HB-leg SMs (bottom) that are modulated via APOD (left) and PD (right) LS-PWM is depicted in Fig. 7. Alike in classical MMC the shape of arm voltages reiterates the profile of the corresponding ac output voltage, therefore, the number of levels is identical. Another thing is the circulating current form. One can notice the effect of specific modulation on output and circulating currents. Although output current for the case of classical MMC modulated via PD LS-PWM, presented in Fig. 6 (top, right), is less 'polluted' in terms of harmonic content, however, the corresponding circulating

arms current clearly contains additive high frequency components. Similar picture can be observed in the ISM-MMC structure, although it is not that evident as in the previous case. One important note shall be done here, namely, the purpose of this paper is to report operational differences between the standard MMC and MMC with interleaved HB-leg SMs, while implementation of control strategies to handle circulating current is out of the scope of this paper and will be investigated in the future works.

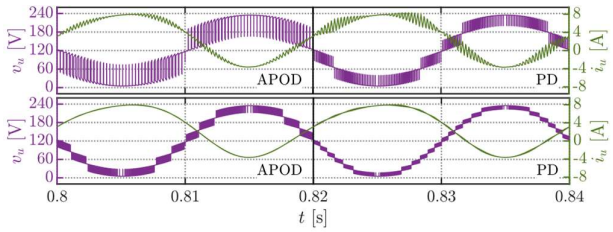

Fig. 7. Upper arm voltage (purple) and current (green) in case of standard MMC (top) and MMC with interleaved HB-leg SMs (bottom), modulated via APOD and PD LS-PWM

Fig. 8 shows submodule voltages in case of standard MMC (top) and MMC with interleaved HB-leg SMs (bottom), modulated via APOD (left) and PD (right) LS-PWM. It is quite apparent the difference among them, which lies in number of generated voltage levels and SM's resulting commutating frequency. The latter one is combined by commutations of each leg that compose the submodule, therefore, in general can be K times higher than, the switching frequency in classical MMC topology. Regarding the voltage levels and the shape of submodule voltage overall, it can be obtained by (3).

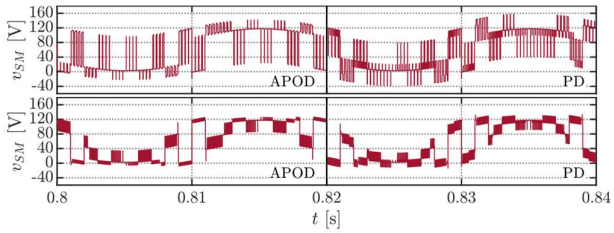

Fig. 8. Submodule voltage in case of standard MMC (top) and MMC with interleaved HB-leg SMs (bottom), modulated via APOD and PD LS-PWM

Fig. 9 and Fig. 10 demonstrate the effect of sorting frequency change on SMs' capacitor voltage balancing and individual HB-leg currents balancing with one SM. It is evident that by rising sorting frequency the better balancing of capacitor voltages among SM in each arm can be achieved (Fig. 9, top). In this instant the voltages are well balanced, practically following the same pattern. On the other hand, decreasing sorting frequency with a certain limit value, the capacitor voltages in one arm become misaligned (Fig. 9, bottom), although, they still fluctuate around a constant value.

The opposite effect can be noticed looking at Fig. 10. The leg currents within one submodule are well synchronized (Fig. 10, bottom) at low sorting frequencies and start having mismatch at higher ones. Another well detectable effect can be noticed by varying sorting frequency. Namely, the parts of leg currents with residual switching ripple can be distributed over a fundamental period with an increase of sorting frequency, while it becomes concentrated with lower value of sorting frequency. So overall, there exist a sorting frequency trade-off between SMs' capacitor voltage balancing and balancing of legs currents in a SM.

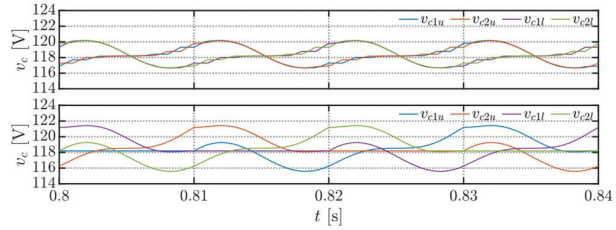

Fig. 9. Voltage across the capacitor in a submodule in case of MMC with interleaved HB-leg SMs at sorting frequency 1 kHz (top) and 100 Hz (bottom), modulated via PD LS-PWM

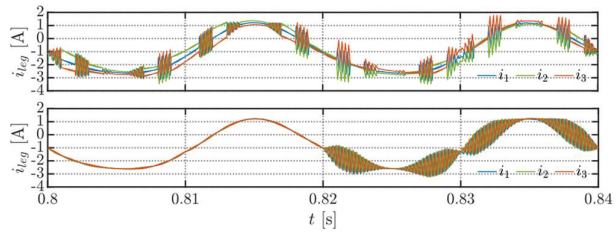

Fig. 10. Leg currents in a submodule in case of MMC with interleaved HB-leg SMs at sorting frequency 1 kHz (top) and 100 Hz (bottom), modulated via PD LS-PWM

V. Conclusion

The interleaved submodule topology has been introduced for modular multilevel converters. The main advantages of the proposed ISM-MMC configuration have been highlighted, i.e., an increased output current rating by adopting a modular structure and improved output waveforms.

A proper modulation scheme has been presented consisting of level shifted PWM for controlling the sub-modules and phase shifted PWM for driving the different legs inside each submodule.

Numerical simulations have been performed in Matlab/ Simulink environment. Output voltages and currents, arm voltages and currents, submodule voltages, and capacitor voltages have been compared in case of PD and APOD LS-PWMs for both the interleaved and classical MMC schemes. The simulation results validate the ISM-MMC topology and the implemented modulation technique, eventually proving feasibility of the proposed MMC structure.

A future development could refer to the extension of the considered single-phase scheme to a three-phase architecture, simply based on three single-phase MMC legs.

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